RESEARCH ARTICLE OPEN ACCESS

Harmonic Reduction on ACMI Using Programmable Logic Controller

Amuthan.S.K[1], Logesh.P[2], Eswaramoorthy K[3]
[1,2](Department Of Electrical And Electronics Engineering, Sasurie College Of Engineering, Vijayamangalam)
[3] (Assistant Professer, Department Of Electrical And Electronics Engineering, Sasurie College Of Engineering, Vijayamangalam)

ABSTRACT
Nowadays Multilevel inverter (MLI) technologies become extremely main choice in the area of high power medium voltage energy control. Although multilevel inverter has a number of advantages it has drawbacks in the layer of higher levels because of using large number of semiconductor switches. This project proposes Single-Phase fifteen-level inverter using seven switches. Inverter is capable of producing fifteen levels of the output voltage levels (Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7, Vdc/7 , 0, -Vdc/7,-2Vdc/7, -3Vdc/7, - 4Vdc/7, -5Vdc/7, -6Vdc/7, -Vdc) from the dc supply voltage The configuration used in this inverter is asymmetrical configuration. Multilevel inverter output voltage level increasing by using less number of switches driven by the multicarrier modulation techniques. A digital multi carrier PWM algorithm is implemented in a MATLAB simulation and the hardware is implemented by using PIC microcontroller.

Keywords- Asymmetric Cascaded Multilevel Inverter, Harmonic Distortion, MATLAB, semiconductor switches, THD

I. INTRODUCTION

A power inverter, or inverter, is an electrical power converter that changes direct current (DC) to alternating current (AC). Solid-state inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. But in normal inverters the THD is much higher. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

- **Staircase waveform quality:** Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

- **Common-mode (CM) voltage:** Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in.

- **Input current:** Multilevel converters can draw input current with low distortion.

- **Switching frequency:** Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. For example, given a 60Hz fundamental waveform, the 2nd, 3rd, 4th and 5th harmonic components will be at 120Hz, 180Hz, 240Hz and 300Hz respectively. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal values as a result of the summation of all these harmonic

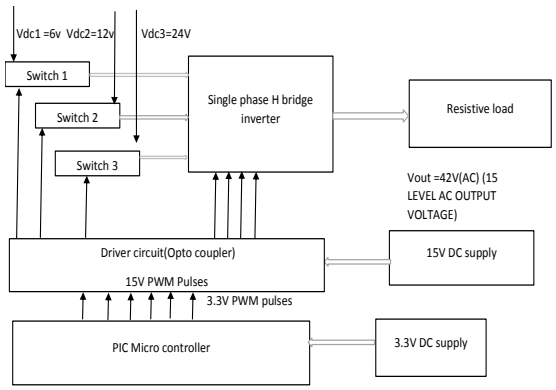
elements. The ideal sine wave as zero harmonic components. In that case, there is nothing to distort this perfect wave. Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave.

$$THD = \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2)}}{V_1} * 100\%$$

The formula above shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal. The higher the percentage, the more distortion that is present on the mains signal.

Harmonic distortion can have detrimental effects on electrical equipment. Unwanted distortion can increase the current in power systems which results in higher temperatures in neutral conductors and distribution transformers. Higher frequency harmonics cause additional core loss in motors which results in excessive heating of the motor core. These higher order harmonics can also interfere with communication transmission lines since they oscillate at the same frequencies as the transmit frequency. If left unchecked, increased temperatures and interference can greatly shorten the life of electronic equipment and cause damage to power systems. So for in this project for reducing the THD level the number of levels or steps can be increased.

II. BLOCK DIAGRAM



(Figure 2. 1 proposed block diagram)

H-Bridge Inverter:

Here the MOSFET based full bridge inverter circuit is cascaded for this fifteen level inverter. Three switches also connected with this h bridge inverter circuit. The snubber circuit (RC) is connected across all the switches for protecting the switching devices from dv/dt and di/dt ratings.

Microcontroller Pic16f877a

PIC 16F877 is a 40-pin 8-Bit CMOS FLASH Microcontroller from Microchip. The core architecture is high-performance RISC CPU with only 35 single word1 instructions. Since it follows the RISC architecture, all single cycle instructions take only one instruction cycle except for program branches which take two cycles. 16F877 comes with 3 operating speeds with 4, 8, or 20 MHz clock input. Since each instruction cycle takes four operating clock cycles, each instruction takes 0.2 micro seconds when 20MHz oscillator is used.

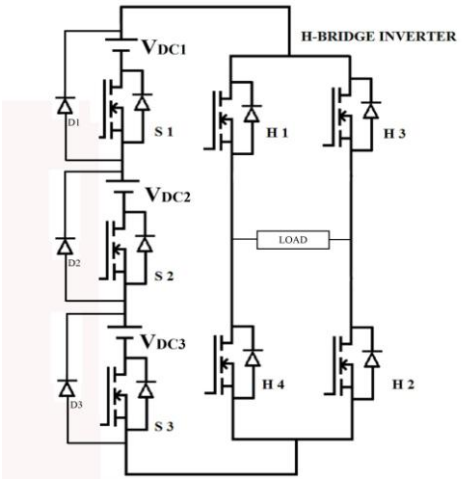
It has two types of internal memories: program memory and data memory. Program memory is provided by 8K words (or 8K*14 bits) of FLASH Memory, and data memory has two sources. One type of data memory is a 368-byte RAM (random access memory) and the other is 256-byte EEPROM (Electrically erasable programmable ROM). The core feature includes interrupt capability up to 14 sources, power saving SLEEP mode, and single 5V In-Circuit Serial Programming (ICSP) capability. The sink/source current, which indicates a driving power from I/O port, is high with 25mA. Power consumption is less than 2mA in 5V operating condition.

Load:

In this project the maximum output power level of the inverter is 60w. The maximum output voltage level of the inverter is 40 volts. For this power rating we can use lamp or small size motors. This project implemented in a prototype.

The voltage levels of the thirteen levels are (Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7, Vdc/7,0, -Vdc/7, -2Vdc/7, -3Vdc/7, - 4Vdc/7, -5Vdc/7, -6Vdc/7, -Vdc) From the DC supply. The voltage levels of the three sources are different. So this method of configuration is called as asymmetrical multilevel inverter. The inverter level is decided by both the modulation index and the applied DC voltage level of the inverter. By adjusting the different voltage level also we can able to increase the number of levels of the inverter. A FPGA controller is used for generating the PWM signals the inverter circuit. The switching devices used in this single phase inverter are MOSFET (IRF840). The power handling capacity of the inverter is low because the hardware is developed in a prototype.

3. Circuit Diagram



(figure 3.1 circuit diagram)

The proposed single-phase fifteen-level inverter was developed from the seven-level inverter. It comprises a Single phase conventional H-bridge inverter, three switches, and three voltage sources. This H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, for inverters of the same number of levels. Proper switching of the inverter can produce fifteen output-voltage levels (Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7, Vdc/7,0, -Vdc/7, -2Vdc/7, -3Vdc/7, - 4Vdc/7, -5Vdc/7, -6Vdc/7, -Vdc) from the dc supply voltage.

Voltage Level	S_3	S_2	S_1	H_1	H_2	H_3	H_4
V_{dc}	ON	ON	ON	ON	ON	OFF	OFF
$6/7V_{dc}$	ON	ON	OFF	ON	ON	OFF	OFF
$5/7V_{dc}$	ON	OFF	ON	ON	ON	OFF	OFF
$4/7V_{dc}$	ON	OFF	OFF	ON	ON	OFF	OFF
$3/7V_{dc}$	OFF	ON	ON	ON	ON	OFF	OFF
$2/7V_{dc}$	OFF	ON	OFF	ON	ON	OFF	OFF
$1/7V_{dc}$	OFF	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF
$-1/7V_{dc}$	OFF	OFF	ON	OFF	OFF	ON	ON
$-2/7V_{dc}$	OFF	ON	OFF	OFF	OFF	ON	ON
$-3/7V_{dc}$	OFF	ON	ON	OFF	OFF	ON	ON
$-4/7V_{dc}$	ON	OFF	OFF	OFF	OFF	ON	ON
$-5/7V_{dc}$	ON	OFF	ON	OFF	OFF	ON	ON
$-6/7V_{dc}$	ON	ON	OFF	OFF	OFF	ON	ON
$-V_{dc}$	ON	ON	ON	OFF	OFF	ON	ON

The proposed inverter's operation can be divided into fifteen switching states; the required fifteen levels of output voltage were generated as follows.

- Maximum positive output (*V*dc): *H*1 is ON; connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S1, S2, S3 are ON the voltage applied to the load terminals is *V*dc.
- 6/7 positive output (6*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S2, S3 are ON the voltage applied to the load terminals is 6*V*dc/7.
- 5/7 Positive output (5*V*dc/7): *H*1 is ON; connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S1, S3 are ON the voltage applied to the load terminals is 5*V*dc/7.
- 4/7 Positive output (4*V*dc/7): *H*1 is ON; connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is 4*V*dc/7.
- 3/7Positive output (3*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc,
- And *H2* is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is 3*V*dc/7.
- 2/7 Positive output (2*V*dc/7): *H*1 is ON; connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S2 is ON and S1, S3 is OFF. The voltage applied to the load terminals is 2*V*dc/7.
- 1/7 Positive output (1*V*dc/7): *H*1 is ON; connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S3 is ON and S1, S2 is OFF. The voltage applied to the load terminals is 1*V*dc/7.
- Zero output: All the switches S1, S2, S3, H1, H2, H3, and H4 are in OFF position.
- 1/7 Negative output (-1*V*dc/7): *H*3 is ON; connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S3 is ON and S1, S2 is OFF. The voltage applied to the load terminals is -1*V*dc/7.
- 2/7 Negative output (-2*V*dc/7): *H3* is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S2 is ON and S1, S3 is OFF. The voltage applied to the load terminals is -2*V*dc/7. 3/7 Negative output (-3*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is -3*V*dc/7.
- 4/7 Negative output (-4*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative

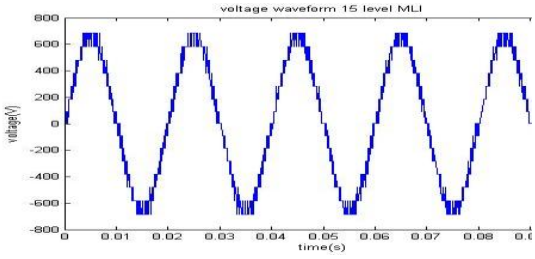
terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is -4*V*dc/7.

- 5/7 Negative output (-5*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground the switches S1,S3 are ON the voltage applied to the load terminals is 5*V*dc/7.
- 6/7 Negative output (-6*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S2, S3 are ON the voltage applied to the load terminals is –6*V*dc/7.

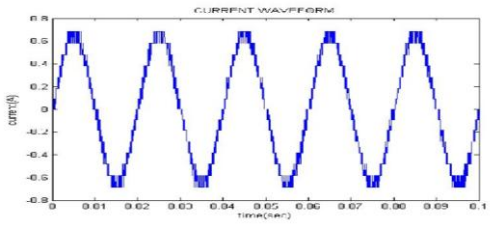
Configurations	No. Of Switches	No. Of Dc Sources	THD %
7 level MLI	9	4	18.07
9 level MLI	8	4	14.59
11 level MLI	8	3	11.50
15 level 12 switches	12	3	6.59
15 level 10 switches	10	3	2.89
15 level 7 switches	7	3	1.65

- Maximum Negative output (-*V*dc): *H*3 is ON; connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S1, S2, S3 are ON the voltage applied to the load terminals is –*V*dc.

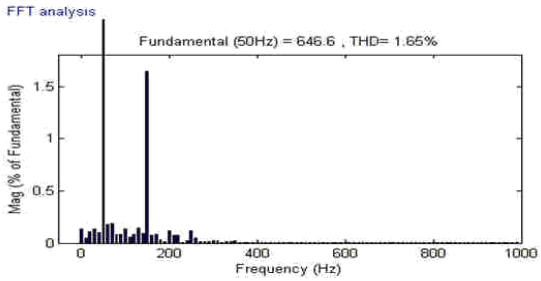
III. RESULT



proposed output voltage waveform



Proposed output current waveform



Proposed FFT Analysis Of Proposed System
Comparison table of FFT analysis

IV. CONCLUSION

In this projected paper, fifteen level asymmetric cascaded multilevel inverter is presented. The projected inverter can create high quality output voltage close to sinusoidal Waves. It is used to provide improved performance than the conventional cascaded multilevel inverter. And also this proposed method is used to minimize the switching losses. The total harmonic distortion (THD) can be supplementary reduced.

REFERENCE

[1]. Rahul Nair, Mahalakshmi R, Amrita Vishwa Vidyapeetham, (2015) ‘‘Power & Energy Performance of Three Phase II-level Inverter with reduced number of switches using different PWM Techniques’’ IEEE transactions vol.13.,

[2]. R Naveen Kumar. Energy Management system for Hybrid RES with Hybrid Cascaded Multilevel inverter. International Journal of Electrical and ComputerEngineering (IJECE). 2014; 4(1): 24~30.

[3]. Bangalore, India- 560 035. K. Gopakumar, Haitham Abu-Rub, P. P. Rajeevan and K.Sivakumar. (2013) “A Nine-Level Inverter Topology for Medium-Voltage Induction Motor Drive With Open-End Stator Winding” IEEE transactions on industrial electronics, vol.60, no.9.

[4]. S. Umashankar, T. S. Sreedevi, V. G.Nithya, and D. Vijayakumar (2013) “A New 7-Level Symmetric Multilevel

Inverter with Minimum Number of Switches Hindawi Publishing Corporation ISRN Electronics Volume 2013

[5]. T. V. V. S. Lakshmi, N. George, S. Umashankar, and D. Kothari, "Cascaded seven level inverter with reduced number of switches using level shifting PWM technique," in International Conference on Power, Energy and Control (ICPEC '13), pp. 676– 680, February 2013.

[6]. J. J. Nedumgatt, D. Vijayakumar, A. Kirubakaran, and S.Umashankar, "A multilevel inverter with reduced number of switches," in Proceedings of the IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS '12), pp.1–4, March 2012.

[7]. J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, pp. 724-738, 2002.

[8]. N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in Proc. IEEE PESC'91 , 1991, pp. 96–103

[9]. D Mohan, Sreejith B Kurub. Performance analysis of SPWM control strategies using 13 level cascaded MLI. IEEE international conference on advances in engineering science &management (ICAESM). 2012.RH Baker, LH Bannister. Electric Power Converter. U.S. Patent 3 867 643. 1975.

[10]. FZ Peng. A generalized multilevel inverter topology with self-voltage balancing. IEEE Trans. Ind. Applicat., 2001; 37: 611-618.

[11]. J. S. Lai and F. Z. Peng, "Multilevel converters-A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp. 509-517, May/June 1996.

[12]. akshay K. Rathore, Joachim Holtz, and Till Boller, "Generalized Optimal Pulse Width Modulation of Multilevel Inverters for Low-Switching-Frequency Control of Medium-Voltage High-Power Industrial AC Drives," IEEE Trans. Ind. Electron., vol. 60, Oct. 2013.

[13]. H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium voltage multilevel converters—State of the art, challenges and requirements in industrial applications," IEEE Trans. Ind. Electron., vol. 57, Aug. 2010.

[14]. Muhammad. H. Rashid, Power Electronics Circuits, Devices and Applications, Third Edition, Person Prentice Hall, pp.40-6430, 2004.

[15]. Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: survey of topologies, controls, and applications. IEEE Trans Ind Appl 2002;49(4):724–38.

[16]. T.F. Wu, H.S. Nien, C.L. Shen, T.M. Chen, "A single-phase inverter system PV power injection and active power filtering with nonlinear inductor consideration," IEEE Transactions on Industry Applications, Vol. 41, No. 4, pp. 1075–1083, Jul./Aug. 2005.

[17]. S.J. Park, F.S. Kang, M.H. Lee, C. Kim, "A new single-phase five level PWM inverter employing a deadbeat control scheme," IEEE Transactions on Power Electronics, Vol. 18 No. 3, pp. 831–843, May 2003

[18]. S.C¸ amur, B.Arifo˘glu, E.Bes¸er, E.Kandemir Bes¸er, "Harmonic analysis of an improved single phase five level inverter," Wseas Transactions on Power System, Vol. 1, No.2, pp 387-392, Feb. 2006.

[19]. K. Sudheer Kumar, E. Mohan, CH. Rajesh Kumar.

[20]. Lakshmi Ganesh, "New Multilevel Inverter Topology with Reduced Switching Devices for Hybrid Electric Vehicles".

[21]. Madhav D. Manjrekar, Peter K. Steimer and Thomas Lipo, "Hybrid Multilevel Power Conversion System: A Competitive solution for High Power applications".