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A VLSI Design of Power Efficient Reversible Logic Gates for Arithmetic and Logical Unit

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Abstract-
Reversible logic is one of the most important issues at present time and it has different areas for its application. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. A power efficient design of reversible gate is implemented in this paper.
One of the major goals of VLSI circuit design is to reduce the power dissipation which is demonstrated by R.Landauer in the early 1960s that states the loss of each one bit of information that dissipates at least KT ln2 joules of energy (heat) ,hence reversible logic based circuit design is an emerging research area which aims at reducing the information loss which causes the energy dissipation
This paper illustrates the VlSI design of reversible logic gates as a building blocks of arithmetic and logical unit. A power efficient GDI logic based standard reversible gates are designed .The schematics are designed in Tanner 14.1 s edit tool in 180 nm submicron technology. Logical and power synthesis is also given for the different gates.

Introduction

Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systems constructed using irreversible hardware was demonstrated by R. Landauer in the year 1960. According to Landauer's principle, the loss of one bit of information lost, will dissipate kT*ln (2) [3] joules of energy where, k is the Boltzmann's constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin[1]. The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods.
In 1973, Bennett, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2].
In this paper , a VLSI design of reversible gates are shown. A GDI CMOS building block is used for reversible implementation.

Reversible logic

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs[5].
Reversibility requires two basic conditions

- The first condition: logically reversible.
- The second condition: physically reversible

I. Reversible Logic Gates

The basic types of reversible logic gates are faynman, fredkin , toffoli ,TSG, URG, Pares.

A. Feynman Gate

The Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q= A XOR B. It has Quantum cost one [16].

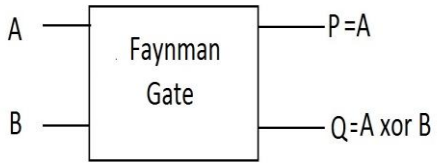

Figure 1. Faymnan gate

B. Fredkin Gate:

Fredkin gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=A'B+AC, R=AB+A'C. It has Quantum cost five [17].

Figure 2. Fredkin gate

C. Urg Gate*:*

It is a 3*3 gate with inputs (A, B, C) and outputs P= (A+B) xor C, Q= B, R = AB xor C [12]. Quantum implementation of R gate is not discussed by author

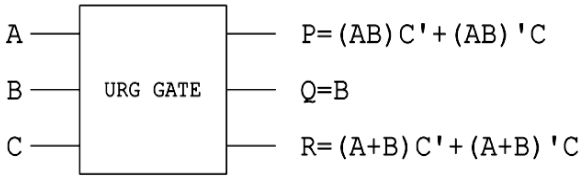

Figure 3.URG Gate

D. Tsg Gate**:**

The TSG gate is a (4, 4) reversible gate. The most significant aspect of this gate is that it can work singly as a reversible full adder, that is, a reversible full adder can be implemented using a single gate only [13].

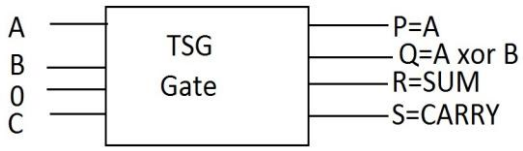

Figure 4.TSG Gate

II. Transistor implementation

A. Feynman Gate

Following figure shows the transistor implementation of the Feynman gate. The transistor implementation is fully reversible, that is, the given circuit can also work for forward as well as reverse operation.

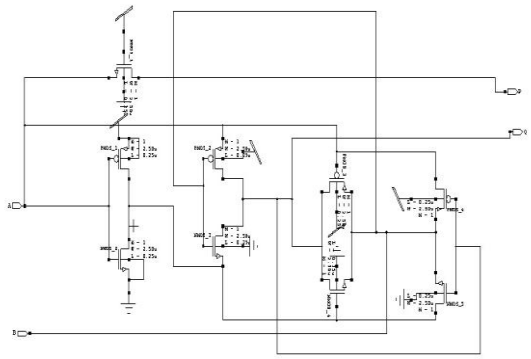

Figure 5. Faymnan gate

B. Fredkin Gate

Fig. 6 shows the transistor implementation of the Fredkin Gate that need only four transistors. In the implementation the output P is directly taken from input A as output P is same as input A. The proposed transistor implementation is suitable both for forward as well as backward computation ,i.e. completely reversible in nature

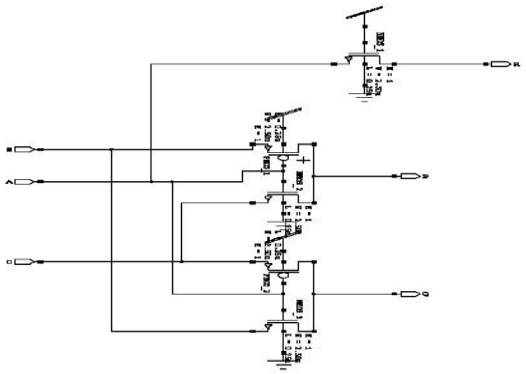

Figure 6. Fredkin gate

C. URG Gate

Fig. 13 shows the Transistor implementation of URG gate .It can simultaneously generate two output functions (from P and R). The output Q is taken with a nmos transistor. It takes 13 transistors for proposed completely reversible implementation of the URG gate. The proposed implementation is suitable for forward as well as backward computation.

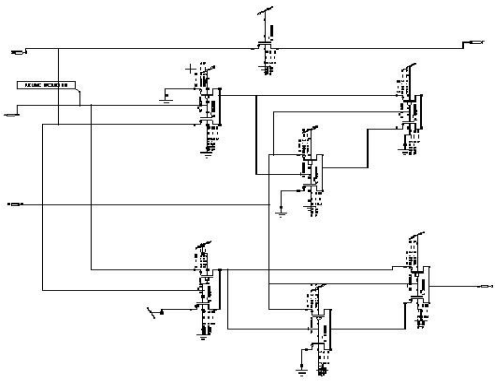

Figure 7. .URG GATE

D. Controlling gate

Fig. 8 shows the the controlling gate and its transistor implementation It can simultaneously generate three output functions (from P and R). The output P is taken with a nmos transistor. It takes 07 transistors for proposed completely reversible implementation of the gate.

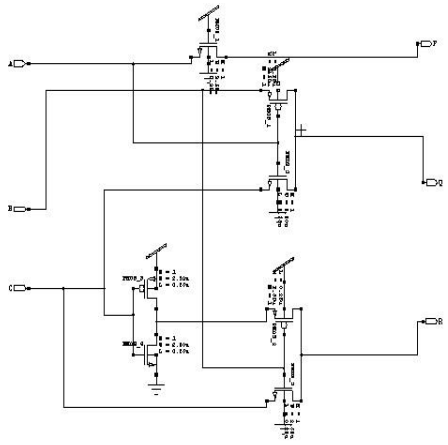

Figure 8. Controlling gate

III. Implemented Work

VlSI designing of the reversible circuits are done for checking the logical functionality of the designed gate in 180 nm technology using TANNER 14.11 Tools S edit tool.

The designs of the reversible gates are done using the GDI logic so as to minimize the required transistor count. The average power calculations are also perforemed for 180 nm technology for various supply voltages. The logical outputs are obtained on TANNER 14.11 W edit tool for transient analysis for same time duration for all designs.

IV. SIMULATION PARAMETERS

Following table shows the simulation parameters of the design

Sr. No.	Parameter	Values
1.	Voltage supply	5V, 3.4V,2.4V
2.	Technology	180nm
3	Simulation Time	1 µs
4	Analysis type	transient
5	Power caculation	Average Power(µw)

Table 1

V. SIMULATION RESULTS

Simulation is based on TANNER TOOL 14.11 S-Edit 180 nm design. Graph presented below are input and output signal at respective input and output terminal at each gate.

A. Feynman Gate

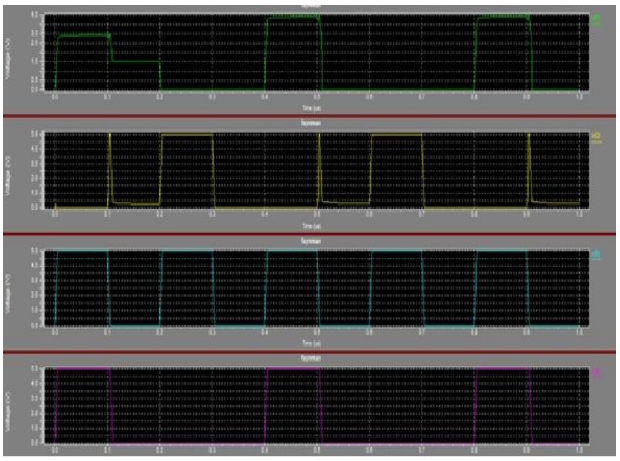

Figure 9

B. Fredkln Gate

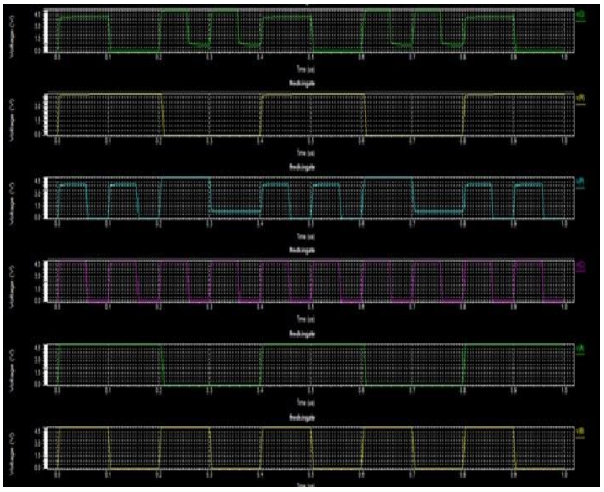

Figure 10

C. Urg Gate

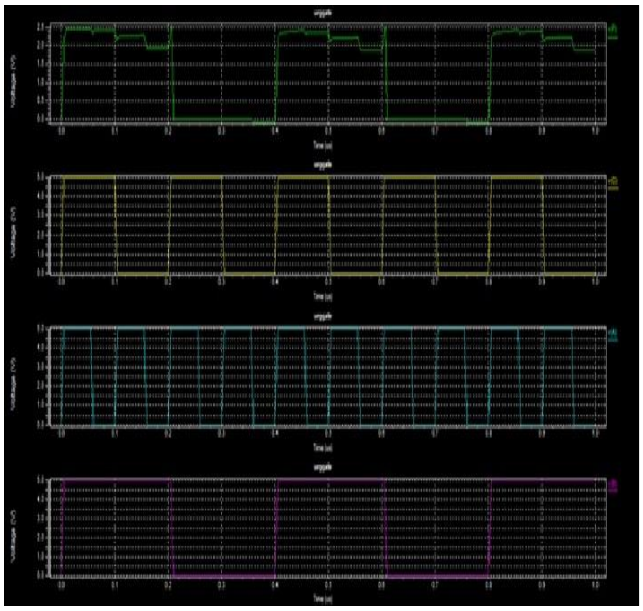

Figure 11

D. Controlling Gate

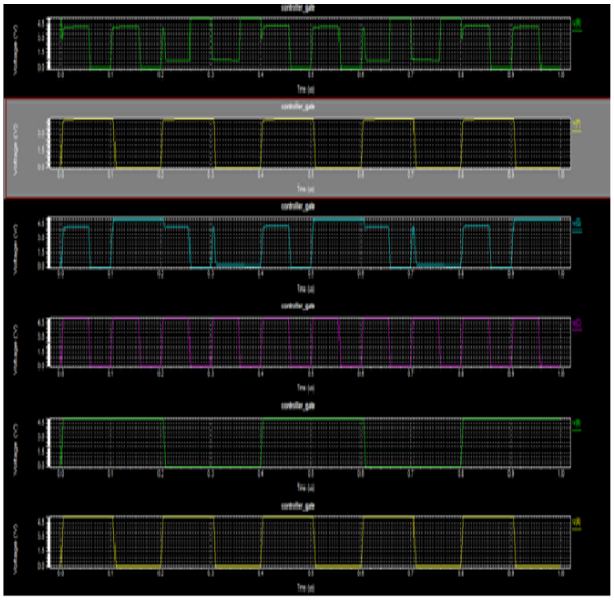

Figure 12

VI. COMPARISONS OF POWER

a. Forword power desipation proposed

Gate	Avarege power dessipation in watts (µw)		
	Vdd =5V	Vdd=3.4V	Vdd=2.4V
Faynman	0.50023	0.13206	0.028374
Fredkin	0.014998	0.0076445	0.0032307
URG	0.018321	0.0090824	0.0048336
Controlling	0.0099105	0.0020083	0.0017715

Table 3

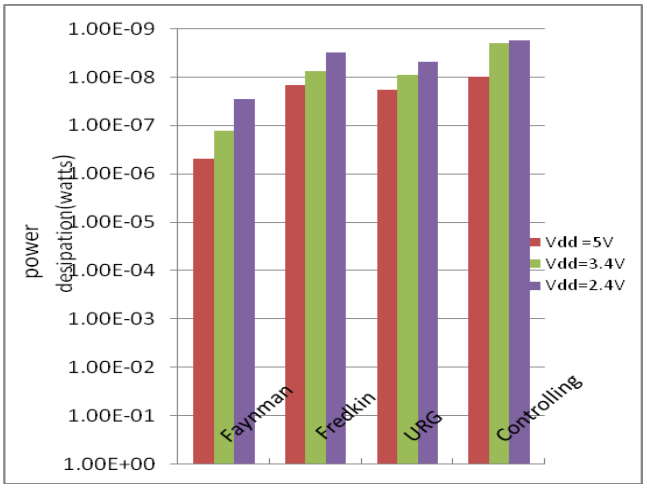

Figure 13. forward power desipation comparision chart

b. Backword power desipation proposed

Gate	Avarege power dessipation in watts (µw)		
	Vdd =5V	Vdd=3.4V	Vdd=2.4V
Faynman	0.50776	0.13589	0.030382
Fredkin	0.016438	0.0072264	0.0036543
URG	0.032842	0.015087	0.0075381
Controlling	0.014219	0.0083366	0.0045069

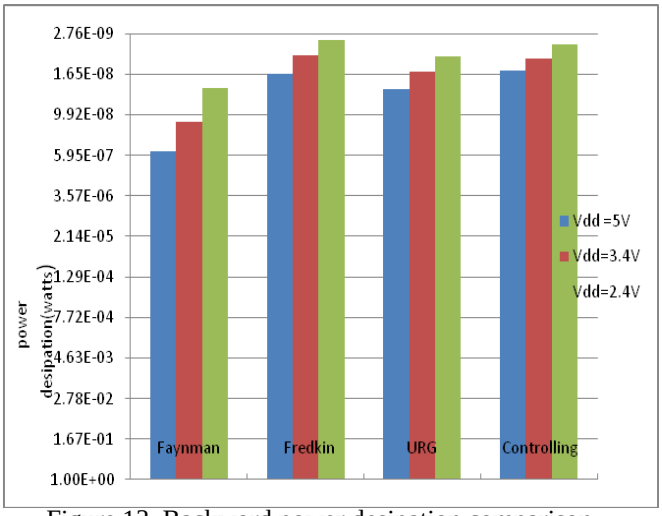

Figure 13. Backword power desipation comparison chart

C. POWER COMPARISON WITH EARLIER WORK

Gate	Avarege power dessipation in watts (µw)			
	Forward[18]	proposed	Backword[18]	Proposed
Faynman	0.9004727	0.50023	70.54828	0.50776
Fredkin	0.3859792	0.014998	0.3662202	0.016438
URG	0.5259238	0.018321	0.9492534	0.032842

CONCLUSION

The reversible circuits form the most useful building block of quantum computers. This paper presents the low power design of reversible gates. The paper also illustrates the logical and power synthesis of the four reversible logic gates. As the latest approach to sequential circuit design using reversible gate we made an attempt to compare our design of different reversible circuits with respect to power dissipation factor

In future work, we plan to implement the reversible logic gate based one bit and four bit arithmetic and logical circuit with power optimization using the designed reversible gates.

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