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VLSI Design of Multichannel AMBA AHB

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Abstract-
The on chip bus plays key role in the system on chip design by enabling the efficient integration of heterogeneous system component like CPUs, DSPs, application specific cores, memories, custom logic. As the level of design complexity has become higher, soc design requires a system bus with high bandwidth to perform the multiple operations in parallel. There have been several type of high performance on chip buses proposed to solve the bandwidth problem such as multichannel AHB busmatrix in ARM, the PLB crossbar switch in IBM, and CONMAX in silicore. Among them multichannel AHB busmatrix have been widely used in many SOC designs. This is because the simplicity of AMBA BUS of ARM, which attracts many IP designers and good architecture of the AMBA bus for applying embedded system with low power. In this project, we implemented multichannel AMBA AHB with its multiple arbiteration techniques such as round robin, fixed priority etc. AMBA AHB is basically single layer bus. But, in this project we implement the design of single layer amba ahb which includes four masters and four slaves and also multilayer AMBA AHB AHB which has four layer so that parallel operation can be performed, which improves the speed of the system. Multi-layer Amba ahb also includes 4-masters and 4-slaves. The bus width of both single layer and multi-layer amba ahb should be for 32- bit, 64-bit, and 128-bit. The design of flexible centre arbiter for flexible busmatrix supports the different priority policies such as round robin, fixed priority, intelligent clocking arbiter and others which are recently used. The design of single and multilayer Amba Ahb also include all the amba ahb signals or specifications. We designed and implemented this by using xillinx simulators and by using FPGA (SPARTAN) because this provides flexibility and high density.
Index Terms- Multichannel AHB busmatrix, on-chip bus, slave side arbitration, system on chip, AHB, arbiter.

I. INTRODUCTION:

The advanced microcontroller bus architecture bus architecture was introduced by ARM Ltd in 1996 and is widely used as the on chip bus in SOC designs. The registered trademark of ARM Ltd is AMBA. The first AMBA buses were Advanced system bus (ASB) and advanced peripheral bus (APB). IN its second version, AMBA 2, ARM added AMBA high performance bus (AHB) that is a single clock edge protocol.

In 2003 ARM introduced the 3rd generation, ARM3, including AXI to reach even high performance interconnects and the advanced trace bus as part of the core sight on chip debugs and trace solutions. Some manufacturer utilizes AMBA buses for non ARM designs. For example Infineon uses an AMBA bus for the ADM5120 SOC based on the MIPS architecture. The important aspect of SOC based on the MIPS architecture. The important side of a SOC is not only which components or blocks it uses, but also how they are interconnected. AMBA is a solution for the different blocks to interface with each others.

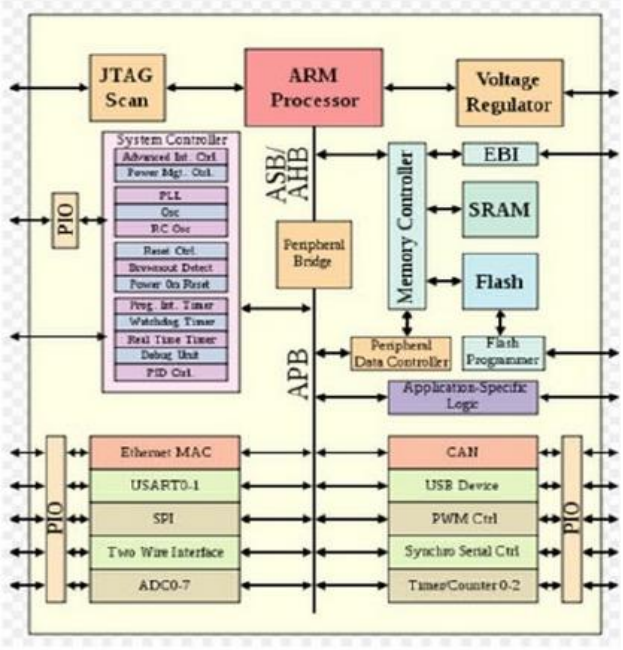

Fig.1 ARM SOC Block Diagram

Since its starts, the scope of AMBA has gone beyond microcontroller devices, and is now widely used on a

range of ASIC and SOC parts including applications processors used in modern portable mobile devices like smart phones.

A.Advanced High Performance (AHB) protocol:

AMBA AHB is high performance,high clock frequency system module. The AHB act as a high performance system bus.AHB supports the efficient connection between processors, on-chip memories and off- chip external memory interfaces with low power peripheral macro cell function.

B. Advanced Peripheral Bus (APB):

The AMBA is for low power peripherals. AMBA APB is improved for minimal power consumption and reduced interface complexity to support peripheral functions. APB can be used in addition with either version of the system bus.

C. Advanced System Bus (ASB):

The AMBA ASB is high performance system modules. AMBA ASB is an alternatives system bus suitable for use where the high performance features of AHB are not required. ASB also supports the ASB connection between processors, on chip memories and off-chip external memory interfaces with low power peripherals macro cell function.

E. Objectives Of AMBA Specification:

The AMBA specification gas been derived to satisfy four key requirements:

- To facilate the right-first-time development of embedded microcontroller products with one or more CPUs or signal processors.
- Next objective is that not be the technology dependent and ensure that highly reusable peripheral and system macro cells can be migrated across a diverse range of IC processes and be appropriate for full- custom ,standard cell and gate array technologies.
- To ensure modular system design to improve processor independence, providing a development of peripheral libraries.
- Next objective is that minimizing the silicon infrastructure required to support efficient on-chip and off-chip communication for both operation and manufacturing test.
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F. A Typical AMBA Based Microcontroller:

An AMBA based microcontroller typically consist of a high performance system backbone bus (AMBA AHB or AMBA ASB) able to sustain the external memory and DMA devices resides .This bus provides a high bandwidth interface between the element that are involved inthe majority of the transfers. Also located on the high performance bus is a high bridge to lower bandwidth APB, where most of the peripherals devices in the system are located (see fig.2) [3]. AMBA APB provides the basic peripheral microcell communication infrastructure as a secondary bus from higher bandwidth pipelined main system bus such peripherals typically.

- Have interfaces with memory mapped registers.
- Have no high bandwidth interfaces
- Are accessed under programme control.

The external memory interface is mainly the application specific and may only the narrow data path, but may also supports a test access mode which allow the internal AMBA AHB, ASB and APB modules to be tested in isolation with system-independent test sets.

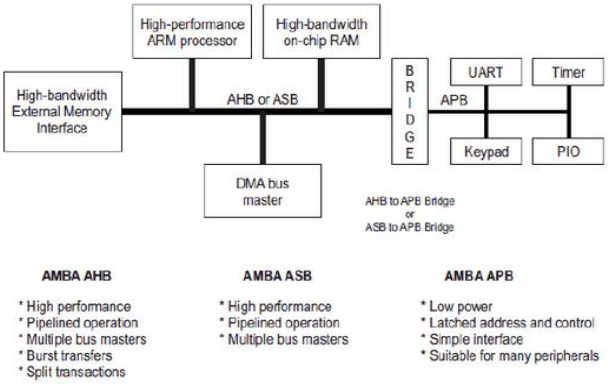

Fig.2 A Typical AMBA AHB BASED System

G. Multi-channel AHB:

The multi-layer AHB busmatrix is an interconnection scheme based on the AMBA AHB protocol which enables parallel access path between multiple masters and slave in the system. This is achieved by using more complex interconnects matrix and gives the benefits of both increased overall bus bandwidth and a more flexible system structures. The multilayer advanced high-performance bus (ML-AHB) busmatrix uses the slave-side arbitration. request and grant signals in Slave-side arbitration is different from master-side signals since, before the master first simply starts a burst transaction and waits for the slave response for processing the forward transfer. Therefore, the unit of arbitration can be a transaction or a transfer. The transaction based arbitration and the transfer based arbiter switches the data transfer based on a single transfer. However, the AHB busmatrix of ARM presents only transfer based arbitration scheme, i.e. transfer based fixed priority and round robin arbitration schemes.

This limit of the arbitration scheme may lead to degradation of the system performance because the arbitration scheme is usually depend on the application requirement, recent application are likewise more becoming complicated. By implementing an efficient

arbitration scheme, the system can be tuned to better suit application. On high performance on chip bus, several studies regarding arbitration scheme has been proposed, such as table look-up based cross bar arbitration, two level TDM, token ring arbitration, bus arbitration alogorithm.

However, these approaches employ master-side arbitration. Therfore, they can only control priority policy and also present some limitations when handling the transfer based arbitration uses centralized arbiter. AMBA advanced high performance bus (AHB supports the following features.

- High performance.
- Burst transfer.
- Split transactions.
- Single edge clock operation.
- SEQ, NONSEQ, IDLE, BUSY transfer types.
- Programmable number of idle cycles.
- Large data bus width 32, 64, 128, 256 bit wide.
- Address Decoding.

II. WORKING:

In this project, we are going to implement interconnect matrix for multichannel AMBA-AHB using multiple arbitration technique. The design of arbiter for flexible busmatrix supports the priority policy as multiple arbitration techniques. The block of the multichannel AMBA-AHB includes arbiter, master, Slave, decoder. Fig. 3 [7] shows the block diagram of the basic Multi-channel concepts. In this we are employing the central arbitration scheme.

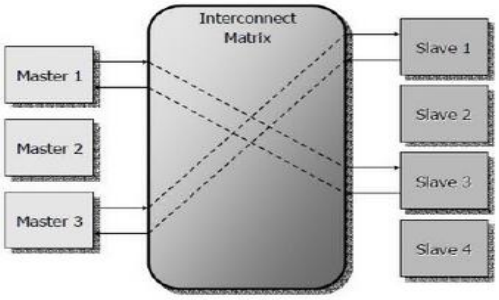

Fig. 3. Block Diagram Of Basic Multi-channel concepts [7].

A master is able to initiate read and write information by providing address and the control information. At one time only one master can access the bus. An ahb bus master has the most complex bus interface in an AMBA system. Typically, an AMBA AHB system designer would used predesigned bus master and therefore would not need to be consider with the detail of the busmaster.

The slave then determines how the transfer should progress After master has started a transfer. Whenever the slave is accessed it must provide a response which indicates the status of the transfer.

The AHB decoder is used to decode the address of each transfer and provide the select signal for slave that is involved in the transfer. The central address decoder is used to provide a signal 'HSELx' for each slave on the bus. The Slave must only sample the address and control signals and first the HSELx is putted then the HREADY is make high, indicating that the current transfer is completing.

The amba Ahb bus protocol is designed with central multiplexer interconnection scheme.

Using this scheme all bus master drive out the address and control signal indicating the transfer, they wish to perform and arbiter determines which master has its address and the control signal routed to the entire slave. Before which initially the master who needs to perform operation should give the request signal to the arbiter and the arbiter will give the grant signal to the master for the further proceedings. Similarly decoder is used to select the slave which has to be active during the operation based on the address given by the master. The central decoder is also required to control the read data and response signal multiplexor, which selects appropriate signal from the slave, which makes the read and write operation smoothly.

Fig 4. Shows the AMBA AHB block diagram.

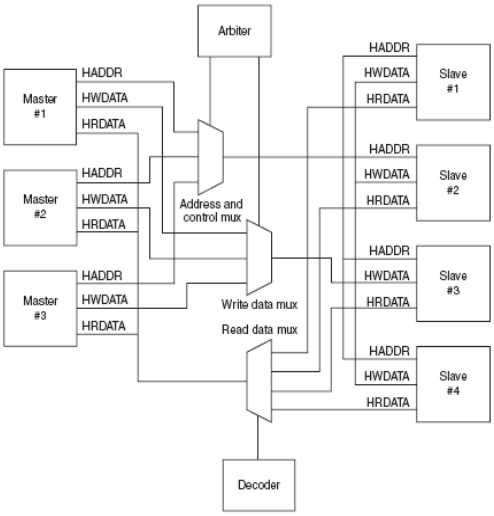

Fig.4. AMBA AHB Block Diagram

III. METHODOLOGY:

In this, we are designing and implementing interconnect matrix for multi-channel AMBA ahb bus with multiple arbitration techniques using xillinx simulator and implementing using FPGA by using vhdl language. In this we are using FPGA because it provides following advantages.

- Flexibility
- Low power consumption

- Short duration required to design
- High density
- Parallel Processing
- Can develop the complex circuit with simple logic with accurate timing.

IV. CONCLUSION:

Thus, we are going to implement the interconnect matrix for multi-channel AMBA-AHB bus using multiple arbitration techniques. The multi- channel AMBA AHB busmatrix which provides interconnection scheme between multiples masters and slave by using AMBA AHB protocol. This can be achieved by using a more complex interconnection matrix and gives the benefit of both increased overall bus bandwidth and a more flexible system structure. In particular, the multichannel-AHB busmatrix uses central arbitration. The designs of a central arbiter for interconnect busmatrix supports the priority policy as multiple arbitrations priority policy.

V. RESULTS:

In round robin arbitrations mechanism , the accesses to the Bus is given to the masters as per there sequence. Round robin arbiter gives 1st priority to the 1st master , 2nd to the 2nd masters and so on. In dynamic arbitration mechanism, the master who gets the accesses to the bus, its priority always reduces by 1, if same master has highest priority after reducing its priority then that master again get the accesses of the bus. But, in this case the less priority masters does not get chance to access the bus in this case dead locks condition arises, which is removed by new arbiter. New arbiter is the combination of round robin and dynamic arbiter.

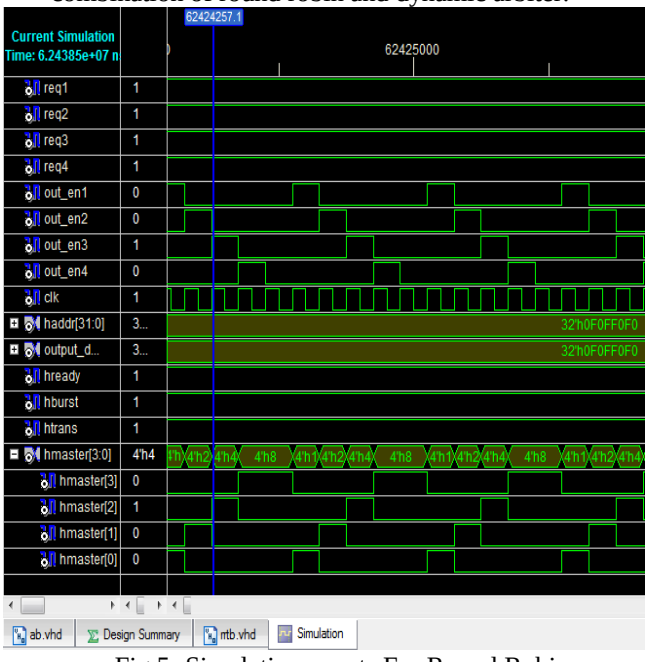

Fig 5- Simulation resuts For Round Robin

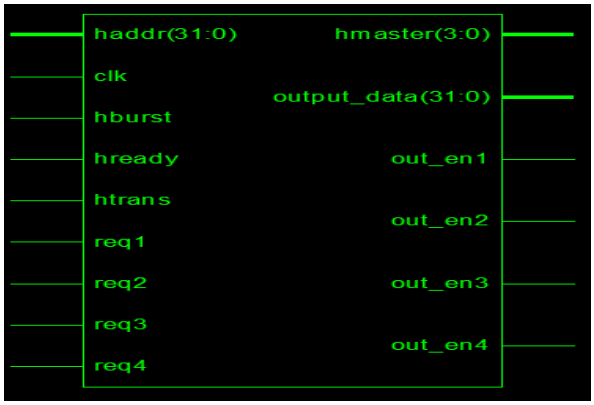

Fig 6- RTL view for Round Robin

Fig 6- Design summery for Round Robin.

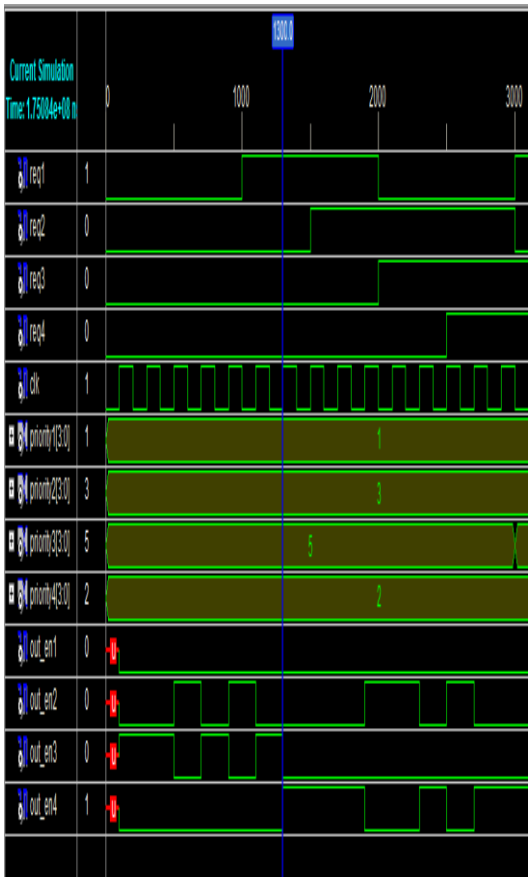

Fig 7- Simulation resuts For Dynamic Arbiter

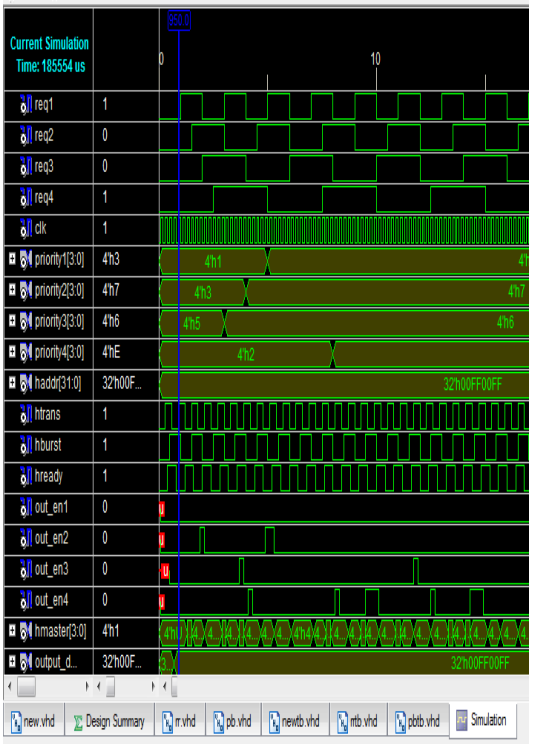

Fig 8- Simulation resuts For New Arbiter

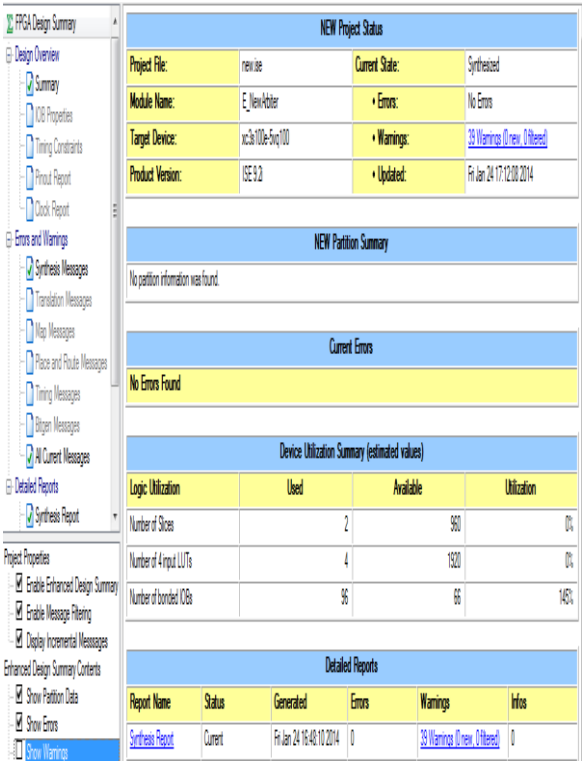

Fig 9- Design summery for New Arbiter

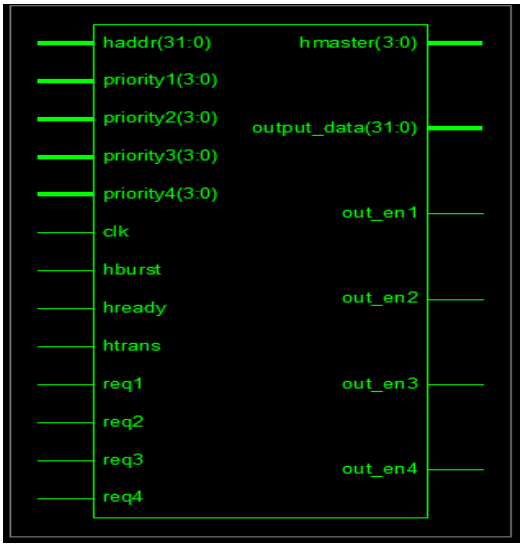

Fig 10- RTL view for New Arbiter

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