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# Design of Sequential Circuit using Low Power Adiabatic Complementary Pass Transistor Logic

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**ABSTRACT:**
Adiabatic logic style is Proving to be an attractive solution for low power digital design. The paper investigates low – power characteristics of complementary pass -transistor logic (CPL) circuits using AC power supply. The two-phase power-clock scheme is more suitable for the design of flip-flops and sequential circuits because it uses fewer transistors. The Adiabatic flip-flop have large energy saving over wide range of frequencies. In this paper, we use 180nm Tanner model Technology. Also analyzing the power dissipation of another adiabatic logic family i.e. CAL and comparing it with adiabatic CPL methodology.
**Keywords:** Adiabatic CPL, Flip-Flops, Power Clock, Low Power , CAL.

## I . INTRODUCTION

Adiabatic circuits are low power circuitry which use "reversible logic" to conserve energy. The word " adiabatic" comes from a Greek word that describe thermodynamic processes which exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In ideal adiabatic logic, each charge could be recycled (reused) an infinite number of times. So that a significant power dissipation reduction would be possible. In real-time computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. There are classical approaches to reduce the dynamic power such as reducing supply voltage, decreasing physical capacitance and reducing switching activity. Adiabatic logic works on the concept of switching activities which reduces the power by giving stored energy back to the supply.

There are several principles that are shared by all of these low - power adiabatic systems. These include only turning switches on when there is no potential difference across them, only turning switches off when no current is flowing through them, and using a power supply that is capable of recovering or recycling energy in the form of electric charge. To achieve this, in general, the power supplies of adiabatic logic circuits have used constant current charging , in contrast to more traditional non-adiabatic systems that have generally used constant voltage charging from a fixed-voltage power supply .The power supplies of adiabatic logic circuits have also used circuit elements capable of storing energy. This is often done using inductors which store the energy by converting it to magnetic flux, or using capacitors, which can directly store electric charge. There are a number of synonyms that have been used by other authors to refer to adiabatic logic type systems, these include: "Charge recovery logic" ,"Charge recycling logic", "Clock-powered logic", "Energy recovery logic" and "Energy recycling logic" . Because of the reversibility requirements for a system to be fully adiabatic, most of these synonyms actually refer to, and can be used inter-changeably, to describe quasi-adiabatic systems.

## II. CLASSIFICATION

Adiabatic logics are of two main types. They are:

- Partially adiabatic logic.
- Fully adiabatic logic.

Now ,Partially adiabatic logic is a logic having non-adiabatic loss present i.e. there is non -zero $V_{DS}$ across transistor when it is being turned ON. It doesn't depend upon frequency. It can be further classified as:

- Efficient charge recovery logic (ECRL).
- 2N-2N 2P logic.
- Positive feedback adiabatic logic (PFAL).
- NMOS energy recovery logic (NERL).
- Clocked adiabatic logic (CAL).

Fully adiabatic logic is a logic having non -adiabatic loss absent . It depends upon frequency. It can be classified as:

- Pass transistor adiabatic logic.
- Split rail charge recovery logic. (SCRL).

## III. ADIABATIC CPL

### *A. CPL inverter using DC power supply*

It is composed of two main parts: the evaluation logic block and the load driven circuit. The evaluation logic block consists of four NMOS transistors with CPL configuration, which functions as pull-down and pull-up devices. The load driven circuit consists of two CMOS output inverters that obtain fully-swing and drive the output loads. Since the output high level of CPL evaluation logic block is $V_{DD}$-$V_{TN}$ ($V_{TN}$ is the threshold voltage of the NMOS transistors), two small pull-up PMOS transistors are usually introduced to achieve the level restoring and reduce short circuit power consumption of the output inverters .

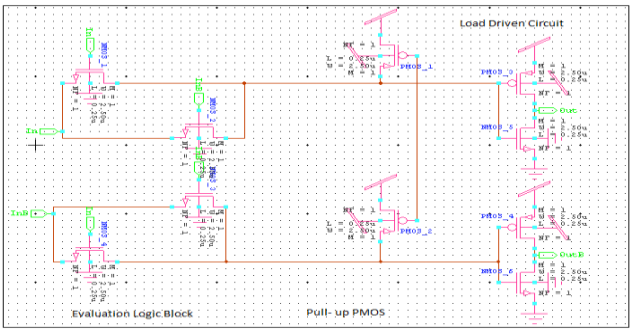


Fig 1(a). CPL Buffer using DC Power Supply

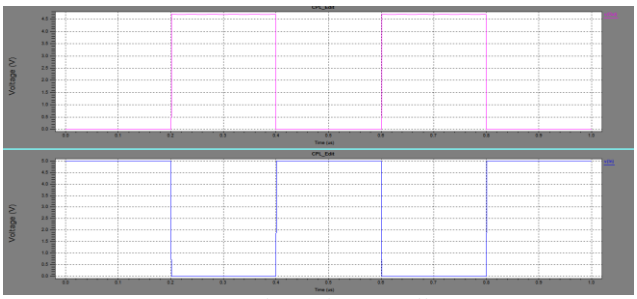

Fig 1(b).Simulation Waveform of CPL Buffer using DC Power Supply

### *B. Adiabatic CPL using AC Power Supply*

Operation of Adiabatic circuit is divided into three phases. They are :

1) Evaluation phase: Load driven circuit is charged during this phase i.e. Power Clock rises from 0 to $V_{DD}$.

2) Hold Phase: Output voltage are stable here and can be used by next logic block .

3) Recovery Phase**:** The load circuit is discharged during this phase as Power Clock ramps down to 0 value.

Power Clock Supply has two fold role and used as Power Supply Signal and Clock Signal. And used to avoid need of two separate sources. During the time interval $T_1$, the voltage of the input INb is low and the input IN goes high. Therefore, NI and N3 are turned on. As the input IN goes up, the node X is charged to about $V_{DD}$- $V_{TN}$ , while the node Yis clamped to ground. During the interval $T_2$, as the input IN falls, NI and N2 are turned off .Thus, the voltage of the node X will keep its state because the node X is isolated. During $T_3$, as the power-clock phi (φ) goes up, the node X are bootstrapped to a higher level than $V_{DD}$-$V_{TN}$ due to the gate to- channel capacitance of the transistor N5. Therefore, as the clock phi (φ) rises, the output OUT is charged through the bootstrapped N5 without non-adiabatic loss, and fully-swing is obtained. At the same time, the output OUTb is clamped to ground because the N8 is turned ON. During $T_4$, as the power-clock phi (φ) falls from $V_{DD}$ to ground, the charge on the output OUT is recovered through the transistor N5 in the adiabatic manner.

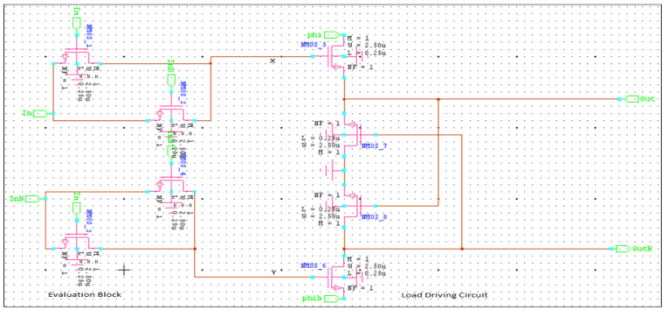


Fig 2(a). CPL Buffer using AC Power Supply

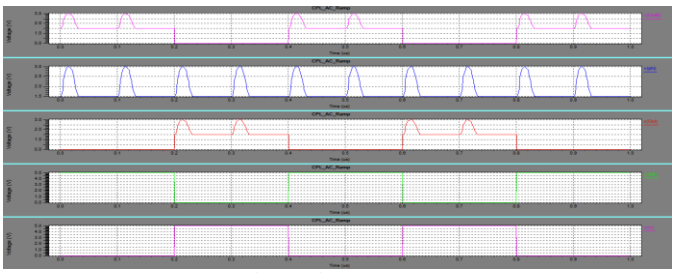

Fig 2(b). Simulation Waveform of Adiabatic CPL using AC Power Supply .

It should be pointed out that the bootstrapped voltage of the node X must be high enough to turn on the transistor N5 during the of T3 and T4. Therefore, the full-swing condition is that the voltage of the node X (or Y) must be bootstrapped to at least one threshold voltage above $V_{DD}$ from $V_{DD}$-$V_{TN}$ when the voltage of the power-clock φ is the peak voltage $V_{DD}$ :

$$V_{DD} - V_{TN} + \Delta V \geq V_{DD} + V_{TN} \qquad -----(1)$$

Therefore , $\Delta V \geq 2V_{TN}$ -------(2)

## IV. ADIABATIC SEQUENTIAL CIRCUIT

The adiabatic flip-flop can be structured using a cascaded logic chain. In this paper, we design a reversible JK Flip-Flop. From the observation, we

conclude that when J and K is connected with complimentary value of D input , we get the Delay(D) Flip-Flop. D Flip- Flop generates a delayed version of input signal synchronised with Power Clock.

$$D = J\bar{Q}_{bar} + K_{bar}Q.$$

Average Power of D Flip-Flop = 1.36e^(-6) = 1.362 µW. By observing the formula $JQ_{bar} + K_{bar}Q$ we see that it is a 2:1 mux with inputs as J and K and select line as Q. Similarly we design a reversible Toggle Flip-Flop when J and K nodes are tied together. Average Power of T Flip-Flop = 2.9826e^(-4) = 0.2986 mW.

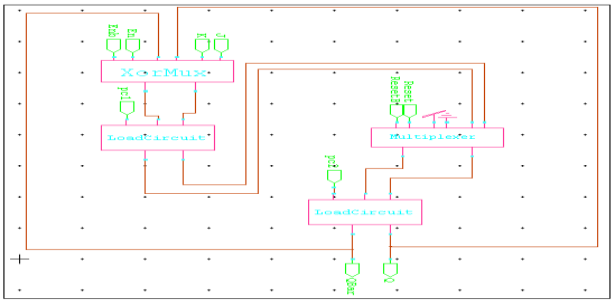


Fig 3. J-K Flip-Flop using Adiabatic CPL

PC 1 and PC 2 are 180 degree out of phase . On PC 1 system is charged and on PC 2 , system is discharged to give output. 2:1 MUX having select line as reset is used to control the signal i.e. if reset is 1 then output is disable and if reset is zero ,input is given to output.Load circuit is used to charge and discharge the output based on PC. If PC is enable then output is equal to input else output is zero.

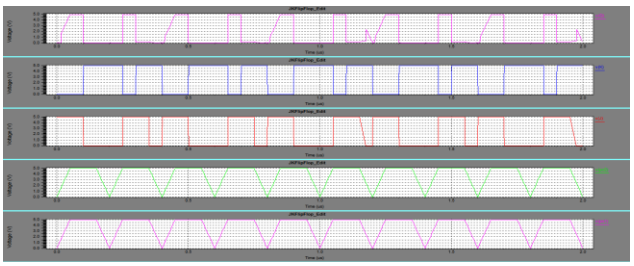

Fig 3(a). Simulation Waveform of J-K Flip- Flop using Adiabatic CPL.

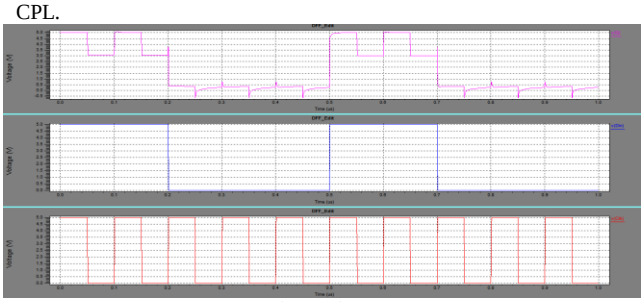

Fig 3(b). Simulation Waveform of D Flip-Flop using Adiabatic CPL.

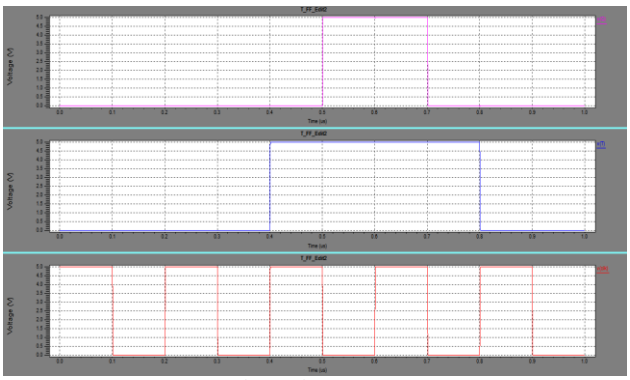

Fig 3(c). Simulation Waveform of T Flip-Flop using Adiabatic CPL.

*16 bit BCD up- Counter*

An adiabatic BCD code up-counter structure is the same as the conventional CMOS Implementation based on T flip-flops (Qo, Ql, Q2, and Q3) with reset terminals . The Reset signal is generated by using AND gates with Qo and Q3. In order to synchronize the signals between the stages, the signals (Qo', Ql, and Q2') from the output of the first buffer of the T flip-flops are used as inputs to the left two AND logic gates, instead of the usual output signals (Qo, Ql, and Q2).

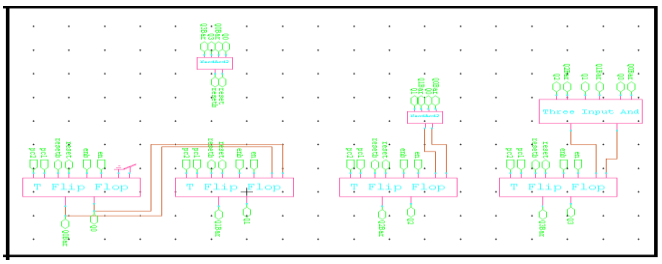


Fig 4(a).16Bit BCD Up-Counter using Adiabatic CPL

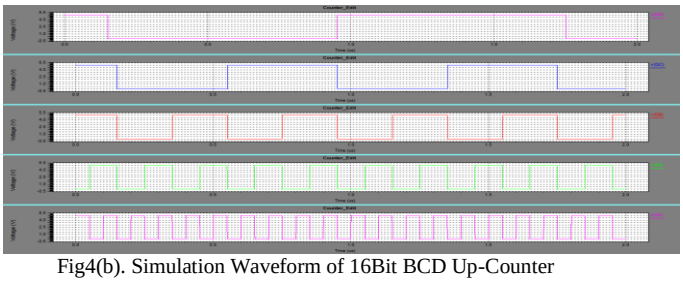

Fig4(b). Simulation Waveform of 16Bit BCD Up-Counter

## V. CLOCKED ADIABATIC LOGIC CIRCUIT

CAL buffer consisting of two part circuits

- logic evaluation
- energy recovery circuits .

The logic evaluation circuits consist of the two NMOS transistors (N1, N2). *CX* is an auxiliary clock signal, and it enables the evaluation NMOS transistors (N1, N2) by

turning on the NMOS transistors (N5, N6). The energy recovery circuit consists of the two cross-coupled PMOS
transistors (PI, P2). The power-clock *(clk)* charges the output *(OUT* or *OUTb)* in evaluation phase through PI and P2. In recovery phase, the energy of the output nodes is recovered to *clk* through PI and P2. The clamp transistors (N3 and N4) ensure stable operation by preventing from floating of the
output nodes. Buffer gives output equal to input when power clock equal to 1.

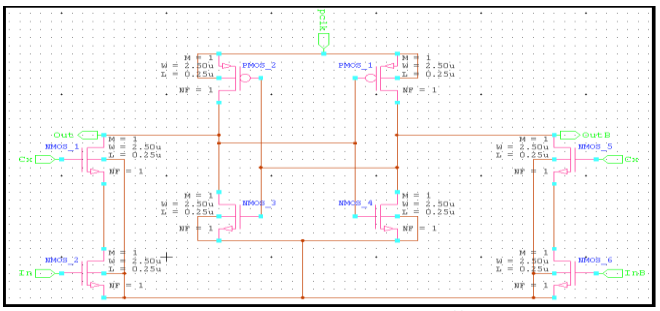

Fig 5(a) .CAL Buffer

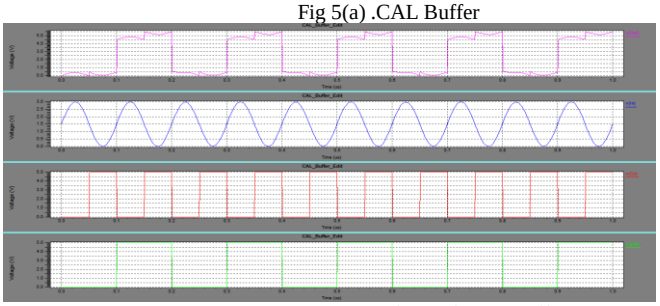

Fig 5(b). Simulation Waveform of CAL Buffer

*CAL D flip-flop*

In D flip-flop output at the end of clock pulse equals the input before the clock pulse. Output equal to input when clock is1. This is equivalent to say that input data appear at output at the end of clock pulse. Thus , transfer of data from input to output is delayed and hence called Delayed or Dflip-flop. CAL D flip-flop is implemented by cascading two buffer.

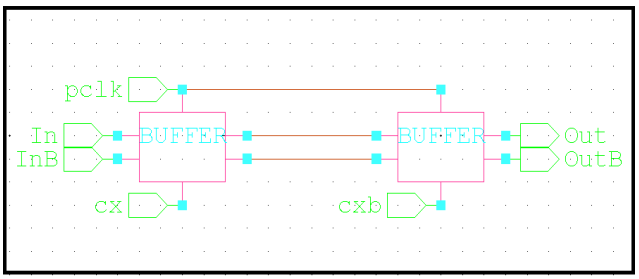


Fig 6(a ). CAL D flip flop

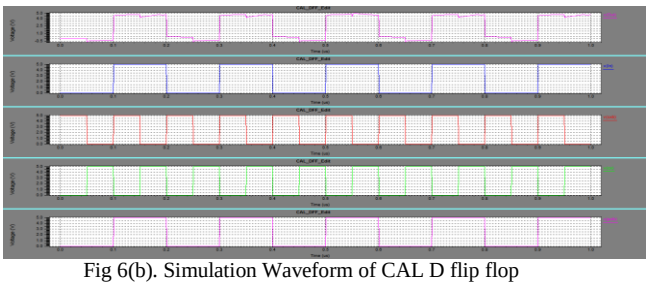

Fig 6(b). Simulation Waveform of CAL D flip flop

*CAL T flip-flop*

CAL T flip-flop are realized by using the XOR and Buffer . When T =1, CLK=1,Output is toggle i.e, output is not equal to previous output . When T=0,CLK=1,Output is equal to last output.

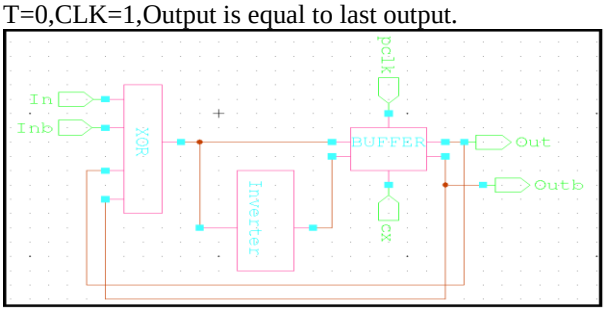


Fig 7(a). Adiabatic T Flip-Flop using CAL

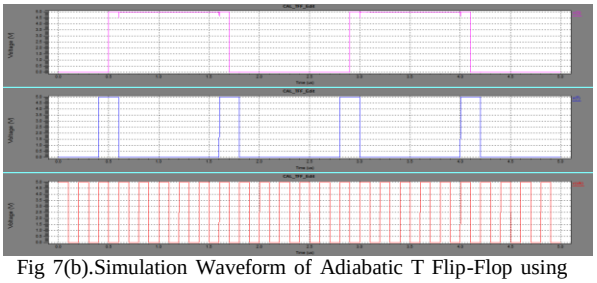

Fig 7(b).Simulation Waveform of Adiabatic T Flip-Flop using CAL

*CAL Counter*

Counter are made to show the application of flip-flop. Digital counter are often needed to count events. Clocked adiabatic logic counter structure is same as the conventional CMOS implementation based on *T* flip-flops (*Q*0, *Q*1, *Q*2,and *Q*3) with reset terminals. The reset signal is generated by using AND gates with *q*0 and *q*3. In order to synchronize the signals between the CAL stages, the signals (*q*0, *q*1, and *q*2) from the output of the first buffer chain of the *T* flip-flops are used as inputs to the upper two AND logic gates. The auxiliary clocks *CX* and *CXb*, which should be in alternate logic stages. For normal counting operation , its clock is maintained at 1. The circuit reset after counting 1111 as the circuit with n flip-flop has 2^n possible states.

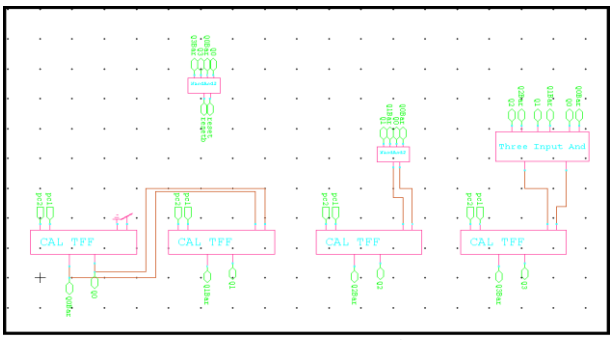


Fig 8(a) .16bit BCD Up-Counter of CAL

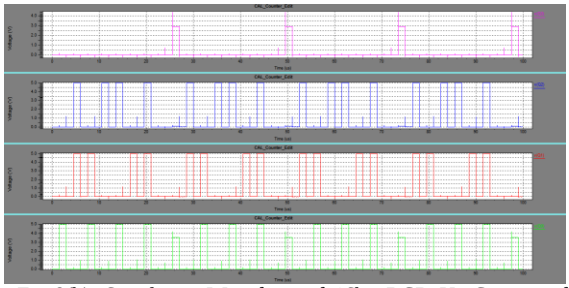

Fig 8(b). Simulation Waveform of 16bit BCD Up-Counter of CAL

**Comparison of Power dissipation between CAL and CPL**

| Parameter | CAL in terms of Power (Watt) | CPL in terms of Power (Watt) |
|---|---|---|
| BUFFER | 5e-12 (5 pW) | 5e-6 (5 uW) |
| D FLIP-FLOP | 5e-12 (5 pW) | 2e-4 (0.2 uW) |
| T FLIP-FLOP | 5e-5 (0.5 uW) | 6e-5 (0.6 uW) |
| COUNTER | 5e-7 (0.5 uW) | 9e-4 (0.9 uW) |

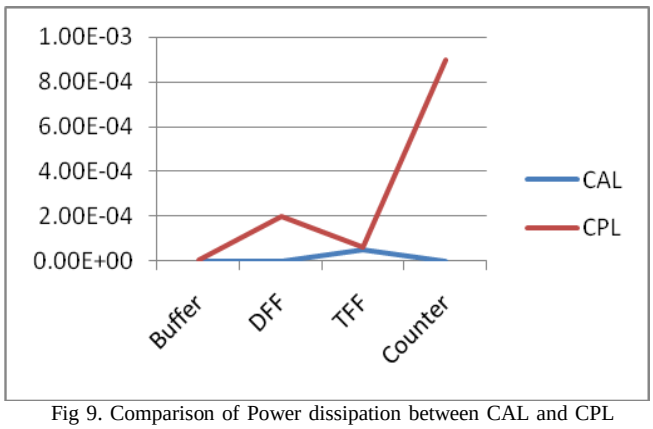


Fig 9. Comparison of Power dissipation between CAL and CPL for parameters shown in table.

## VI. CONCLUSION

From the above analysis , it is justified that CAL gives better performance with respect to CPL as CPL dissipates more power than CAL. In order to reduce more power of CPL and CAL Counter Power gating scheme has to be implemented so that we can reduce power even in idle state and compare it with and without power gating CPL and CAL Counter.

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