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Line-Voltage-Regulators Optimization in ElectricPowerQuality

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A B S T R A C T

The rapid expansion of distributed energy resources in the low voltage grid causes voltage limit violations, especially in rural areas with little electric load. To solve this issue without costly grid reinforcement, one approach is the use of smart devices such as line-voltage-regulators. However, the majority of these devices carry out stepped voltage adjustments, which cause a negative effect on the dynamic voltage characteristic. For this reason, this paper deals with a novel line-voltage-regulator and its power quality optimized control. The novel setup enables a continuous voltage regulation in a robust way by using variable inductors. The control design focuses on mitigating side-effects like harmonic distortion emission and increased grid impedance. Finally, a laboratory analysis evaluates the novel line-voltage regulator in comparison to a stepped one with regard to powerquality.

Keywords: Line-voltage-regulation Low voltage grid Power quality Variable inductor Voltage control

INTRODUCTION

The rapid expansion of distributed energy resources (DER) in the low voltage grid and the resulting reverse power flow cause voltage limit violations [8,22], especially in rural grids with little electric load. To keep the voltage within the limits specified by EN50160 [1], but not toslowdown this expansion, the low voltagegridneedstobeimproved. Grid reinforcements can be partly avoided using innovative devices, such as on-load tap changers and line-voltage-regulators (LVR) [18]. These devices control the line voltage directly without changing the reactive power flow. The majority of these devices carry out stepped voltage adjustments, such as those presented in [6] and [16]. However, this type of adjustments causes rapid voltage changes and thus leadsto flicker effects [5]. Further negative effects due to rapid voltage changes aremoto rbraking/ acceleration, malfunctionofcontrolsystemsacting on the voltage angle and impairment of electronic equipment [19]. Alternatively, LVRs can be based on power electronics to enable a continuous voltage adjustment [3,4,7]. These devices can be quite powerfulastheyhaveahighcontrolspeedandcancompensat evarious voltage issues. However, these devices usually emit high frequency harmonics [7]. Furthermore, power electronics have a relatively high failure rate [23]. Therefore, more maintenance and repairs have to beexpected,whichleadstohighoperatingcosts.

In this context, the InLiNe project analyzed the use of variable in- ductors(VI) asanovel techniquefor LVRs.TheVItechniquecanmerge a continuous voltage adjustment with a robust, cost effective design by avoiding power electronics. However, in a naive design thedevice

increases the grid impedance and emits harmonic distortions. To miti- gate these effects an improved setup is constructed in laboratory [11]. Building on the constructed setup, this paper focuses on a control ap- proach that provides a power quality (PQ) optimized operation. The control approach enablesa continuousvoltageregulationandmitigates the side effects of the novel LVR. To identify a suitable controller, a detailed model is constructed that considers the nonlinear behavior ofthe setup. A laboratory analysis validates the control system and eval- uates remaining side effects with regard to PQ. Moreover, the results are compared to a measured, stepped voltage-regulation to illustrate the advantages of the continuousvoltage-regulation.

All in all, this paper provides the setup and the controller devel- opment for a novel, PQ optimized LVR, which can be an effective ap- plication for the

distribution grid. The presented approaches for modelling and controlling can be adapted for other applications based on variable inductors as these applications are typically characterized by a nonlinear behavior due to the changing inductance. The laboratory analysis provides a detailed overview of the PQ effects on the grid and can be utilized to evaluate the use of an LVR for a specific grid section with voltage limit violations.

1. Setup andfunctionality

To understand the general concept of an LVR based on VIs, one needs to consider first its elementary structure. An LVR based on VIs is composed of a series transformer, whose primary winding is part of an inductive voltage divider, and a VI, which forms the second part of the

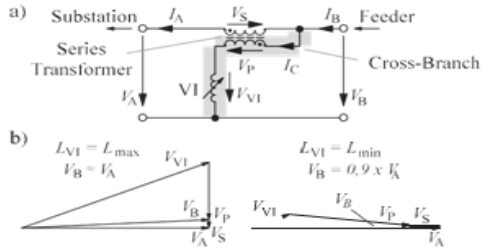


Fig. 1. Elementary design in voltage-reduction mode: a) Single-phase circuit b) Phasor diagrams for twoVI control states.

voltage divider. The inductance of the VI can be reduced, which increases the voltageattheprimarywindingoftheseriestransformerand its effect on the output line voltage. Depending on the transformer winding direction, voltage-boost mode or voltage reduction mode can be selected. Fig. 1a) shows a simplified single-phase circuit in voltage- reduction modethatcanbeusedtocompensateovervoltagescausedby DER. Fig. 1b) shows the corresponding phasor diagrams for two VI control states. The voltages by different inductivities are depicted qualitatively. The presented elementary design is similar to the design patented in[21].

The elementary design has the main disadvantage of increasing the grid impedance in the initial state if the VI has a high inductance. This disadvantage results from dimensioning the cross-branch to prevent a power flow over the series transformer in this state. Because the initial inductance value of the VI must be chosen accordingly high, the series transformer is almost in no-load operation on the primary side. As a result, the magnetizing reactance of the series transformer has a high inductive impact on the grid impedance.

An increased grid impedance causes well-known effects such as a reduction of the short-circuit current and the interference immunity to PQ. Recent research also shows that frequency dependent grid im- pedance has a strong influence on harmonic stability of converters [10,24].

To avoid the grid impedance increase, a significant improvement is developed and published in [11]. According to this, Fig. 2shows the improvedLVRdesign.AsecondVI(VI_{Byp})isconnectedinparalleltothe series transformer. By a maximal reduction of the VI_{Byp} inductance, the series transformer is nearly

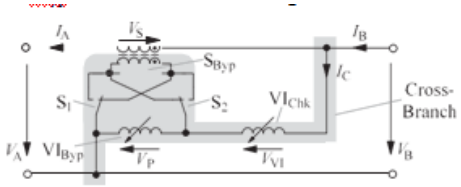


Fig. 2. Single-phase circuit of the improved LVR design [11].

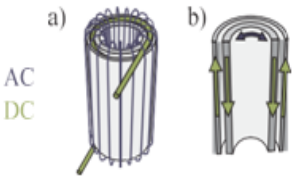


Fig. 3. VI design: a) Setup b) Magnetic flux in the core.

short-circuited. This reduction bypassesthe influence of the transformer's magnetizing reactance. To enable a continuous LVR control, a combined control of VI_{Chk} and VI_{Byp} is required.Thecontroltaskistoensurethattheseriestransformerd oesnot work in no-load operation. Yet, the impedance of the cross-branch should be still suffcient to limit the cross-current $I_C$to allow for compactcomponentsandlessgridlosses.Section3discussesthiscombined control approach in more detail. As a result, VI_{Byp} is an important tool tooptimizetheinfluenceoftheLVRonPQ.

In addition to the elements described before, Fig. 2shows three switches. The switches S_1 and S_2 enable switching from voltage-re- duction mode to voltage-boost mode by commutating the series trans- former. The switch S_{Byp} enables short-circuiting the series transformer

to separate the influence of the LVR completely from the grid. By closing S_{Byp}, the LVR is turned to standby mode without any interrup- tion in the distribution system. In this mode only the copper losses of the secondary winding occur.

Next, the setup and functionality of the used VI technique is con- sidered. In principle, a VI can be built using a variety of techniques [12]. However, to enable a continuous and robust control, the best choice is a saturable reactor. In this technique, the core of an inductoris driven into saturation by an extra DC winding. The saturation reduces the permeability of the material. As a result, the inductance of the AC winding decreases proportionally. In a naive design, the DC flux only generatesasaturationeffectinoneofthetwoAChalfwaves. Thisleads to asymmetries in the AC signals. Furthermore, an unwanted voltage transfer from the AC to the DC winding occurs. To mitigate these ef- fects,avarietyofdi□erentdesignsexist[17].

The VI design utilized for the LVR presented here is patented in [9]and is illustrated in Fig. 3. This VI consists of an AC and a DC winding that are wound on two toroidal cores (Fig. 3a)). The two windings and the corresponding fluxes are orthogonal to each other (Fig. 3b)). Thus, the DC and AC windings are decoupled, and the saturation a□ects the AC signals symmetrically.

2. Combined controlapproach

In the following, a combined open-loop control of VI_{Chk} and VI_{Byp} is developed to enable a PQ optimized operation of the LVR. The com- bined control approach considers the minimization of the additional grid impedance while providing a continuous voltage regulation. In addition, the approach takes into account the reduction of power con- sumption, by limiting the cross-current, and the mitigation of voltage disturbances generated by the saturation effects in the VIs. For this purpose, characteristic maps are determined with measurments. Each map takes into account one characteristic quantity depending on the control states of the VIs. Based on these maps, the best control path is selected.

The characteristic quantities as voltage variation ΔV, cross-current $I_C$and output voltage distortions THD_V are measured during normal grid operation. Thereby, the voltage variation ΔV corresponds to the difference between $V_{B,RMS}$and $V_{A,RMS}$. By short-circuiting the LVR output, the characteristic quantity of the additional grid impedance $Z_{LVR,grid}$is determined.

Fig. 4 a) - d) shows the characteristic maps of the LVR in voltage- reduction mode by an inductive line-current. For voltage-boost mode, the maps are nearly similar, only ΔV changes polarity.

To understand the LVR behavior depicted in these maps, one needs to remember that the voltage regulation of the LVR works by varying the voltage divider ratio between VI_{Chk} and the series transformer. A high DC control-current in VI_{Chk} reduces its inductance and leads to an increased voltage variation ΔV at the LVR. VI_{Byp}, on the contrary, by- passes the impact of the series transformer. As a result, a high DC control-current in the VI_{Byp} reduces the LVR effects on the line.

Consequently, the initial operation point is achieved by a control state of VI_{Chk} at 0% (of $I_{DC,max}$) and VI_{Byp} at 100%. At this point, the LVR has nearly no effect on the line, and the variation of the output voltage is nearly zero. In contrast, the control state of VI_{Chk} at 100% and VI_{Byp} at 0% causes the maximal voltage variation by the LVR(see

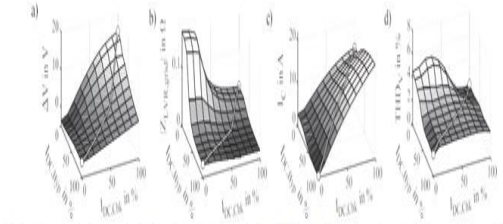


Fig. 4. Characteristic maps including the selected control path for the following characteristic quantities: a) Output voltage variation $\Delta V = V_{B,RMS} - V_{A,RMS}$ b) Additional grid impedance $Z_{LVR,grid}$ c) Cross-current I_C d) Output voltage distortion THD_V.

Fig. 4a)).

For the control path, the control states of both VIs around 0% have to be avoided to minimize the impact of the magnetizing reactance of theseriestransformeronthegrid(seeFig.4b)).Inaddition,the control states of both VIs around 100% are prohibited to limit the cross-current I_C(see Fig. 4c)). For the combined control approach, the aim is to avoid the top 20% of I_C. Furthermore, the use of VI_{Byp} can reduce output voltage distortion THD_V caused by the saturation effects in the VI cores (see Fig. 4d)). Again, the top 20% of THD_V should beavoided.

Building on these constraints specified above, a control path is es- tablished and displayed in the characteristics maps. For the DC control current, the following functional relationship is obtained by a max-imum control current of 1 A.

$$\begin{cases} I_{DC,Chk} = 1\,\text{A} & \text{for } 0\,\text{A} < I_{DC,Chk} \le \frac{1}{3}\,\text{A} \\ I_{DC,Chk} = -\frac{2}{3}\,\text{A} & \text{for } \frac{2}{3}\,\text{A} < I_{DC,Chk} \le \frac{3}{3}\,\text{A} \end{cases} \quad (1)$$

Due to the selected control path, the additional grid impedance is lower than 0.04 Ω and the cross-current $I_C$is limited to 15 A. According to

similar control range (7 % of the line voltage according to

3. Modelling

In addition to the control path developed in the previoussection,aclosed-loop control is required to regulate automatically theoutput voltageof the LVR. Toidentifyasuitablecontroller,firstadetailedmodelisconstructedthatconsidersthenonlinearbehaviorofthesetup.

The modelling is divided into three parts. First, the LVR circuit and its mathematical relations are determined. The AC impedances of the two VIs are currentineachVIresultsfromaDCvoltage,dependingontheelectrical characteristics of the DC winding, which are modeled in the thirdpart.

linear components. The transfer behavior of the series transformer ismodelled by using an ideal transformer. In addition, a parallel im- pedance $Z_M$represents the magnetizing reactance and the core losses of the series transformer. For simplicity, its winding joule losses and its leakage reactances' are ignored since they have negligible influence on the LVR behavior. Each VI is represented by an impedance with a variable value. The impedance is varied by the core saturation caused by the DC flux. Since the DC currents generate this flux, the impedance valuescanbeexpressedasafunctionoftheDCcurrentsas$Z_{Chk}(I_{DC})$and $Z_{Byp}(I_{DC})$.

Based on this equivalent circuit, (2) is obtained for the input voltage

$V_A$according to Kirchhoff's laws:

$$V_A = V_S + V_P + V_{VI} = \frac{1}{a} \cdot V_P + V_P + Z_{Chk}(I_{DC}) \cdot I_C \quad (2)$$

Here, the transformer voltage V_S at secondary side ... voltage, ...

voltage at VI_{Chk} and is also expressed by the cross-current $I_C$and the variable impedance $Z_{Chk}(I_{DC})$.

The voltage at the series transformer depends on the input current

I_A as well as the cross-current $I_C$and can be calculated according to the superposition principle in (3):

$$V_P = V_{P,IC} - a \cdot V_{S,IA} = Z_P(I_{DC}) \cdot I_C - \frac{a}{a^2} Z_P(I_{DC}) \cdot I_A \quad (3)$$

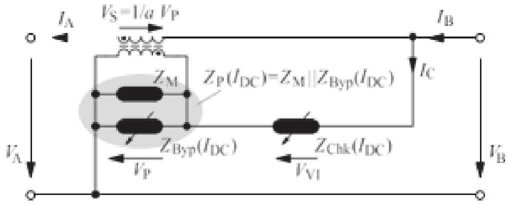
required as parameters in the LVR circuit and are modeled inthesecondpartbytheirdependencytotheDCcurrents.TheDC

The currents $I_A$and $I_C$generate two fluxes in opposite directions in the core. Each flux would inject a di erent voltage, $V_{P,IC}$and $V_{S,IA}$, at the transformer windings. The total voltage results from to the super- position of these two voltages. $Z_P(I_{DC})$ is the total impedance of $Z_{Byp}(I_{DC})$ and Z_M. It is referred to the primary side. To calculate the voltage drop caused by I_A, the impedance

An overview of the entire model is given in Fig. 9 in Section 5.

LVRCircuit

Fig. 5 shows the equivalent circuit of the LVR in voltage reduction mode. In this circuit, the series transformer and the VIs are modelled as



needs to be referred to the secondary side. However, the resulting voltage $V_{S,IA}$must be referred back to the primary side to get the total voltage for this side.

Inserting (3) in (2) and converting to I_C yields (4):

$$I_C = \frac{V_A + \frac{a+1}{a^2} Z_P(I_{DC}) \cdot I_A}{\frac{a+1}{a} \cdot Z_P(I_{DC}) + Z_{Chk}(I_{DC})} \quad (4)$$

The output voltage $V_B$corresponds to (5):

$$V_B = V_P + V_{VI} = Z_P(I_{DC}) \cdot I_C - \frac{1}{a} \cdot Z_P(I_{DC}) \cdot I_A + Z_{Chk}(I_{DC}) \cdot I_C \quad (5)$$

Substituting $I_C$with (4) yields the required relation:

$$V_B = \ldots \cdot Z_P(I_{DC}) + Z_{Chk}(I_{DC}) \quad (6)$$

It follows from (6)that $V_B$can be controlled by varying the VI im- pedances.However,thereisnolinearrelation.Additionally, $V_B$depends on input voltage $V_A$and on inputcurrent I_A.

The analogous procedure can be used to find the system equation for the voltage boost mode resulting in (7). The difference occurs be- cause $V_S$has reversed polarity.

V_B = Z (I)Hm

1

ZP) /

VIModel:ACIMPED ANCE

For modelling the VI impedances, a black box model is derived by measurements. The purpose is to model the VI impedances as a linear component, which depends on the DC current.

It should be noted that modelling the VI impedances with a linear component is a simplification. Due to saturation effects in the VI core, the VI impedance doesn't behave linearly in every control state. Linearity exists only in an unsaturated core in the initial state and in a completely saturated core in the maximal reduction state. For the LVR, this means that voltages and currents in the cross-branch are distorted especially in the medium operating range. Here, the third, fifth and seventh harmonic occur in particular. However, the line voltage is hardly distorted since only a fraction of the distortions is added to the line voltage by the series transformer. Since only the relation between the output voltage $V_B$and the DC current is important for the control system design, it is acceptable to neglect the distortions in the cross- branch and to describe the VI impedances only with their total im- pedances. These total impedances can be calculated by the RMS quantities of measured voltages and currents.

Forthispurpose,theLVRisdrivenintovariouscontrolstate sbased on the combined control path from Section 3. Meanwhile, the cross- branch voltages and currentsaremeasured.Forthemeasurement,the idling, there is no affecting the voltage at the series

(3)).

Based on these measurements, characteristic curves are determined

6b)thetotalimpedanceZ isconsidered(Z(I)= for the VI impedances, which are shown in Fig. 6a) and b). However, in

P P DC ZM

ZByp(IDC)

The depicted curves are obtained by averaging three di□erent mea- surement series that are smoothed with spline interpolation.

AccordingtothecharacteristiccurvesZ$_{Chk}$showsahighim

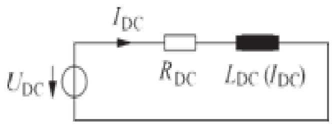


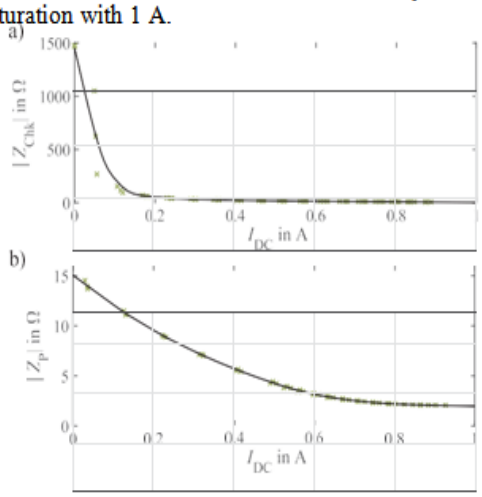
Fig. 7. Equivalent circuit of the DC winding of the VIs.

To model the impedances, the characteristic curves are saved in look-up tables. By means of the measured copper losses R (R = R = 0.11Ω Chk 0.14Ω, P), the complex impedance can be provided for themodel.

VI Model: DCcircuit

Up to this point, the LVR model just represents the gainandphaseshiftbehaviorinsteadystate.Inthefollowing,thetimebehaviorisadded to the model. For that reason, the inductivityoftheDCwindingisconsidered.IntheVIdevices, theDCwindinghasamuchhigherinductivity than the AC winding due to a higher numberofwindings.Therefore,thechargingand dischargingtimeoftheDCwindingsde- terminesthetimeresponseoftheLVR.However,thetimeresponseisnotconstantduetothevariablepermeability.Thus,theinductanceofthe DC winding also depends on the DC current itself. BecausetheDCcircuitsoftheVIsareidentical,thefollowing modelisusedforbothVIs.Fig.7demonstratestheequivalentcircuitoftheDCwinding.Inthis circuit L_{DC}models the inductance and R_{DC}represents the joule losses, which are 90 Ω according to measurements. The circuit can be de- scribed with a differential equation and after Laplace Transform the following transfer function $P_{DC}$is obtained:

Accordingtothecharacteristiccurves,Z_{Chk}showsahighim edance change at low DC currents. The reduction flattens evenmore with in- creasingDC current.The impedance rangeofZpismuchsmallerdueto theinfluence bfZM.Anopen-circuittestwiththeseriestransformer [13] determines $Z_M$with approximately $j16\ \Omega$. The common feature of both curves is that they achieve saturation with 1 A.



Due to the dependency of $L_{DC}$to I_{DC}, the numerical solution of (8) is the most reasonable way for the model. Additionally, for L_{DC} (I_{DC}), a look-up table is generated. For this purpose, step responses of $I_{DC}$are measured for different voltage intervals. Because a constant time re- sponse is assumed in each interval, time-constants τ can be established according to a first-order differential equation. For this type of di□er- ential equation, τ corresponds to the time until the step response reaches 63.2% of its final value [14].

Exemplary, Fig. 8a) shows the step response of $I_{DC}$for onemea- surement series. The point $5 \cdot \tau$ is marked for each response (99.3 % of the step response). Based on τ, the inductance L_{DC}can be calculatedfor

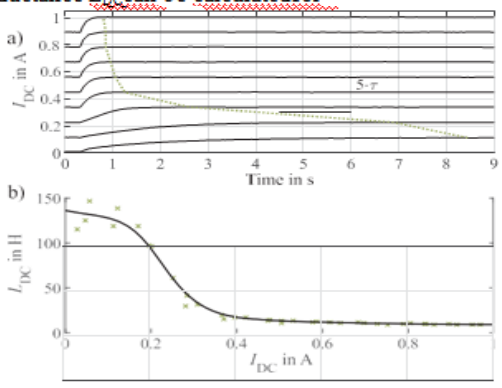


Fig. 8. Inductive behavior of the DC circuit: a) Step responsesof I_{DC}b) Characteristic curve of the DC inductivity L_{DC}.

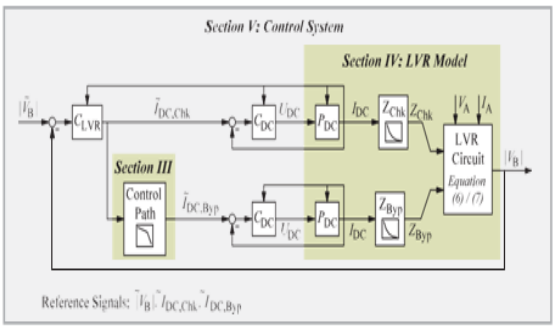


Fig. 9. Characteristic control system

each interval *i* according to(9).

$$L_{DC} = R_{DC} \cdot \tau_i \quad i \in \{1, \cdots, n\} \tag{9}$$

These inductances are assigned to the average value of

The choice of the interval size determines whether the largesignalorthesmallsignalbehaviorismodelledmoreaccu rately.Acompromiseis attempted to model both behaviors adequately by using measurement serieswith5Vand10Vintervals.Basedonthreemeasuremen tseries,a characteristic curve is determined for the look- up table and is shown in Fig. 8b). As one can see in this Figure, the DC inductance acts similarto theACimpedancesanddecreaseswithahigherDCcurrentan dreaches saturation at 1 A. With a decreasing inductance from130Hto10H,thechargingand□dischargingtimeisshorte nedfromaround8sto0.5s.

4. Control systemdesign

behavior in time and gain response. The objective is to compensate these nonlinearities, resulting in a continuous and linear voltage reg- ulation. For this purpose, a cascade-control system is developed (see Fig. 9). Two identical inner-loop controllers (C_{DC}) control the DC cur- rents of the VIs and also compensate the nonlinear time response. An outer-loop controller C_{LVR}tracks the set point, i.e. corrects disturbances, while compensating the nonlinear gain response. To design suitable controllers, desired closed-loop systems are defined for the inner- loops and the outer-loop. These desired systems are constrained by the fea- sible hardware range. Based on these desired systems and the LVR model, the controllers are computed.

For the two identical inner-loops, the desired time

thedesiredtransferfunctionneedstobeslowerthantheinner.

According to simulations, a time-constant of 5 s achieves good results andisusedfor$\tilde{H}$LVR.

$$H_{LVR}(s)=\frac{C_{LVR}P_{LVR}}{5\cdot s+1\quad 1+C_{LVR}P_{LVR}} \tag{12}$$

To obtain the outer-loop controller $C_{LVR}$from (12), first the new plant P_{LVR}needs to be derived. P_{LVR}combines the new time behavior, whichischaracterizedby$\tilde{H}$DC,andthegainbehaviorK_{LVR}specifiedby the LVR circuit, which is depicted in Fig. 4a) as the control path overlay. Because regarding on (1), $I_{DC,Bypass}$is fully dependent on $I_{DC,Chk}$and K_{LVR}depends only on $I_{DC,Chk}$. Thus, the new plant $P_{LVR}$is calculated as:

$$P_{LVR}(s,I_{DC,Chk})=K_{LVR}(I_{DC,Chk})\tilde{H}_{DC}(s)=\frac{K_{LVR}(I_{DC,Chk})}{1.66\cdot s\quad 1} \tag{13}$$

Basedon(12)and(13),C_{LVR}isobtainedasfollo

$$C_{LVR}(s,I_{DC,Chk})=\frac{1.66\cdot s+1}{5\cdot K_{LVR}(I_{DC}} \tag{14}$$

response is lim- ited by the highest charging / discharging time of the DC circuits DC 1.66

Overshooting the input signal U_{DC}would decrease this time, but this is not possible for discharging because the input signal $U_{DC}$is limited to 0Vbythecontrolhardware.Forbothinner-loops,adesiredclosed-loop systemisdefinedasafirst-ordertransferfunction$\tilde{H}$DCwiththe time constant $\tau_{DC}$of 1.66 s. This transfer function should be equal to the

$$H(s)=\frac{1}{1.66\cdot s+1}=\frac{C_{DC}P_{DC}}{1+C_{DC}P_{DC}} \tag{10}$$

After inserting (8) in (10), the equation is solved to C_{DC}:

$$C_{DC}(s,I_{DC})=\frac{L_{DC}(I_{DC})\cdot s+R_{DC}}{1.66\cdot s} \tag{11}$$

According to (11), a PI controller is obtained for C_{DC}that changes its parameter L_{DC}analog to the plant P_{DC}. Due to this variable parameter, the nonlinear time behavior can be compensated.

Adesiredclosed-looptransferfunctionfortheentiresystem$\tilde{H}$LVRis defined for designing the outer-loop controller. To preventinstabilities.

Again a PI controller is obtained for C_{LVR}that changes its parameter K_{LVR}analog to the plant $P_{LVR}$and can therefore compensate the non- linear gain behavior.

Fig. 9gives an overview of the control system representing the controllers and the model approach from the previous section.

The control system is validated in the simulation environment MATLAB / Simulink. In the control approach, the time response is chosen accordingly large that theoretically there is no overshooting of the control hardware limits. But, the simulation results show that the control signals get still constraints by the hardware limits if the error between the reference and the output signal is large. The hardweare limits are set by the DC current source wich supplies the DC circuit of the VIs. The DC current source has a range between 0-1 A at 0–90 V. Due to this limits and the time response, the controllers cannot com- pensate the nonlinear behavior of the LVR model completely. Furthermore, a non-linear behavior is visible, based on the simplifica- tions in the VI modells of the AC impedance and DCinductivity.

Nevertheless,thecontrolsystemrepresentsagoodcompromisebe-tween control speed and compensation of non-linearity be suffcient for the control task.

However, windup e□ects on the PI controllers occur when the

[illegible] can lead to unstable operation. To solve this issue, anti-windup systems are im-plementedforeachPIcontroller.Theusedanti-windupsystemisbased onabackcalculationwithgain.Muradetal.[15]givesanoverviewof such an anti-windup system and demonstrates its positive impact. The gain of the anti-windup system at $C_{DC}$is set to 0.1 and at C_{LVR}it is set to 100.

Next, the controller is validated in the laboratory with the LVR setup. For the validation, step responses of $V_B$are measured.

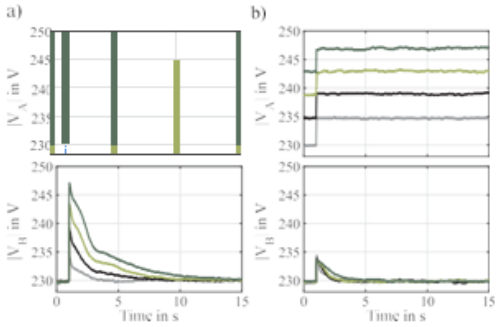


Fig. 10. Steps of $V_A$and responses of V_Ba) Di□erent step sizes b) Di□erent startingvoltages.

Theoretically, the step responses should be a decaying exponential function, but due to nonlinearities, the responses deviate as seen in Fig. 10a). This especially applies for steps larger than 10 V. For 4.5 V- steps, the control system acts nearly linear as seen in Fig. 10b). How-
ever, for these smaller steps the response is almost twice as fast as in the simulation. These deviations are caused by the simplifications during modelling. Evidently the DC inductance L_{DC} is modeled too large for small steps. In further approaches, parameter adjustment can be attempted to find a better compromise between the small- and large- signal behaviors.

All in all, the control behavior is satisfying, as the most non-

linearities are compensated. Moreover, the control system is suitable as the control act is robust with a control time less than 10 s, and as the control accuracy is lower than 1 V without overshooting. Due to the anti-windup system, good stability is achieved even when the control range is exceeded.

5. Power quality analysis

The novel LVR with the developed control system is evaluated re- garding to its influence on PQ. For this purpose, the usage of the novel LVR is compared to the usage of a stepped LVR. For reference, a setup without any LVR is also measured.

For the PQ analysis, a test-grid is configured in the laboratory in- frastructure of the smart-grid-tec-lab at the ie³[20], which is depicted in Fig. 11. A power amplifier is connected via a 300 m cable and a transformer to the external grid. Depending on the setup, an LVR technique can be linked in series between the line and the power am- plifier.

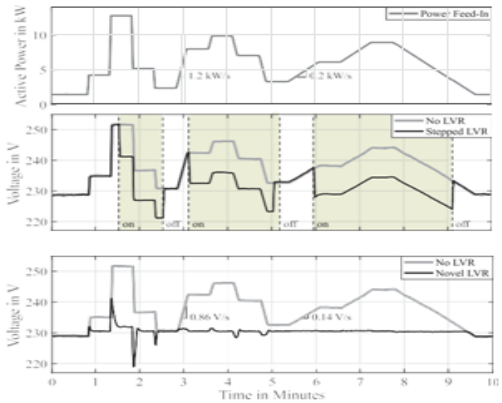


Fig.12. Single-phase power feed-in and the resulting voltages at bus bar (B) for the di erent setups.

Table 1

PQ Parameteres for the analysed Voltage Sequenzes (mean ± standard de- viation) and requirements of standard *EN50160[1], **EN 61000-2-2[2].

Case	Voltage in V			THD$_V$ in %			Flicker P_{st}
All Cases at (A)	230	±	0.3	1.9	±	0.03	0.1
Without LVR at (B)	239	±	5.3	2.0	±	0.06	0.9
Stepped LVR at (B)	233	±	3.8	2.0	±	0.05	1.6
Novel LVR at (B)	231	±	0.6	2.4	±	0.13	0.9
Standard	230	±	10%*	≤8*			≤ 1**

This paper focuses on the issue of voltage rise due to the feed-in of DER, i.e. the analysis considers the LVR operation in voltage reduction mode. For the feed-in, the power amplifier generates an active power signal with different gradients of power change. The resulting line current causes a voltage drop at the cable. As the voltage at bus bar (A) is kept constant by the external grid, the voltage at bus bar (B) in- creases.

Fig. 12 illustrates the single-phase power feed-in and the resulting voltages at bus bar (B) for the different setups. For the measured voltage sequences, the mean voltages with standard deviations are given in Table 1. Additionally, the voltage distortion THD$_V$ and the sho

rt term

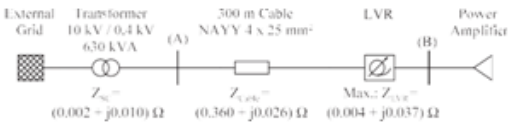


Fig. 11. Configuration of the test grid.

flicker P_{st} (weighted 10 min mean) are listed. For comparison, the re- spective requirements of the standard are given last.

In the reference setup, the voltage signal at bus bar (B) tracks the power signal. With the usage of an LVR, the voltage rise at bus bar (B) should be compensated. The stepped LVR can reduce the line voltage by 10 V. It switches on at 236 V and switches off at 225 V with a delay of 10 s. With this mechanism, the mean voltage decreases by 6 V for the chosen feed-in scenario. Nevertheless, the on-off control of this LVR amplifies the voltage fluctuations and emits additional flicker. For this scenario, the flicker even exceeded the required value of 1%.

ThenovelLVRadjuststhevoltageatbusbar(B)inacontinuousway by tracking a set-point of 230 V. Due to the slow control, rapid voltage variations initially result in control deviations, which are gradually compensated. However, gradients of 0.14 V/s can be completely compensated. With a voltage rise above 250 V the control range of the new LVR is exceeded, but still the voltage is reduced with the maximum range of 20 V. As the voltage follows a set-point, there are less voltage fluctuations and the dynamic voltage characteristic is improved. As aresult, the mean voltage decreases about 8 V without amplifying the flicker value. The setup has the highest THD_V caused by the saturation effects in the VIs. However, due to the optimized combined control presented in Section 3 the THD_V is lower than in comparable LVR de- vices based on VIs [11] and clearly complies with therequirement.

Via the grid impedance, the voltage interferences expand primarily tothesubordinatedfeedersection,andthusthePQatbusbar(A)isnot influenced by theLVRs.

CONCLUSION

This paper dealt with a novel LVR and its PQ optimized regulation.The novel LVR is distinguished by the use of the VI technique, which enables a robust and continuous control. Three results have been pro- vided in the course of this paper.

First, a detailed model is presented, which considers the nonlinear behavior of the novel LVR. In this paper, the model is necessary for the control design. Besides that, the model can be used later for dynamic RMSsimulations.However,itgotevidentthatthesignalbehaviorofthe model does not completely match the LVR in laboratory. In further approaches, parameter adjustment can be attempted to find a better compromisebetweenthesmall-andlarge-signalbehaviors.

Second, the control approach for a PQ optimized regulation has beengiven.Basedontheopen-loopcontrol,sideeffectsaremitigatedto an acceptable level. This is achieved by specifying a combined control for both VIs which avoids undesirable control states. The additional closed-loop control proves to be robust and suitable for the desired control task and compensates mostof the nonlinearities.

Third, the laboratory analysis evaluated remaining side effects of the novel LVR with regard to PQ and the results were compared to the usage of a stepped LVR. According to the analysis, both LVRs improve the static voltage characteristic. While the stepped LVR amplifies the voltage fluctuations and emits additional flicker, the novel LVR does not generate such kind of interferences, although there is still some harmonic distortion emission. Thus, the deployment of a simpler stepped LVR can be feasible in some situations, but it is advisable to chooseanLVRwithlesssideeffectslikethenovelLVRpresentedinthis paper if the corresponding PQ parameters requireit.

Conclusively, this paper provided the conditions for the upcoming field test in a distribution system which is the final part of the InLiNe project. Additionally, the model provided in this work can be used to carry on the analysis of the novel LVR in different directions. For example, it would be possible to examine the control of voltage un- balances or the interoperability with other voltage regulation equip- ment.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influ- ence the work reported in this paper.

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