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Design and Implementation of Reconfiguarable Router for Network on Chip (Noc) Using System Verilog

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ABSTRACT—FPGA based plan of Reconfigurable Router for NoC applications is proposed in the present work. Structure passage of the proposed Router is finished utilizing SystemVerilog. The router planned in the present work has four channels (in particular, east, west, north and south) and a crossbar switch. Each divert comprises of First in First out (FIFO) supports and multiplexers. FIFO buffers are utilized to store theinformation and the input and the output of the information are controlled utilizing multiplexers. Initially, south channel is structured which incorporates the plan of FIFO and multiplexers. From that point forward, the crossbar switch and other three channels are structured. All these planned channels, FIFO buffers, multiplexers and crossbar changes are coordinated to shape the total router architecture. The proposed structure is simulated utilizing Modelsim and the RTL view is acquired utilizing vivado. Xilinx SPARTAN-6 FPGAs are utilized for implementation of proposed plan. Power dissipation of the proposed reconfigurable router is decreased utilizing Power gating system. All out power is determined by the utilization of XPower Analyzer apparatus. Acquired outcomes demonstrate that the proposed plan devours less power contrasted with the recently structured reconfigurable switches.

Keywords-Network on Chip(NoC);Reconfigurable Router ;First in First out(FIFO)Buffer; Crossbar Switch; Multiplexers; Register Transfer Level(RTL) Design, Low Powe,power gating.

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I. INTRODUCTION

NoC is an innovation that is biased to expel the deficiencies of the buses. It is a point of view to structure the communication subsystem between IP cores in a SoC design. System on Chips utilizes devoted buses for the communication among different IP cores. These buses don't give enough adaptability to the communication. NoC is an elective worldview to evacuate issues identified with the buses by utilizing a communication network of switches/routers interfacing the IP cores. In spite of the fact that, the system on chips giving answers for the issue identified with the bus based structures and considered as the fate of the ASIC design, these design faces a few structure issues. First is the reasonable topology for the objective NoCs to such an extent that the design requirements and performance needs are fulfilled. Second is, the network interfaces configuration to get to the on chip network and routers give the physical interconnection channel to transport information between processing devices. Third is, the decision of communication protocols which are reasonable for on chip interconnection networks. At long last, as innovation scaled and switching speed develops, network on chips for future become increasingly prone to faults and errors. The NoC more often have three basic components-routers, links, and wrappers. Router or switch is a significant part of NoCs. The performance improvement, low area, and low power are essential necessities of the router design. The objective of the present work is to plan a reconfigurable router for use in NoCs. As a router contains different components like FIFOs, Arbiters and so on; the center is to plan design components for the low power, low area and high performance.

II. PROPOSED WORK

1. Original Router Architecture

The proposed Router design was installed in the SoCIN NoC. SoCIN has an ordinary 2-D-mesh topology and parametric router architecture. The router design utilized is RaSoC, which is a routing switch with up to five bi-directional ports (Local, North, South, West, and East), each port with two unidirectional channels and every router associated with four neighboring routers (North, South, West, and East). This router is a VHDL soft core, parameterized in three measurements: communication channels width, input buffers depth, and routing information width.

The design utilizes the wormhole switching approach and a deterministic sourcebased routing algorithm. The routing algorithm utilized is XY routing, equipped for supporting deadlock free data transmission, and the flow control depends on the hand-shake protocol. The wormhole methodology breaks a packet into numerous flow control units called flits, and they are measured as a fundamental several of the channel width. The first flit is a header with destination address pursued by a lot of payload flits and a tail flit. To demonstrate this data (header, payload, and tail flits) two bits of each flit are utilized.

There is a round-robin arbiter at each output channel. The buffering is available just at the input channel. Each flit is put away in a FIFO buffer unit. The input channel is instantiated to all channels of the NoC, and in this way all channels have a similar buffer depth defined at design time.

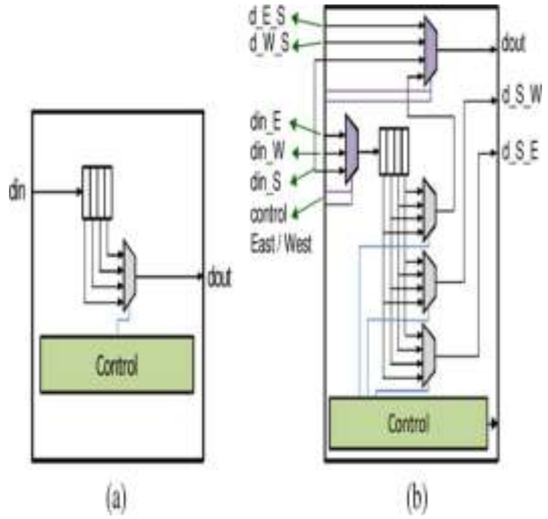


Fig.1.Input FIFO (a) original and (b) proposed router

2. Reconfigurable Router Architecture

On the off chance that a NoC's router has a bigger FIFO buffer, the throughput will be bigger and the latency in the network smaller, since it will have less flits stagment on the network. Nevertheless, there is a point of confinement on the expansion of the FIFO depth. Since every communication will have its characteristics, sizing the FIFO for the worst case communicationscenario will compromise not only the routing area, but power as well. However, if the router has a little FIFO depth, the latency will be bigger, and quality of service (QoS) can be compromised. The proposed arrangement is to have a heterogeneous router, in which each channel can have a different buffer size. In this circumstance, if a channel has a communication rate smallerthan its neighbor, it might lend a portion of its buffer slots that are not being utilized. In an alternate communication pattern, the jobs might be turned around or changed at run time, without a redesign step.

The proposed design can continue execution because of the way that, measurably, not all buffers are utilized constantly. In our design it is possible to powerfully reconfigure different buffer depth for each channel. A channel can lend part or the entire of its buffer slots as per the requirements of the neighboring buffers. To reduce connection costs, each channel may just utilize the available buffers slots of its right andleftneighborchannels. Thisway, eachchannelmayhaveup to multiple times more buffer slots than its original buffer with the size defined at design time.

Fig. 1 demonstrates the original and proposed input FIFO. Comparing the two designs, the new proposal utilizes more multiplexers to permit the reconfiguration process. Fig. 1(b) presents the South Channel as an example. In this architecture it is possible to dynamically configure different buffer depth for the channels. As per this figure, each channel has five multiplexers, and two of these multiplexers are capable to control the input and output of data. These multiplexers present a fixed size, being autonomous of the support estimate. Other three multiplexersare important to control the read and write procedure of the FIFO. The size of the multiplexers that control the buffer slots builds as per the depth of the buffer. These multiplexers are controlled by the FSM of the FIFO. So as to diminish directing and additional multiplexers, we received the system of changing the control some portion of each channel.

A few guidelines were defined so as to empower the utilization of buffers from one channel by other neighboring channels. At the point when a channel fills all its FIFO it can barrow buffer words from its neighbors. First the channel requests buffer words to the right neighbor, and in the event that despite everything it needs more supports, it endeavors to acquire from the left neighbor FIFO. Thusly, a few signs of eachchannelmustbesentfortheneighboringchannelsin order to control its stored flits.

Inresult, eachchannelneedstoknowhowmanybufferwords it employments of its own channel and of the neighboring channels, and furthermore how much the neighbor channels involve of its own buffer set. A control block advises this number. At that point, in light of this data, each channel controls the storage of its flits. These flits can be stored on its buffer slots or in the neighbor channel buffer slots. Each input port has a control to store the flits and this control is situated in pointers. Each input channel needs six pointers to control the read and write process: two pointers to control its very own buffer slots, two pointers to control the left neighbor bufferslots, and twomorepointersto controlthe right neighbor buffer slots(for each situation, one pointer to the read operation and one pointer to write operation).

In this plan, we are not thinking about the LocalChannelusingneighboringbuffers, onlytheSouth, North, West, and East Channel of a switch can utilize their nearby neighbors.

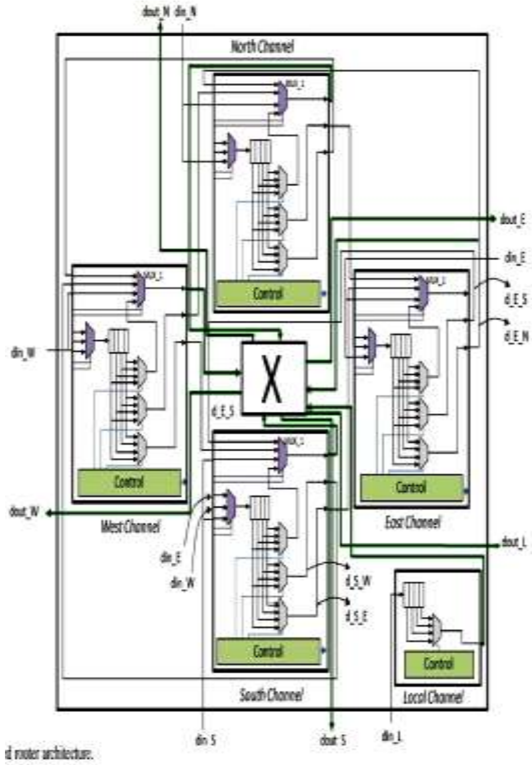


Fig.2.proposed router architecture

As referenced previously, the advance granularity utilized in this proposal is a bufferslot. Theareresultsof the reconfigurablerouter would not present a significant change if credit granularity was increased. Thisis duetothe truth thatthe controloverheadis defined essentially by the FIFO's control circuit. As the buffers are implementedusing circularFIFOs, the FIFO pointers are incrementedtoeachnewslot, andthiscontrolwillbethesame whatever the utilized loan granularity. On the off chance that we increment the loan granularity to more than one slots, at that point the loss in performance could be huge, and the decrease in area or power would be insignificant.

Inaddition, weareconsideringsharingofthebufferslotsonly among neighboring channels. This choice depends on the expenses of interconnections, multiplexers, and rationale to control the combination of all advances among all information channels. Thus, the area and power utilization would be a lot bigger in the event that we con-sider the last case, and the additions in execution would not be sufficiently extensive to remunerate this additional expense.

Fig. 2 demonstrates the channel of Fig. 1(b) sorted out to establish the reconfigurable router. Each channel can get three information inputs.

LetusconsidertheSouthChannelasanexample, havingthe accompanying sources of inputs: the own input (din_S), the right neighbor input (din_ E), and the left neighbor input (din_W). For illustration purposes, let us expect we are utilizing a router with buffer depthequalto4, andthereisarouterthatneedstobeconfigured as pursues: South Channel with buffer depth equivalent to 9, East Channel with cradle buffer depth equivalent to 2, West Channel with buffer depth equivalent to 1, and North Channel with buffer depth equivalent to 4. In such case, the South Channel needs to obtain buffer slots fromitsneighbors.

AstheEastChanneloccupiestwoofitsfour slots, this channel can loan two slots to its neighbor, yet and still, after all that, the South Channel still needs progressively three buffer slots. As theWestChanneloccupiesonlyoneslot, thethreemissingslots can be loaned toward the South Channel. At the point when the South Channel has a flit stored in the East Channel, and this flit must be sent to the output, it is passed from the East Channel toward the South Channel (d_ E_ S), thus the flit is legitimately sent to the output of the South Channel (dout_ S) by a multiplexer. The South Channel has the fallowing outputs: the own output (dout _S) and two increasingly outputs (d_ S_ E and d_ S_ W) to send the flits stored in its channel however having a place with neighbor channels.

Thechoicetoresendtheflitsstoredinaneighborchannelstoitsownchannelbeforesendingthemtotheoutputwaspreferred so as to avoid changes in others mechanism of the architecture. As such we didn't change the routing algorithm, staying away from the deadlock, since the NoC continues utilizing XY routing, which is naturally deadlockfree.Withthisdefinition,thecomplexityoftheimplementationtoobtainthecorrectfunctionoftherouterwasreducedinthis aspect. Each flit stored in a neighbor channel comes back to the particular channel when it should be sent to a output channel. For this situation, when an input channel is associated with an output channel, theflitsaresentone-by-one, andthepointersareupdatedaseach flit is sent.

Aseachchannelknowshowmanybufferslotsithasallocated, when the pointers present a location having a placewithaneighborbufferslot,thecontrolofthefirstm ultiplexerofFig.1(b)allowsthesendingoftherespectiveflitstotheoutputofitschannel.As we don't change the directing approach, there is no plausibility of enteringadeadlocksituation. Ofcourse, onecouldbeconcerned around one channel asking buffers from another channel which is additionally requesting supports. Since just the neighbors are gotten some information about loaning/obtaining, no cycle can be made, and henceforth at the circuit level there is additionally no probability of deadlock.

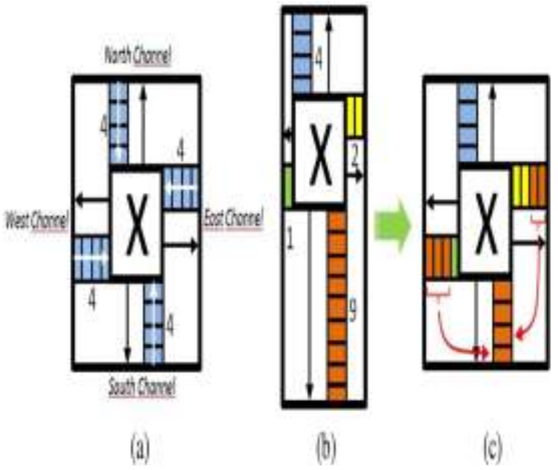


Fig.3. (a) Router design with FIFO depth 4; (b) One example of need of configuration of the router; (c) Reconfiguration of the buffers to attend the need

Fig. 3 demonstrates a case of the reconfiguration in a router accordingtoaneededbandwidthineachchannel.First, a buffer depth for all channels is chosen at configuration time, for this situation, we definedthebuffersizeequalto4,asillustratedin Fig.3(a).After this, the traffic in each channel is verified and a control defines the buffer depth required in each connect to take care of this flow, as appeared in Fig. 3(b).

The appropriation of the buffer words among the neighbor channels is acknowledged as appeared in Fig. 3(c). Then, the buffer physical aura in each channel reporter the FIFO depth at first defined, as appeared in Fig. 3(a), yet the allotment of buffer slots among the channels can be changed at run time, as exemplified in Fig. 3(c).

III. RESULTS AND DISCUSSION

1. SIMULATION RESULT

Output waveform of the total south direct is appeared in Fig. 4. All the four channels are associated with crossbar switch since definite output is taken from the crossbar.Code is written in System Verilog and simulated utilizing Modalsim. By giving a few information into FIFO, stack memory areas could be checked. Simulation waveforms of FIFO are appeared in Fig. 4. In the simulated waveforms it very well may be confirmed that FIFO_ buffer locations or memory areas are involved by this arrangement of information or not. It tends to be found in Fig. that every one of the four memory areas are involved by a progression of information. And fig.4.also indicates that how the FIFO buffer of south, west and east occupies by information value. Waveform of reserved value in south, east, west and north channels are shown. The total output of south channel is taken from themux5 of the south channel, and connected to the crossbar switch.

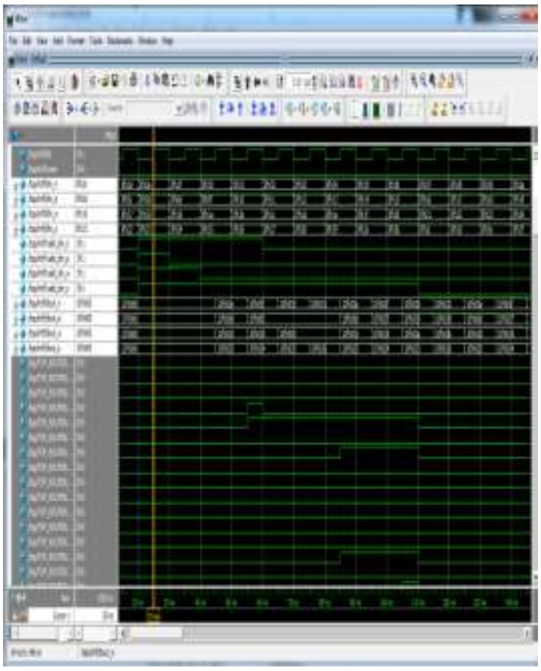


Fig.4.simulation waveform of complete south channel

2. SYNTHESIS RESULT

Synthesis is the process of transforming an RTL specified design into a gate level representation. And it also provides RTL view of the design, design summary of circuit and total power consumption by the circuit. Theseare shown in the fallowing fig.5, fig.6, and fig.7 respectively.

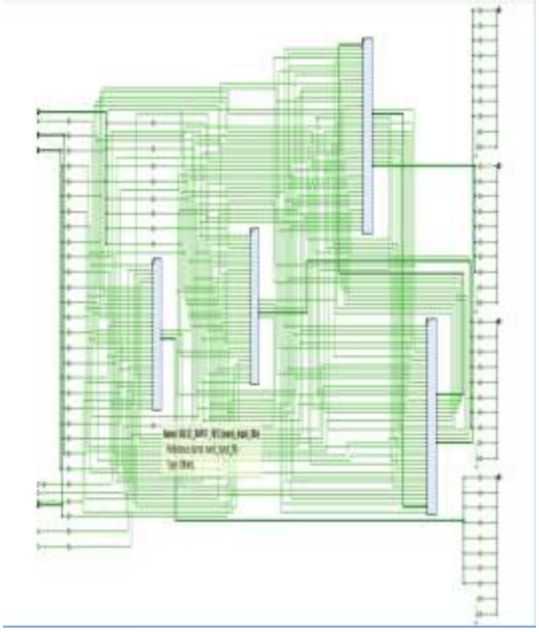
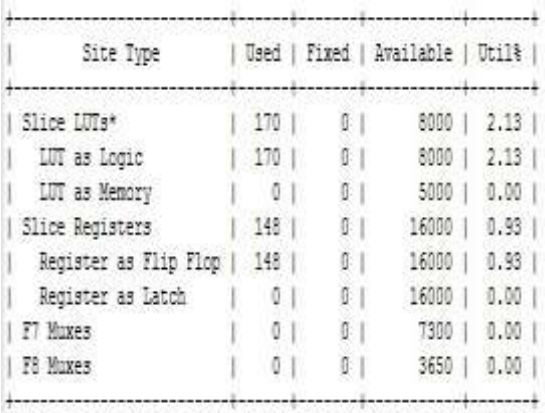


Fig.5.RTL view of the complete architecture



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+------------------------+------+-------+-----------+-------+
|       Site Type        | Used | Fixed | Available | Util% |
+------------------------+------+-------+-----------+-------+
| Slice LUTs*            |  170 |     0 |      8000 |  2.13 |
|   LUT as Logic         |  170 |     0 |      8000 |  2.13 |
|   LUT as Memory        |    0 |     0 |      5000 |  0.00 |
| Slice Registers        |  148 |     0 |     16000 |  0.93 |
|   Register as Flip Flop|  148 |     0 |     16000 |  0.93 |
|   Register as Latch    |    0 |     0 |     16000 |  0.00 |
| F7 Muxes               |    0 |     0 |      7300 |  0.00 |
| F8 Muxes               |    0 |     0 |      3650 |  0.00 |
+------------------------+------+-------+-----------+-------+
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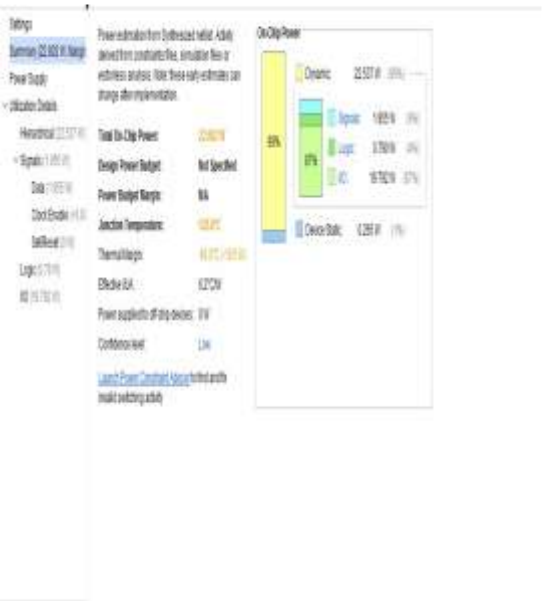
Fig.6.design summary of circuit



Total On-Chip Power: [illegible]
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: [illegible]
Thermal Margin: [illegible]
Effective θJA: [illegible]
Power supplied to off-chip devices: 0 W
Confidence level: Low

Fig.7.total power consumption by circuit

IV. CONCLUSION

Router is the most significant part of NoCs plan. A changed reconfigurable router to be utilized in NoCs is proposed in the present work with targets of low power utilization and high performance. The proposed router design comprises of four channels (to be specific, east, west, north and south) and a crossbar switch. Each direct has First in First out (FIFO) buffers to store the information and multiplexers to control the input and output of data. Stack tallness of a FIFO buffers is viewed as four and stack width of FIFO is viewed as three. It implies it has four areas and every area can store three piece of information. Each channel has five multiplexers. Two multiplexers are utilized to control the input and output of information and staying three are used to control read and write procedures of FIFO.System Verilog is utilized for the structure passage of this Router. For simulation and synthesis MODELSIM EDITION10.4aand vivado are utilized individually. The proposed reconfigurable router is synthesized utilizing Xilinx SPARTAN-6 FPGAs. After Simulation and Synthesis of the proposed router architecture, absolute power is determined with the assistance of XPower analyzer apparatus. The power gating system is utilized to decrease the power dispersal of the proposed reconfigurable router. And power is reduced after applying power gating technique in the proposed router architecture compared to the previous architecture.

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