RESEARCH ARTICLE OPEN

FPGA-Based Low-Power Quadrature Digital Converter for Real-Time 5G and IoT SDR Systems

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ABSTRACT
In Today's digital communication world Sample rate translation plays an imperative role in each and every aspect. Digital up/down converters (**DDU/DDC**) can be used to achieve multirate signal processing. The design of a digital up and down converter with high-performance for software definedradio (**SDR**) applications is discussed in this paper. At the transmitter, digital up converters are used to transform the original message signal to an intermediate frequency (**IF**) signal. At the receiver end, digital down converters are used toperform the reverse operation. The specification of anelevated All-digital up/down converter with adjustable **IF** configurations is also discussed in this article. Interpolation/decimation is used to up/downconvert the signal, with just a reconfigurableanti-alias filter retaining the specified spectrumonly during thesample rate translation.This results in relatively highapproach with limited power consumption. To incorporate scalable IF settings, we had to use a novel approach. The resulting enhanced framework is ideal for coaxial software defined modem implementations and can handle signals up to 160 MSPS.
Keywords: Digital down converter (DDC), Digital up converter (DUC), Direct digital synthesizer (DDS), Cascade integrator comb (CIC), Field programmable gate array (FPGA), ADC, DAC converter, FIR filter. Intermediate frequency (IF).

Date of Submission: 20-05-2025 Date of acceptance: 30-05-2025

I. INTRODUCTION

In modern era due to technological advancementsdigital techniques are now capable of performing IF/RF functions.As a result, in today's communication applications, the distinction between digital and analogue components is becoming a design parameter [1]. The standard solution of a digital core handling baseband functionality as well as analogue IF/RF front-end might not be always potent.However, this should not preclude the use of modern methods to eliminate analogue functionality. Somewhat more, the benefits that digital technologies should have been weighed adequately throughout the development process.Analogue hardware is usually vulnerable to a wide range of non-idealities and nonlinear effects. This may be problematic, particularly if a sophisticated modulation technique is needed. The majority of these undesirable effects are eliminated as automated tools are used .However, since digital hardware has drawbacks (for example, the existence of efficient AD converters), it cannot be considered a fundamental solution. We present a proper realization of a moderate quadrature up as well as down converter in this article. Several scholars have already looked into this topic [2][4].However, in order to attain the optimal results, both of these strategies sacrificed simplicity, since they all share a common IF band.It is shown that the trade-off among programmability and efficiency may not seem to be so stark, and therefore that significant versatility can be maintained when meeting the requisite performance targets.This aids in the development of software radio system with various parameters collection on reconfigurable device platform.

The transmitting side of a wireless communication modem is built using advanced Digital up converter (DUC), with an elevated Digital Signal Processor (DSP) performing baseband processing and a FPGA kit performing up conversion to Intermediate Frequency (IF).Also a Digital down converter (DDC) is also utilized on the receiver end of wireless communication implementing the opposite action.

Thisresearch article is organized as follows: the first section will provide a quick summary of possible digital down conversion methods, as well as their benefits and downsides. Following that, in second section, the device

specifications will be discussed, followed by a description of the chip design after that section.The last section includes a summary of chip specifications and simulation performance as well as conclusion.

Design of DUC and DDC

I. Digital up converter

The up convertermodulates two message signals, such as in-phase as well as quadrature phase, into a unique reasonable band pass signal. FPGAs may be used to realize the DUC's architecture [1]. These signals are multiplied with the digital local oscillator to achieve quadrature modulation.

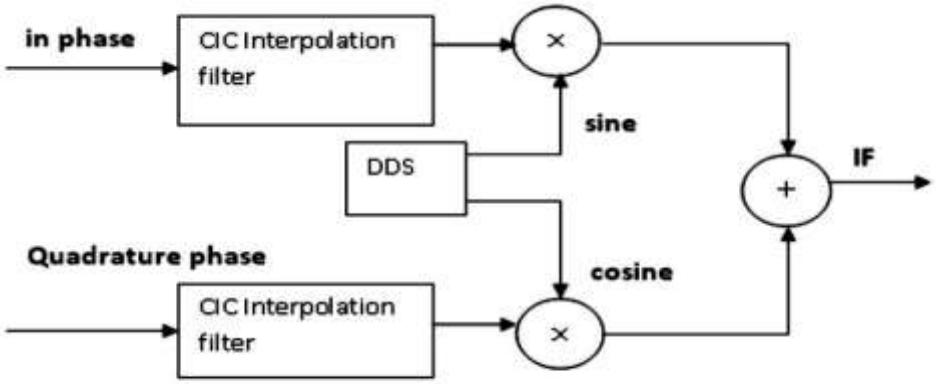

Fig : 1 Block Diagram of DUC

The generation of band pass signal based on the frequency of the digital LO, with amplitudeas well as phase offset aligned with the complex weight allocated to a certain channel. A DDS is used as the receiver for the digital LO(local oscillator).

II. Digital down converter

On the receiver end of the wireless communication system a digital IF signal is modulated by Digital down converter (DDC) with original message signal and then an in-phase as well as Quadrature signal are produced. FPGAs may be used to execute the DDC architecture.Quadrature demodulation is achieved by multiplying **intermediate frequency** signals with such a local oscillator, which is implemented with a direct digital synthesizer (DDS)[1].

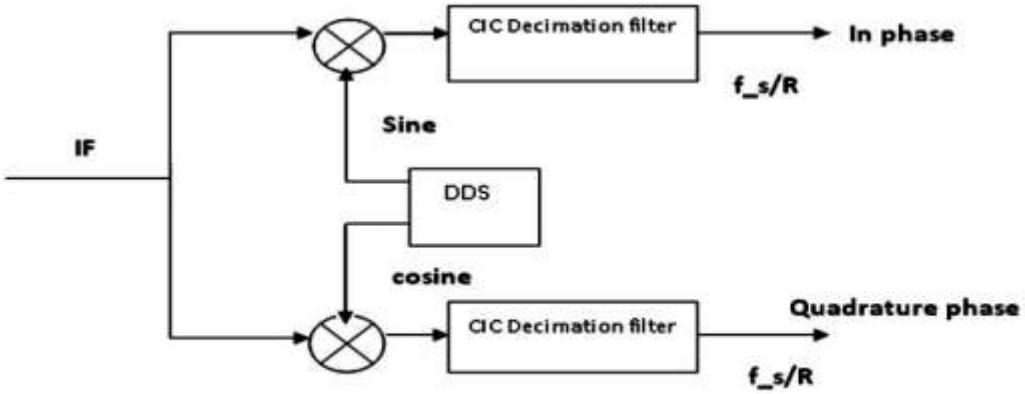

Fig : 2 Block Diagram of DDC

DUC & DDC implemented on Spartan-3 FPGA starter kit

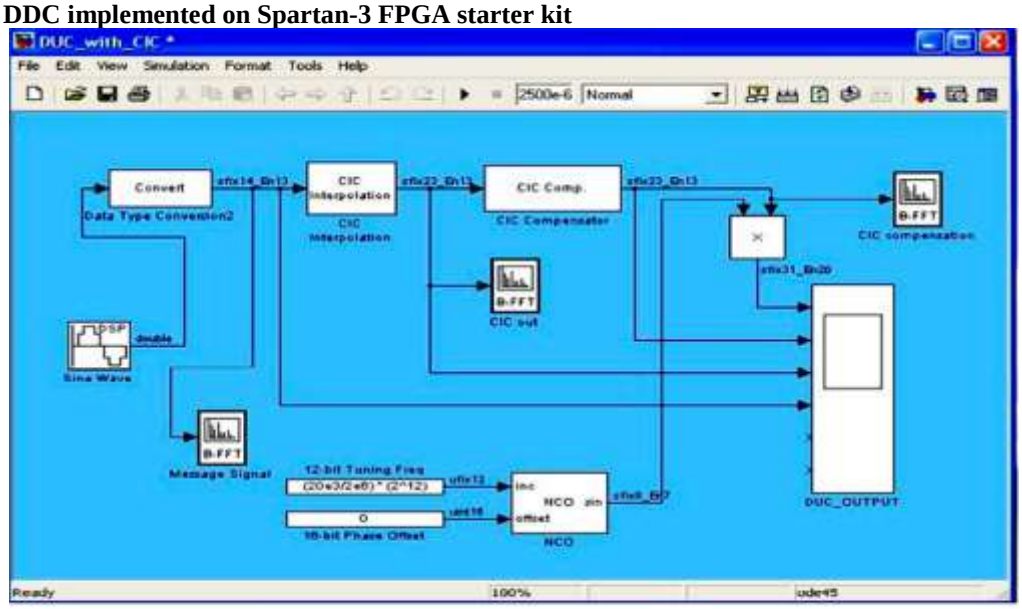

Fig : 3 MATLAB modelling of DUC

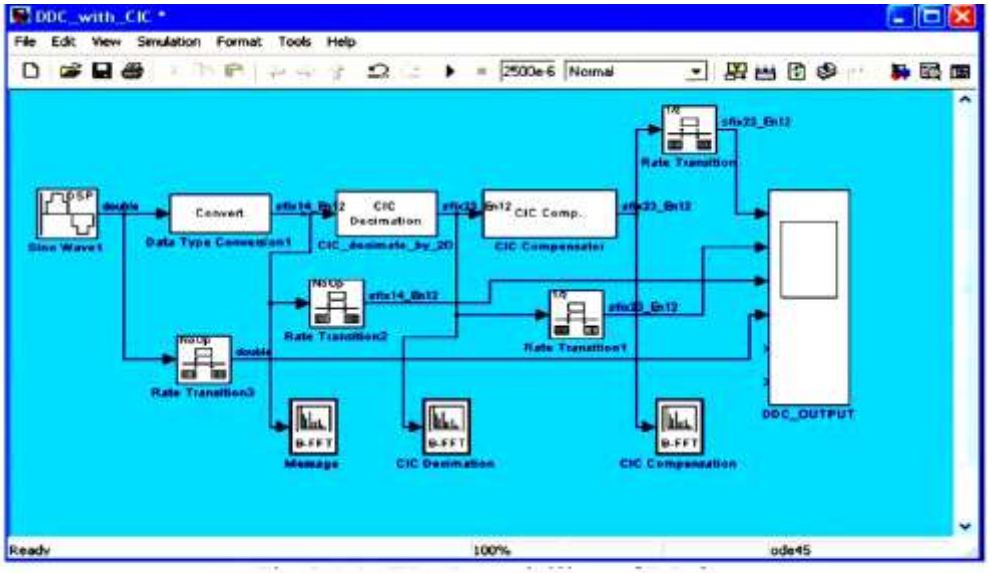

Fig : 4 MATLAB modelling of DDC

There are several methods for achieving digital downconversion. All of these alternatives have a significant effect on the eventual implementation's design constraints [3].

Just one way, configurable implementation (see [5]), such as the one seen in the upper portion of Fig.5 and based on a mixer and sine generator, have a significant degree of versatility in **IF** environments.The frequency to downconverter can be immediately changed by modifying (reprogramming) the sine generator despite affecting the remainder part of the implementation.Then limitation is that enormous number of high-frequency hardware, which significantly restricts the application's operating frequency (for example, the DDC mentioned in [5] can handle 75 MSPS and the DUCcan only handle 52 MSPS).

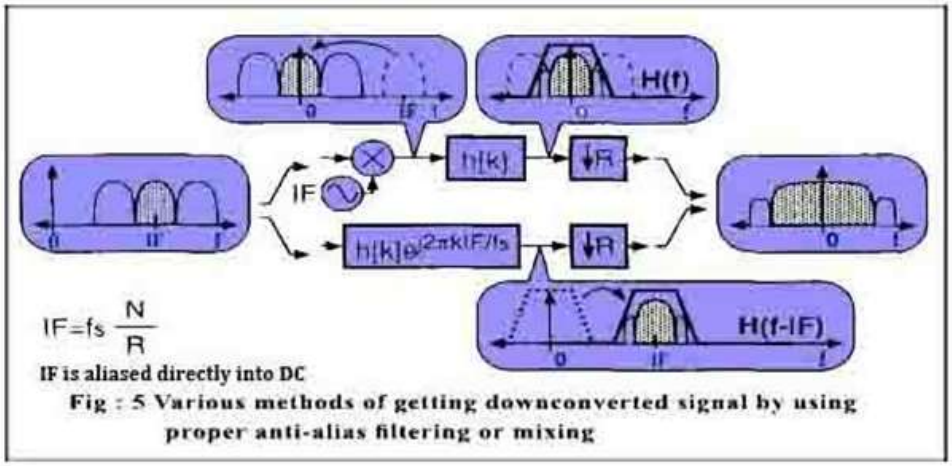

Fig : 5 Various methods of getting downconverted signal by using proper anti-alias filtering or mixing

Alternatively, methods specialized to the downconversion of a unique **IF** [4-6] might be described.These methods are mainly focused on the prominent decimation concept after that it is impossible to decide the actual location of the signal in the defined frequency range (e.g., after decimated by **2**, it's impossible to determine if a signal originally clustered about**0** or $\mathbf{f_s/2}$). Rather of downconverting the incoming signal to baseband until decimation, a anti-aliasing filter upconverts the signal just at the signal point, resulting in same ultimate result as seen in Fig.5. This renders it a compelling option in terms of both speed (e.g. 250 MSPSfor Quadrature amplitude modulation modulator/demodulator in [2]) and power consumption (see [4-6]). That being said, as the real **IF** to downconvert being converted to changed filter variables, any **IF** adjustment would be necessarily much reluctant to accomplish.

Our approach demonstrates that,while maintaining high speed, there is a chance to accomplish these issues and can provide a large level of adaptability in decimation-based downconversion. This is managed by the use of a revolutionary decimation-based solution in conjunction with an innovative implementation technique.

Overview of the System

The design specifications were derived from the MCNS (Multimedia cable network system) modem standards (see [8]), with the aim of covering the entire spectrum for upstream transmission channel.Fig.6 depicts the importance and effectiveness of the whole system. In down conversion of signal, afrequency band of 3.3 MHz, located in one of 31 available locations, being downconverted into less**IF**.

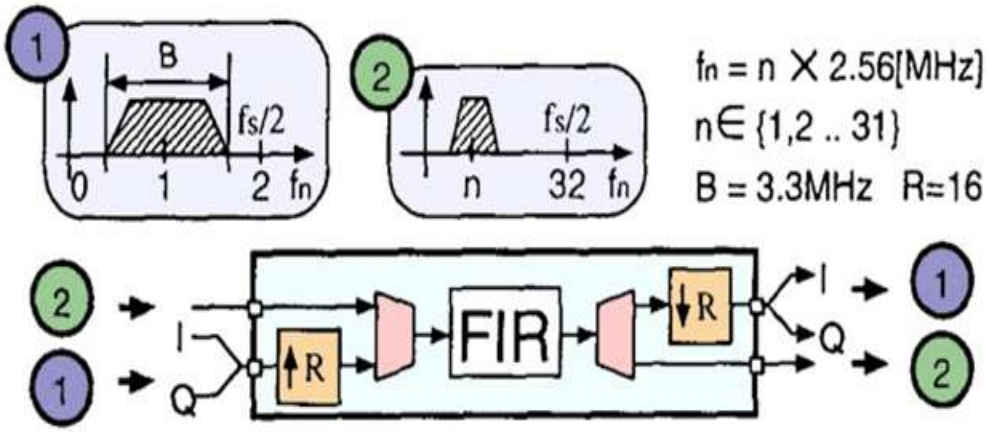

Fig : 6 Most simple System Configuration

It is reduced by 16 as well as set at **IF** = 2.56 MHzat the same time .Upconversion operates in the exact opposite direction, with lower**IF**= 3.3 MHz signal filtered by component 16 subsequently

upconverted for one of 31 viable **IF** points.Instead of an indeterminate IF, the implementation of a decimation-based downconversion approach resulted in a distinct succession of **IF**s rather than an arbitrary**IF**.

The complete downconversion by 16 was divided into two consecutive downconversions by 4 to reduce the filter criteria. Fig.7 depicts the signal direction through the filters. The $\mathbf{H2_8}$filter is made up of four forms, each of which preserves four **IF** groups.If**n = 17** is chosen, the channel is set in the correct location without being filtered with a frequency shift. The $\mathbf{H1_8}$filter is similar in that it integrates four forms, each of which preserves single**IF** band also employs frequency shifts as necessary.Ultimately, the **H0** filter stops the I and Q elements from aliasing. Consider the case of a channel with **n=25**. It is moved by $\boldsymbol{\pi/2}$ at the position of channel 9 in the first step, resulting in the form $\mathbf{H2_2}$ being selected within the first reduction by 4.

The signal may changed by **π** from **n = 9** to **n = 1** in the second stage, resulting in the form $\mathbf{H1_1}$ being chosen during the second decimation by 4. After filtering by the final filter **H0**, the downconverted signal will be precisely at **IF =** $\mathbf{f_s/4}$ and suitable for decoding.

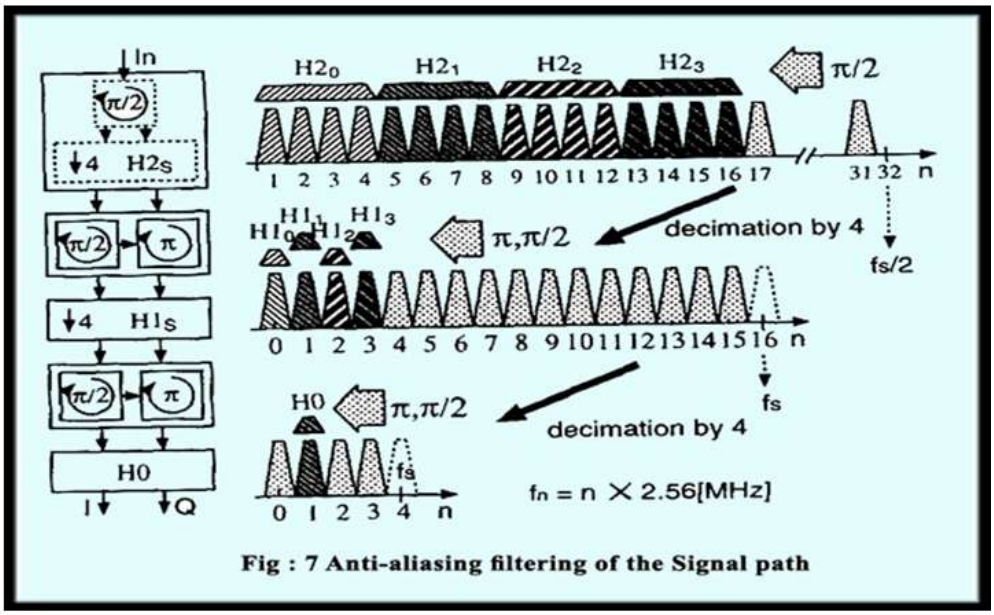

Fig : 7 Anti-aliasing filtering of the Signal path

The overall system context represents a trade-off between adaptability and multishape filter installation costs. The chip may switchbetween up conversion and down conversion mode, but not all at the same time. The **up/down** control signal selects the mode.

System Layout

The following Fig.8 depicts the entire system design. The filters **H1**and **H2**(depending on the mode) are interpolating/decimating filters, whereas the **H0** is a single rate filter. Polyphase decomposition is used to reduce the operational frequency of these filters **H1** and **H2**(both **H1**and **H2**operate at 10 MHzas well as 40 MHz respectively).As described earlier, the rotors via**π** as well as**π/2** can be used to relocate the signal spectrum's frequency so as to enhance theantialias filter design.Finally, multiplexers are required when selecting an **up/down** mode. Various design optimizations must be carried out in terms of producing an effectiveresult. A few of these will now be discussed in further extensively.

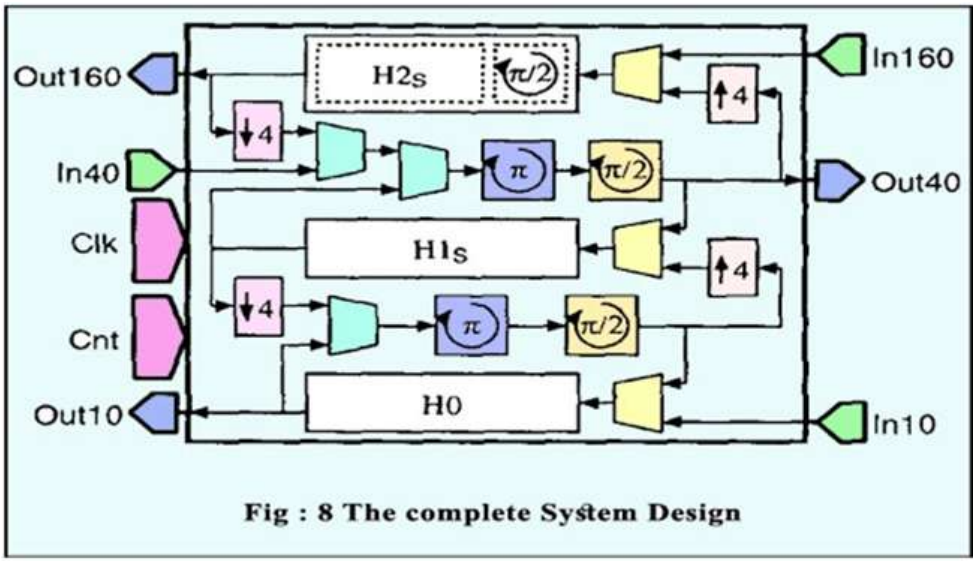

Fig : 8 The complete System Design

Configuration of a FIR filter

In connection with area and power usage, the filters are essential building blocks of the overall design and development. A method known as **Interpolated finite impulse filter** [3] is applied to ease the constraints set on the filters.The theory is that in several steps, filtering out a signal that has already been filtered from the previous stage is unnecessary. Anti-alias filter orders were dramatically decreased as a result of this process. The various filter shapes were created by complex rotation of a low-pass prototype, which results ina frequency translation / uptransformation of the filter pass band to **Intermediate frequency**(**IF**).

In filters **H1**and **H2**, polyphase reduction being utilised to minimise the operating frequency of anti-alias filters, as seen in Fig.9.

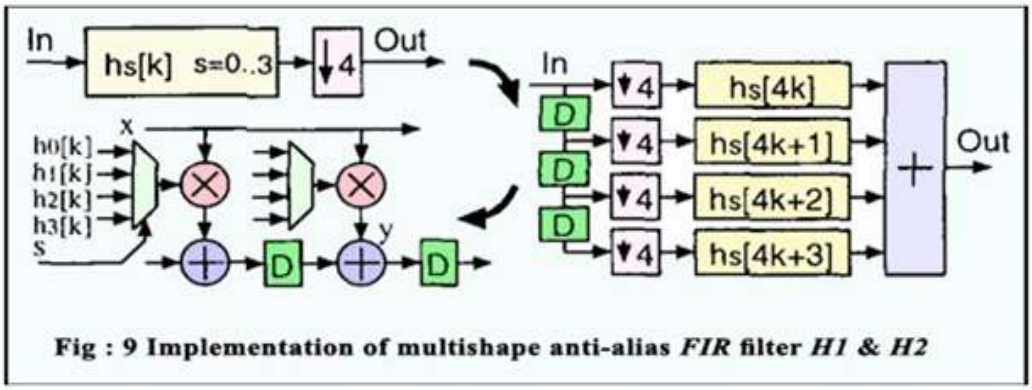

Fig : 9 Implementation of multishape anti-alias *FIR* filter *H1* & *H2*

The polyphase design of FIR filters is detailed in [2] and [6], thus it's is worth mentioning that each of these filters was split down into four concurrentsubfilters operating at four-fold lower frequency.The successful realisation of several coefficients based on various filter shapes was a key aspect of FIR filter design. To alleviate this challenge, we developed a tweaked Canonic Signed Digit (CSD) approach (for more information on the traditional CSD approach, see [7]).As with the CSD coefficients, the multiplications being broken down in a series of add-shift activities. Since various parameters lead to different shift factors, several coefficients can be implemented by having the shifts programmable rather than hardwired.This allows for the selection of suitable shift factors during operation. Add/Sub cells are used to replace adders or subtractors as desired (see Fig.10).

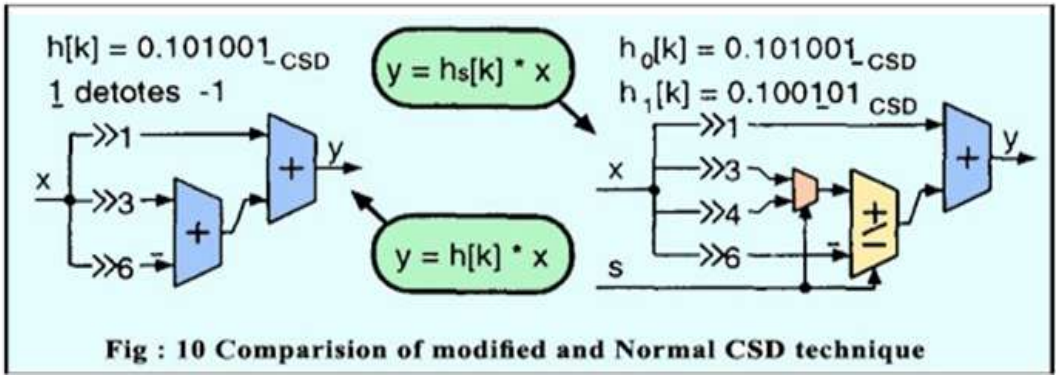

Fig : 10 Comparision of modified and Normal CSD technique

Upgrading the CSD parameters by a constant may lead to a reduced number of overall non-zero bits owing to the irregular distribution of the CSD numbers (see [7]). An extensive search is used to identify the scaling ratio properly. This method was also implemented in our design.The optimisation was performed independently for each CSD group since the **H1** and **H2**filters combine four distinct forms, consisting of four CSD groups for every filter.Following that, the scaling proportion that provided the greatest enhancement for all four forms was then chosen.

Thereal fact is that some actions just on signal spectrum may be accomplished with less hardware expense allowed for the diminution of the required filter shapes.Just the multiplications with 1, -1, and 0, i.e. **sin/cosof kπ/2,** and fewfurther multiplexing of real as well as imaginary components are required for frequency shifts by **π** and **π/2**.Because any frequency as from <$\mathbf{f_s/4}$, $\mathbf{f_s}$> interval could be moved into<**0**,$\mathbf{f_s/4}$> just using combo of **π** and **π/2** translations, all processing can be done on the <**0**,$\mathbf{f_s/4}$> portion of the spectrum. As a result, the exact number of forms in the **H1** and **H2** filters was dropped to one-fourth and one-half, respectively.

Enhancement of FIR filter configuration

Since antalias filters seem to be at the core of the architecture, they must be implemented with extreme caution [10]. The filter configuration may also be optimised by certain design factors. The optimisations would be addressed separately since they are filteringsensitive. The**H2** filter does have peculiar property that only the real part must be generated in upconversion, while certain real part must be read in downconversion mode (see Fig.11).

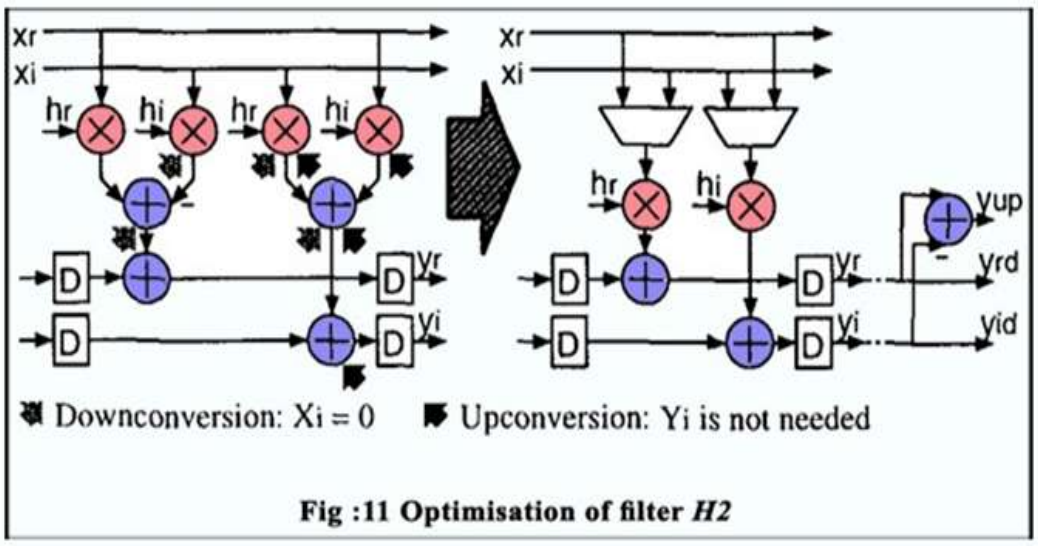

Fig :11 Optimisation of filter *H2*

It is possible to effectively minimize the circuitry of the **H2** filter by using multiplexers to identify the both (real andimaginary) input component for the multipliers, as seen in Fig.11.The **π/2** rotor can also be conveniently integrated into the filter configuration as a side effect of the added multiplexers [11]. Apart from the polyphase decomposition systems, this also excludes nearly all hardware that operates at 160 MHz.

The filter frequency shift factors in filter **H1** architecture are multiples of **π/16**. This has significant ramifications.

a. That's because the rotation parameters are still **4kπ/4**, the filter $\mathbf{H1_0}$ remains real.
b.If the existing Filters **23**-tap filter had already been symmetric (which it was), filters$\mathbf{H1_1}$ and $\mathbf{H1_3}$would appear evenly spaced requiring just half of its taps to ever be applied.
c. Filter $\mathbf{H1_2}$ would not only be true, but if any extra multiplexing operation being used, instead of four multipliers per tap, just two are needed. Since the rotating parameters have either been real or imaginary also, or $\mathbf{h_r = h_i}$, this reduction is necessary.

Polyphase Expansion

The only hardware that must operate at maximum frequency is the polyphase expansion components. Using multiplexers, we built both downconversion and upconversion parts as shown in fig.12. The severe speed requirements were met by this basic structure.

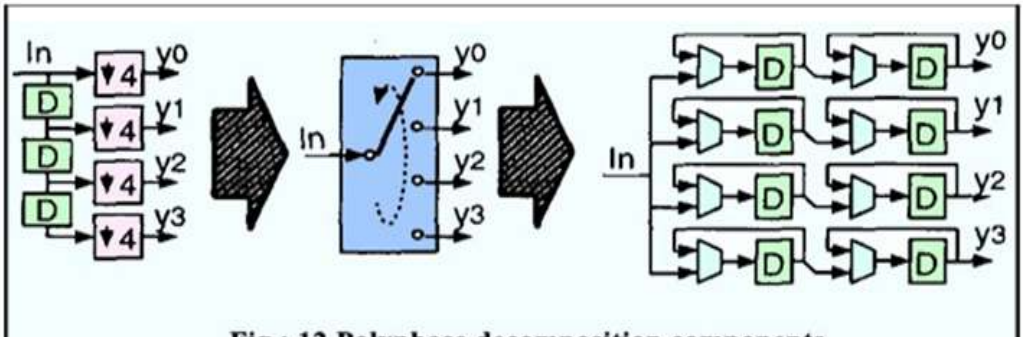

Fig : 12 Polyphase decomposition components

Assessment of chip characteristics

The design was developed with the OCAPI C++ design platform in multirate mode [13]. The C++ definition is 4400 lines long, and the Simulink design compiler generates 12000 lines of RT-level VHDL code.The chip was successfully packed out, fabricated, and practically checked. Fig.13 shows the chip specifications. Measurement circuitry and additional analogue circuitrySeparate

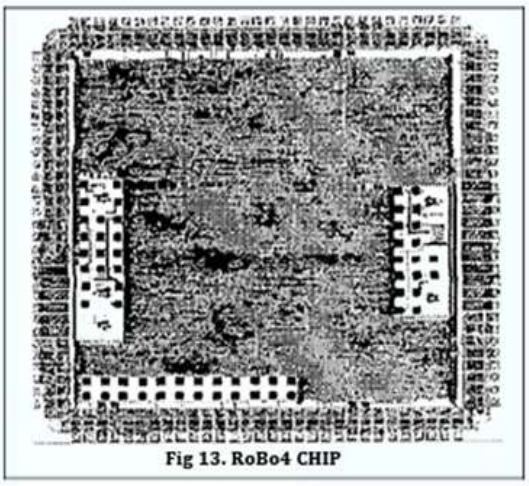

Fig 13. RoBo4 CHIP

PARAMETERS	
Technology	Alcatel-Mietec CMOS 0.5m/3.3V
Master Clock	163.84 MHz
Internal Clocks	40.94, 20.48 and 10.24 MHz
IO Word	12 bits
Internal Word	14 bits
Gate Count	86k
Core Area	24.22 mm^2
Chip Area	38.4 mm^2
Package	120 pin PGA

Clock zonebase (substrate) noise may be found in the three unique portions on either sides and also at the bottom.
Fig.14 depicts the characteristics of the three different FIR filters, and also the composite one. $\mathbf{H2_0}$, $\mathbf{H1_0}$, and **H0**are the different shapes in Fig.14as translated into DC. Any channel has the same composite characteristic, i.e. stopband attenuationand passbandripples,**S.B <- 45 dB** as well as **P.R< 0.1dB**respectively.

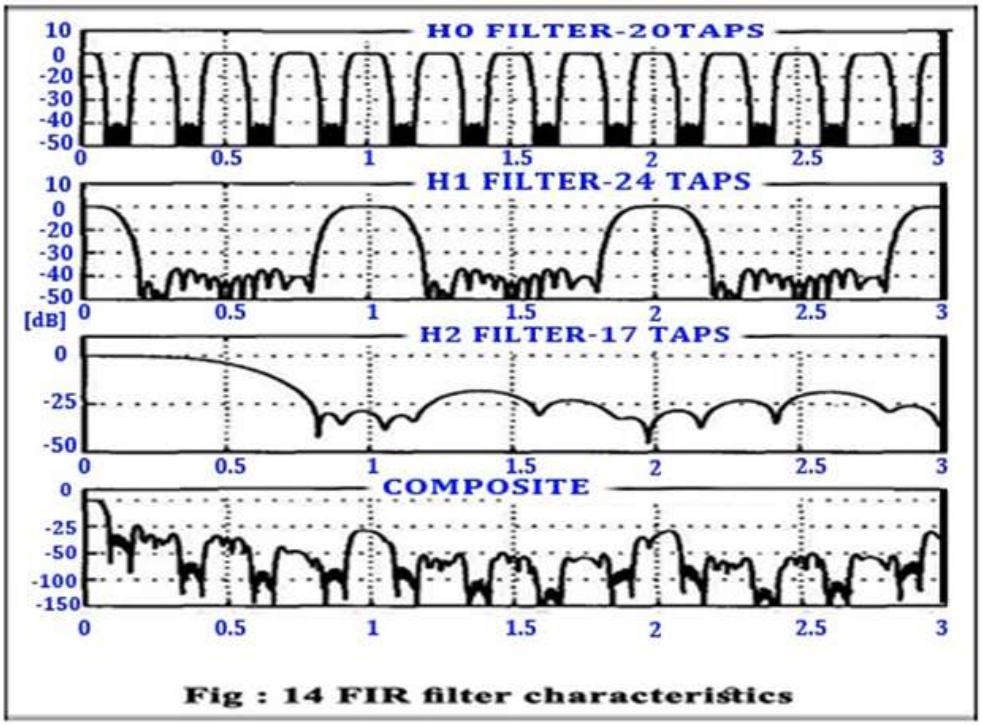

Fig : 14 FIR filter characteristics

Co-simulation of such chip with the Quadrature Amplitude Modulation (QAM) transmitter and receiver was used to test the quantization. After **RoBo4**'s upconversion or downconversion, the obtained QAM-16 signal's Error Vector Magnitude (EVM) was calculated.The values ofError Vector Magnitude(EVM) obtained from fixed point and floating point and fixed point simulations are shown in Fig.15.

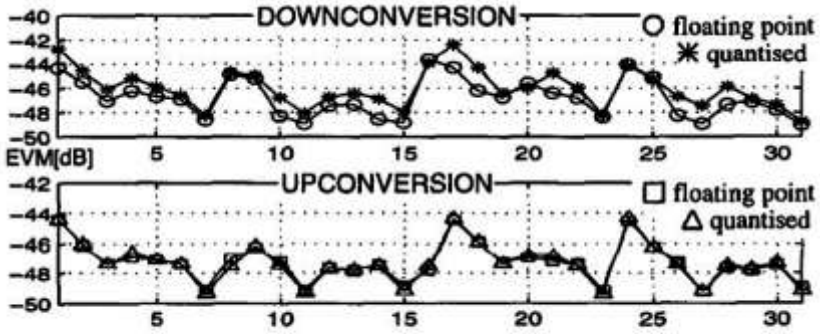

Fig : 15 Simulated EVM values with respect to the selected channel

II. CONCLUSION

An all-digital quadrature up &down converter with high efficiency has beendemonstrated. Itemploysan innovative approach to implement**IF**range diversity while remaining efficient and cost-effective. It also demonstrates that all-digital up and downconversion at high frequencies and with high efficiency is possible.

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