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RESEARCH ARTICLE OPEN ACCESS

Cascaded Multilevel Inverter with Reduced Switch Count for Solar Generation

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ABSTRACT
Usage of Multi-Level Inverters (MLI) are at its boom, since they have low harmonics in the output when designed with higher level, high efficiency and can be designed as per the requirement. Particularly for renewable integration. The main concern for designing MLI is its high component counts with high-level output. To deal with this problem the conventional topologies of MLI are converted into modular structure to obtain the high-level output with reduced component count. For this cascaded structure is best suited since its each unit are separate which can be easily molded to design the required modular structure. In this work 19-level cascaded topology of inverter for solar power integration into the AC-system. The topology has reduced switch count with only 12-switches and four DC-sources which very low as compared to the conventional topology which require 36 switches and 9 DC-sources. The system is designed in MATLAB environment and the gate pulses for the switches are designed using level-shifted sinusoidal pulse width modulation technique which is simple in design which can be easy to implement at high level for the system with complicated structure.
Keywords – 19-level Inverter, Asymmetrical Cascaded Modular Topology (ACMT), MPPT, Solar Generation Utility (SGU), Level-shifted Sinusoidal PWM.

I. INTRODUCTION

Scarcity in the available conventional resources and development in the unconventional power generation technology like solar, wind, fuel cell, etc., had raised the bar for inverter technology development. Since inverters acts as an interfacing medium between the DC-sources and AC utility. In this context Multi-Level Inverters (MLI) are becoming the preferred choices as they inject low harmonics even with in the grid code when high-level topology is used. Also, they have high performance efficiency and are available in various designs as per the requirement. In literature numerous MLI topologies are available including conventional and unconventional design. The conventional topologies are bulky and has low performance efficiency [1, 2]. In conventional inverter only two-level AC output is obtained with +Vdc and -Vdc. In MLI topology AC is obtained in multiple of Vdc as stair-case type waveform. MLI is preferred since its AC output resembles the sine wave hence losses are reduced with increased efficiency. MLI are designed with series and parallel combinations of semiconductor switches which helps in generating the AC output [3]. Conventional topologies have high component requirement when operated for high-level output.

For example, in case of 5-level output, eight semiconductor switches are required and it goes on with 4 switches per odd levels. This paper proposes 19-level topology which in conventional design has 36 switch requirements. This makes the system very complex and uneconomical also its performance degrades with each component contributing to the losses and voltage drop across each switch. Hence need for the reduced count topology is required which has high performance efficiency, low THD and compact modular design [4, 5]. These topologies make it possible to use the device effectively and simplify the overall system design compared with available conventional designs. Several topologies have recently been proposed to reduce the number of devices in multilevel inverters. In this work modular cascaded topology is presented for 19-level output. In which only 12 switches are required to design the single-phase MLI topology with 4-DC sources.

In this work SGU is designed for single phase system. The interfacing of the SGU is done using 19-level Asymmetrical Cascaded Modular Topology (ACMT), ACMT is a Multi-Level Inverter

(MLI) with less switch count. MLI are the class of inverters where DC is converted into AC in small stepped output waveform.

II. SOLAR GENERATION UTILITY (SGU)

One of the most important renewable and green energy sources, solar energy is also a terrific source of energy and ecologically friendly technologies. It contributes significantly to the achievement of energy solutions for sustainable development. Thus, solar energy is a particularly appealing resource for producing electricity due to the enormous amount of energy that can be obtained every day. In order to meet our energy needs, both solar photovoltaics and concentrated solar power applications are constantly being developed. Thus, in the same context, a high installed capacity of solar energy applications globally benefits the energy industry and meets the demand for jobs to grow sufficiently. But its wide applications also required compatible inverter structures to incorporate the various usage and system configurations [6-9].

In this work 19-level inverter which required 4-solar system as the DC-source with different ratings are examined for single-phase system. The simulation analysis is carried out in MATLAB environment. A PV-array block is available in renewable library of simulink whose parameters are given in table-1. The solar connected across the asymmetrical structure has different DC-source and different polarity too. The first PV is connected with positive polarity and has the rating of 300W and 50 V with 1-series and 1-parallel array connection. The second PV is connected with negative polarity and has the rating of 300W and 50 V with 1-series and 1-parallel array connection. The third PV is connected with positive polarity and has the rating of 1200W and 100 V with 2-series and 2-parallel array connection. The fourth PV is connected with negative polarity and has the rating of 7500W and 280 V with 5-series and 5-parallel array connection. The DC-output voltage of all the four PV-block, which is regulated and boosted using DC-DC boost converter as shown in figure 1. The boost converter is tuned to regulate the DC-output of PV and the tuned parameters for LC components are given in table-1.

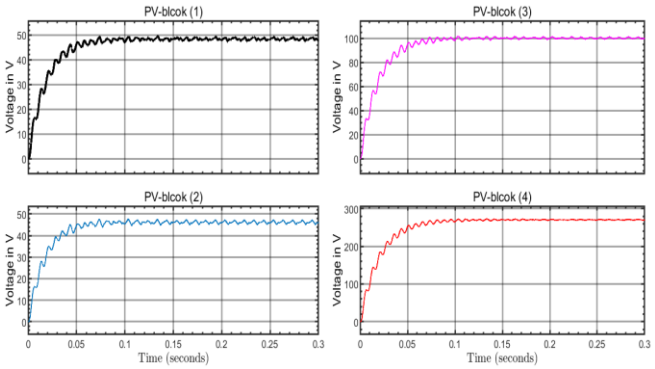

Fig. 1 DC-voltage output of boost converter

TABLE 1 Parameter used for solar cell:

Parameter	Value
DC-bus voltage	50 V, 50 V, 100 V, 280 V
Operating Irradiance I_r	1000 W/m^2
Quality factor, N	1.5
Series resistance, R_s	0
Energy gap, E_g	1.12
No of cell connected in series, Ns	4
No of cell connected in parallel, Ns	4
Cell reference Temp, T_{r0}	25^{0}C
Cell operating Temp, T_r	25^{0}C
V_{oc} for module	64.2 V
I_{sc} for module	5.96A
Boost converter capacitance	900 µF
Boost converter inductance	2 mH
Boost converter resistance	1 mΩ

III. REDUCED COUNT MLI TOPOLOGIES

The lowered total by adjusting the number of levels with fewer switching devices, their triggering circuits, diodes, capacitors, and other components, MLI has reduced the harmonics in the output voltage waveforms [10, 11]. To generate a multilayer output, these topologies need one DC source or multiple separate DC sources. The topology of several sources might be either symmetric or asymmetric. Every DC-source in a symmetric topology has the same magnitude, but every DC-source in an asymmetric topology has a distinct magnitude. In actuality, DC-sources in symmetric topologies may vary because of PV panel shading or varying battery charging statuses. Battery balancing systems solve these issues [12-15]. Figure

2 classifies the many reduced count topologies that have been developed recently. Figure 2 presents the classification of all the reduced count topologies available in literature. The nomenclature for these are presented in table-2. From the classification it can be seen, that for designing reduced count topologies cascaded inverters are the preferred choice, since they are modular in structure.

The Modular Cascaded MLI (MC-MLI) has successive series parallel combination and in each row DC-source is connected across the two switches [16-18]. For conventional topology, a constant DC-source is required with equal value. In the proposed topology asymmetrical cascaded design is used, where all the cascaded units are not symmetrical to each other [19]]. The schematics of the proposed topology is presented in figure 3 and the comparison between the proposed and the conventional topology is demonstrated in table 3. In this work level shifted Sinusoidal PWM technique is used to design the driver circuit for the switches of the MLI. In this type of PWM technique a carrier wave is sinusoidal wave and the modulated wave is triangular wave. The frequencies of the modulated wave is shifted in multiple of 2 whereas for carrier wave a fixed frequency particularly fundamental one is considered [20- 22].

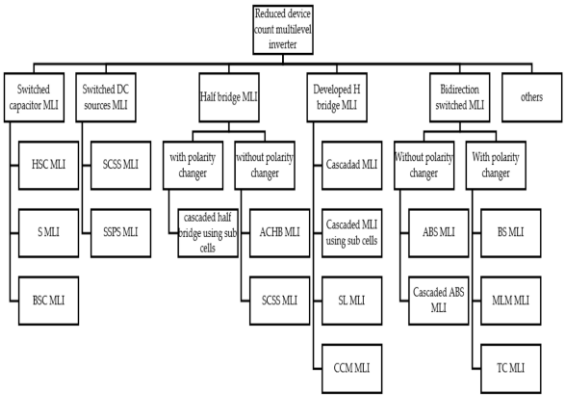

Fig. 2 Classification of reduced count MLI topologies

TABLE 2 Nomenclature for various reduced count MLI topology

Parameter	Value
HSC-MLI	hybrid-switched capacitor
S-MLI	sub-multilevel inverter
SSC-MLI	switched capacitor converter
SSPS-MLI	switched-series-parallel-sources
ACHB-MLI	asymmetric cascaded half-bridge
SL-MLI	switch ladder
CCM-MLI	cascaded compact module
ABS-MLI	asymmetric bidirectional switch
BS-MLI	Boost switched capacitor
MLM-MLI	multilevel module
TC-MLI	transistor-clamped

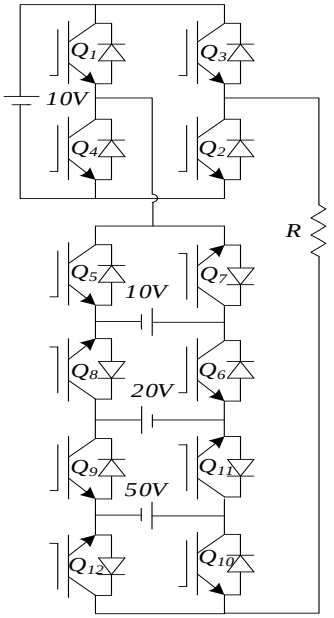

Fig. 3 Schematic of Proposed reduced count 19-level inverter topology

TABLE 3 Comparison of conventional and proposed reduced count19-level inverter

Parameter	Topologies	
	Conventional 19-level	Proposed 19-level
Configuration	Symmetrical	Asymmetrical
No. of switches	36	12
DC-sources	9	4
THD %	3	0.94

IV. SIMULATION RESULTS

This paper presents a lesser switch count 19 level inverter. Although the presented 19-LI resembles H-bridge, the inverter has less components than a conventional 19-level H-bridge inverter. The proposed reduced count topology is a multiple voltage level inverter with unsymmetrical blocks and 4 different level DC sources. There are 12 switches in the current scheme. To examine the various voltages under load at different intervals, each of the 12 switches must receive a unique pulse. The output waveform generated is shown in figure 4

and the THD with battery as DC-source is shown in figure 5 which is very low of the order of 0.32 %. The proposed reduced count inverter is designed for solar integration. Hence the DC-battery source is replaced by the PV-block. The voltage and current waveforms for the PV-connected 19-level reduced count inverter are shown in figure 6 and figure 7 respectively. The voltage THD graph for the system designed is shown in figure 8 which is 1.48 %. The proposed topology does not require any filter unit and the THD percentage shows that the generated output is AC resembling sine wave hence reducing the burden on the system as well as component requirement.

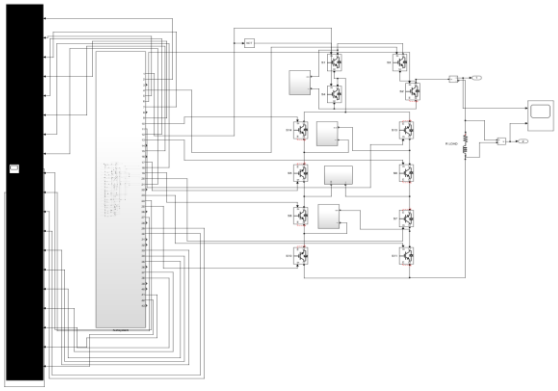

Fig. 4 MATLAB simulation model of proposed reduced count 19-level inverter with solar integration

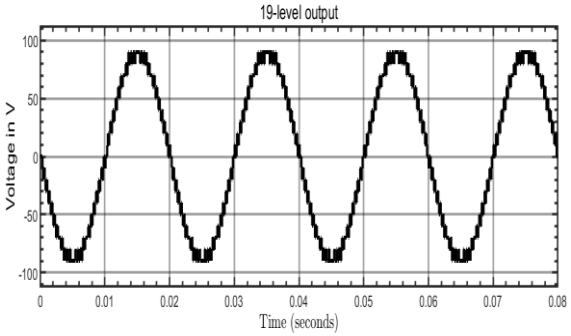

Fig. 5. Output voltage of 19-level proposed MLI

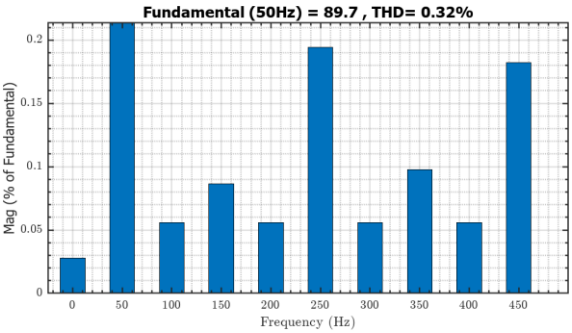

Fig. 6. THD of voltage of 19-level reduced count inverter

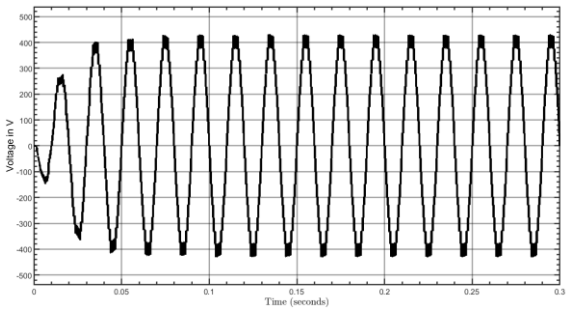

Fig. 7. Sinusoidal Output voltage of 19-level proposed reduced count inverter

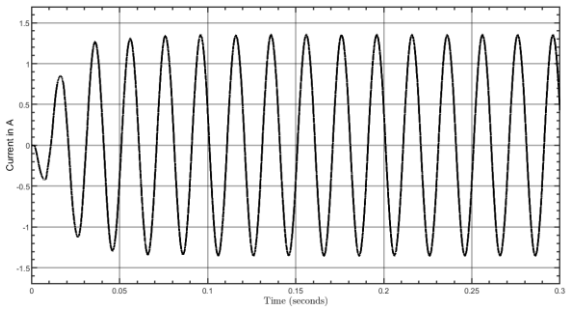

Fig. 8. Sinusoidal Output current of 19-level proposed reduced count inverter

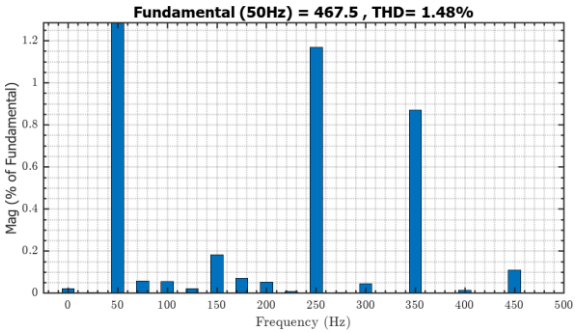

Fig. 9. THD of voltage for 19-level reduced count inverter with solar integration

V. CONCLUSION

A solar system with grid integration is presented for single phase utility system. For generating AC output a reduced count 19-level inverter is designed. The single-phase AC-output is designed for 465 Voltage which can be supplied for single-phase distribution supply. The THD in the voltage waveform is 1.4 % without any filter unit. Hence the designed inverter can be utilized in transmission system. More-over, the reduced count topology has very low component count and simple in design. This makes the system very efficient and can be used for very precise applications.

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