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RESEARCH ARTICLE OPEN ACCESS

An asymmetrical Cascaded 19-Level Inverter with Reduced Switches Count Using Phase Shift Frequency Modulation

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ABSTRACT
An expansion of inverters to more than two layers to reduce distortion from the simple sinusoidal waveform is where the concept of a multilayer inverter arose. The incorporation of additional switches, which increases system size and expense and lowers system dependability owing to the increased component count, is a disadvantage of using multiple level inverters. When compared to a symmetrical H-bridged nineteen-level inverter, a nineteen-level inverter (19-LI) with fewer switches is provided in this work to rectify the problem of system becoming bulkier, costly and less reliable with less distortion. The sinusoidal carrier wave frequency modulation technique is used to control the gating of the switches. The MATLAB platform is used to build the concept, and the results are obtained under various loading condition and change in modulation index.
Keywords - 19-Level Inverter (19-LI), Pulse Width Frequency Modulation (PWFM), Modulation Index (MI), Sinusoidal Carrier Wave, Total Harmonic Distortion.

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I. INTRODUCTION

A power-electronic device known as an inverter converts direct current (dc) to alternating current (ac) power at a specified voltage and frequency [1-2]. Because it is a power electronic device with no moving components and a high switching ability, it is more reliable and efficient. An inverter is now more than just a DC-AC converter; rather, it is a crucial component of the electrical industry. Since a fundamental inverter only has two levels, the output wave of a basic sine wave with the same period and frequency is somewhat distorted. This affects the overall efficiency of the system by increasing the likelihood of a failure and adding harmonics to the circuit [3], [4]. Harmonics are detrimental to both the load and the power system overall because they result in distortion and system heat. As a result, the concept of a multilayer inverter—in which the inverter's levels are increased to lessen the distortion of the outgoing wave—was invented. As the level increases, the output wave becomes more sinusoidal, lowering the harmonic content [4]– [6]. Multilevel inverters are devices that monitor the voltage across the load and determine the levels using DC voltage sources. Furthermore, the circuit is completed via several paths in a single full wave cycle for variable periods by using different switching configurations. Higher harmonic distortion is a disadvantage of dual level inverters, although this may be avoided by using multiple level inverters.

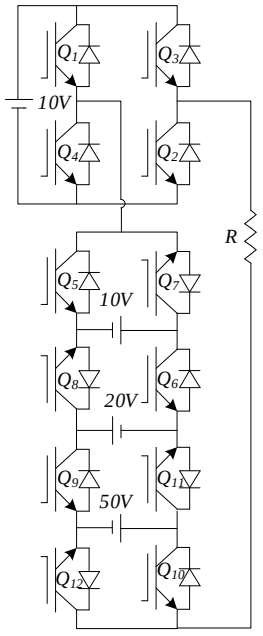
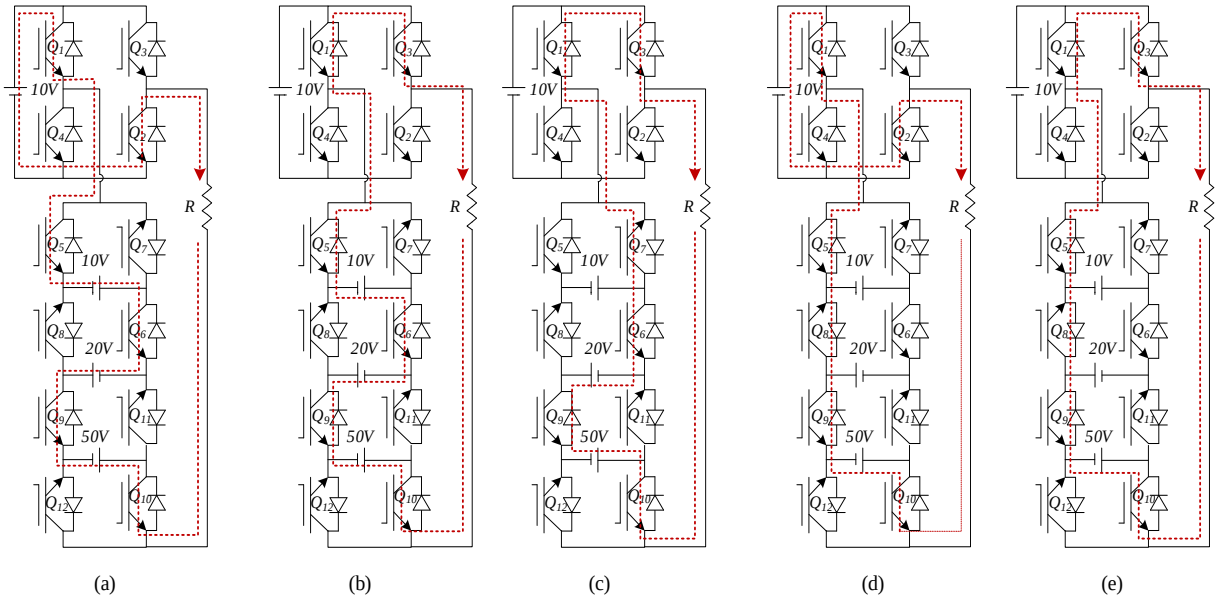


Fig. 1 Presented 19-LI

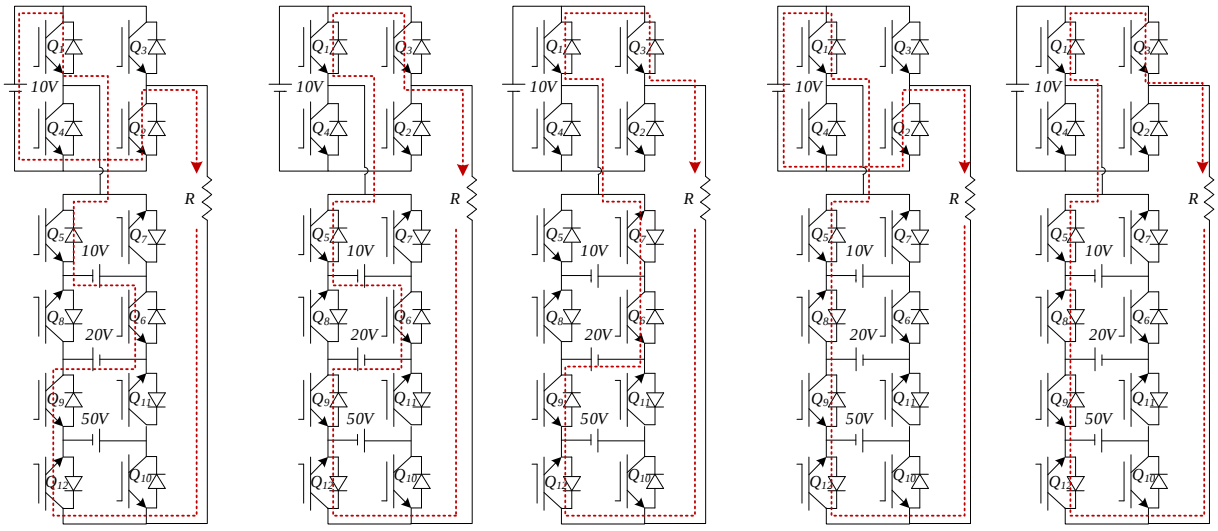
This piece of art presents a lesser switch count 19 level inverter (19-LI). Although the presented 19-LI resembles H-bridge, the inverter has less components than a conventional 19-level H-bridge inverter. Figure 1 depicts a multiple voltage level inverter with two symmetrical blocks and 4 different level DC sources. There are 12 switches in the current scheme. To examine the various voltages under load at different intervals, each of the 12 switches must receive a unique pulse. In conventional 19-level cascaded topology, for generating 19-level 36 switches are required. In order to ensure that the required voltage is available during load, this system's control is developed with KVL in consideration.

In this part of article, the working of presented 19 level inverter is explained in details.

Four voltages used to verify this topologies are 10V, 10 V, 20V, and 50V so the different levels of voltages for this inverter are +90 V, +80V, +70V, +60V, +50V, +40V, +30V, +20V, +10V, 0V, -10V, - 20V, -30V, -40V, -50V,-60V,-70V,-80V, -90V. In order to elaborate the presented inverter's working. All seven modes are elaborated as under and the network explaining all the nineteen level in Fig.2 (a)-(s). The levels are controlled via gating signals generated with the help of phase-shift frequency modulation.


Q1
Q3
10V
Q4
Q2
R
Q5
10V
Q7
Q8
20V
Q6
Q9
50V
Q11
Q12
Q10

(a) (b) (c) (d) (e)


Q1
Q3
10V
Q4
Q2
R
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Q9
50V
Q11
Q12
Q10

(f) (g) (h) (i) (j)

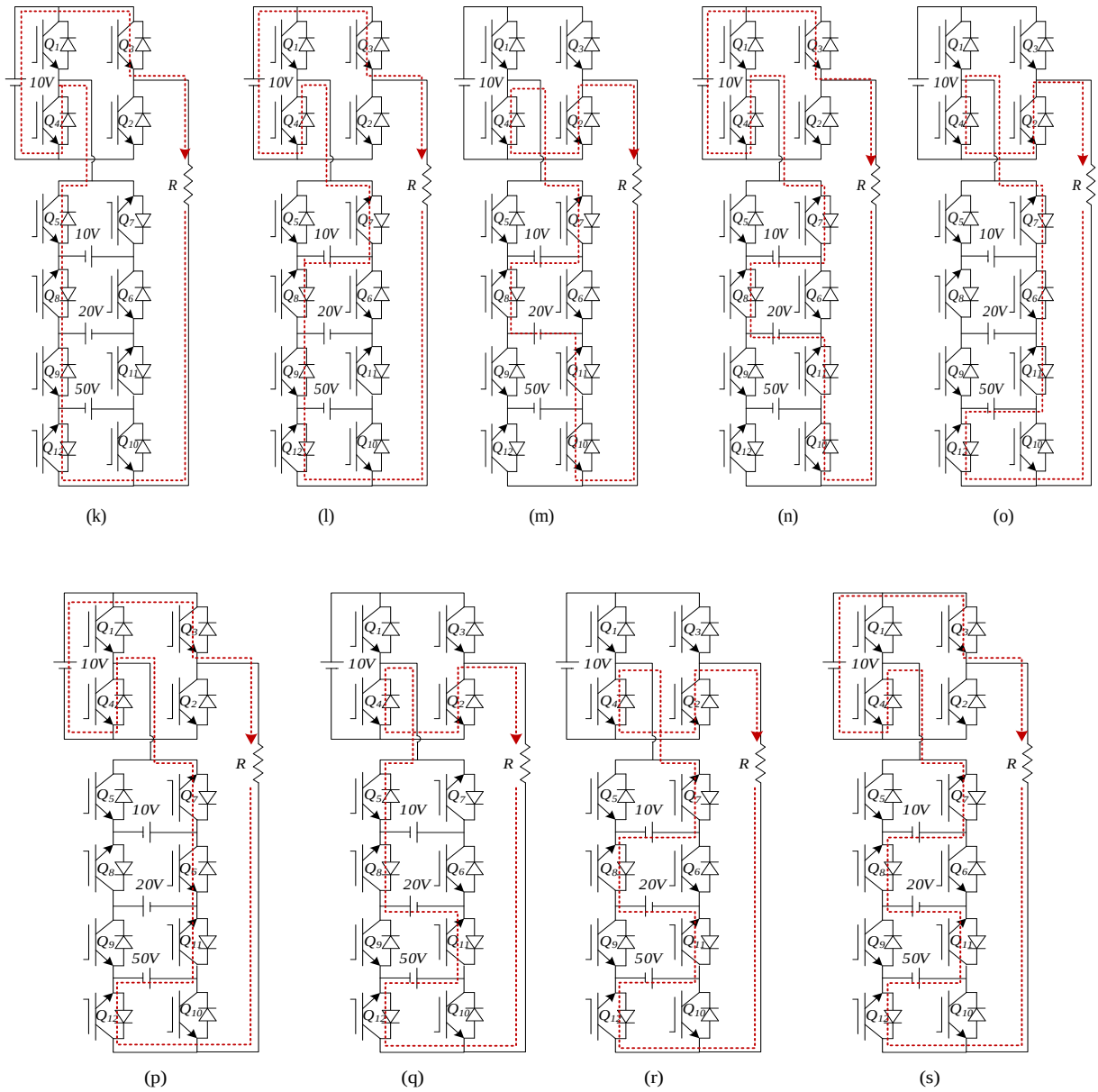

Fig.2 A 19-level inverter working during different load voltage levels (a) +90V, (b) +80 V,(c) +70 V, (d) +60V, (e) +50V, (f) +40V, (f) +40V, (g) +30V, (h) +20V, (i) +10V, (j) 0V, (k) -10V, (l) –20V, (m)-30V, (n)-40V, (o)-50V, (p)-60V, (q)-70V ,(r)(-80), (s)-90V.

[1] Mode A- During mode-A, switches active are Q10, Q9, Q6, Q5, Q1, and Q2. The Kirchhoff's rule for voltage is followed and the potential across load is measured to give + 90 V.

[2] Mode B- During mode-B, switches active are Q10, Q9, Q6, Q5, Q1, and Q3. The Kirchhoff's rule for voltage is followed and the potential across load is measured to give + 80 V.

[3] Mode C- During mode-C, switches active are Q10, Q9, Q6, Q7, Q1, and Q3. The Kirchhoff's rule for voltage is followed and the potential across load is measured to give + 70 V.

[4] Mode D- During mode-C, switches active are Q10, Q9, Q8, Q5, Q1, and Q2. The Kirchhoff's rule for voltage is followed and the potential across load is measured to give + 60 V.

II. PROPOSED WORK

The current approach makes use of the phase opposition deposition level shifted pulse modulation technique to enhance the observed

waveform's sine character at load as shown in Fig.3. Several level-shifted waves with 180 degree phase differences are used in the phase deposition approach to get interception with an ideal sine wave for the extraction of the gate pulse for the 19-LI. Figure 3 displays the waveform for inverter control with the same phased, level-shifted pulse width modulation.

Though numerous topologies for multi-level inverter with reduced switch count has been cited in literature [7-10], but either they are cost efficient or have low harmonic content. Both benefits are rarely obtained. [11] presents a modified cascaded topology which can be applicable to 11/15/19 level with reduced switch count. But it can handle low voltages only. [12] presents 11-level topology with reduced count as well as harmonic analysis is also presented. But the results are presented with static loading condition with change in modulation index. This paper presents a comparative analysis of asymmetrical 19-level topology designed via cascaded inverter presented in [13]. The comparative analysis for both the topologies is presented in table-1. In [13], though component count is reduced as compared to the conventional 19-level topology, but it uses multiple types of component, which makes the system complex as well as it has high harmonic component.

In the proposed topology, though switch count is higher then [13], but it does not uses any other component except Dc-source. Also, Harmonics are negligible and the output voltage waveform obtained is nearly sinusoidal. Reduced harmonics in MLI topology is very important since it assists the power quality conditioning when applied to design power conditioners like Dynamic Voltage Restorer (DVR) [14] and Unified Power Quality Conditioners (UPQC [15].

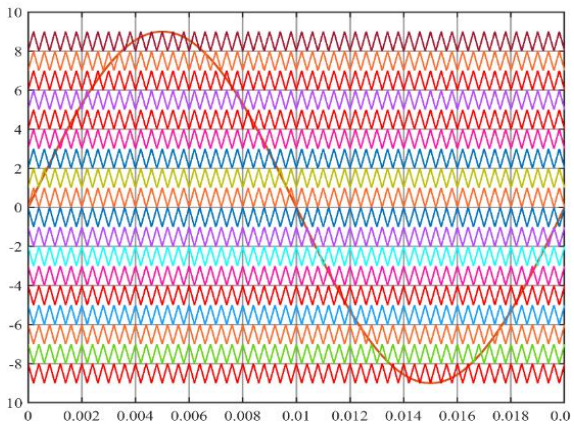

Fig.3 Phase opposite level shift deployed PWM scheme

Table-1 Comparison of the 19-level MLI topology

Parametres	Asymmetrical 19-level topology	Proposed topology
Number of level	19	19
Voltage level	160V	160 v
No. of DC-source	3	5
No. of switches	9	12
No. of diodes	6	Nil
No. of Capacitors	2	Nil
Sample Time	10 µs	50 µs
Switching frequency	5 kHz	5 kHz
Output frequency	50 Hz	50 Hz
Resistive load	R = 300 Ω, 150 Ω	R = 300 Ω, 150 Ω
Resistive-Inductive load	R = 300 Ω, L = 22 mH	R = 300 Ω, L = 22 mH
THD	7.22%	0.94%

III. RESULTS

The output wave shape of the phase deposition level shifting pulse breadth modulation method using a 19-LI is shown and described in this section. The gating signals for all the 12 switches are shown in figure 4. The proposed topology has been analysed for four cases;

- Case-1; Z=300Ω from 0.01-0.05 sec and 150 Ω, from 0.05-0.1 sec.
- Case-2; Z=300Ω from 0.01-0.05 sec and 150Ω +200mH, from 0.05-0.1 sec.
- Case-3; Z=300Ω for Modulation Index (MI) 1.
- Case-3; Z=300Ω for MI 0.5.

The degree of modulation applied to a carrier signal is measured by the MI. The ratio of the modulating signal's amplitude to the carrier signal's is known as amplitude modulation. In this paper amplitude for carrier wave is taken as 9, hence MI can be calculated using equation (1);

$$MI = \frac{A_M}{A_C} \quad (1)$$

Where; A_M is the amplitude of modulating signal and A_C is the amplitude of carrier signal. The output voltage waveform for all the four loading conditions are shown in figure 5 and figure 6 presents the current output. The THD graph with the output

waveform for 300 Ω constant load with 1 MI is shown in figure 7.

When compared to asymmetrical 19-level inverter of the base paper, THD is 7.22% which is very. With the proposed 12 switches MLI, THD is only 0.94%. this shows that the proposed topology is highly efficient.

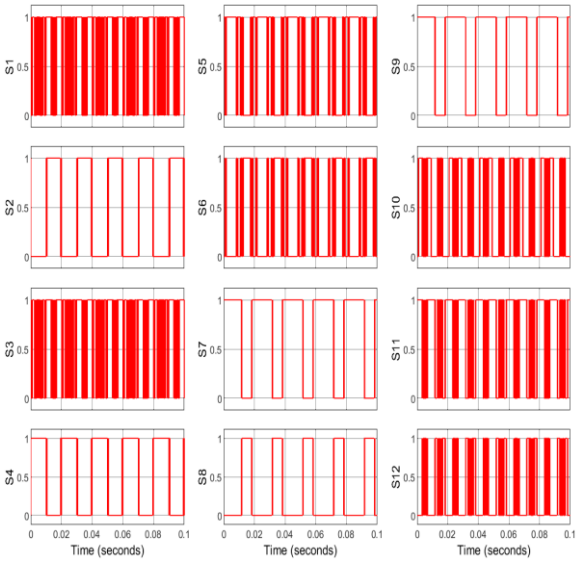

Fig. 4 PWM graph

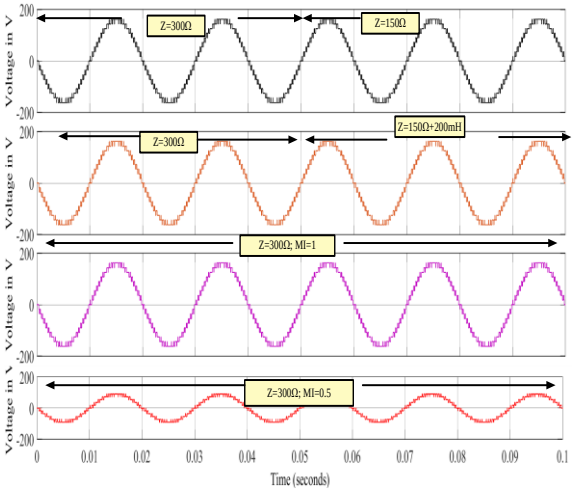

Fig. 5 19-LI voltage outcomes for all the four loading conditions

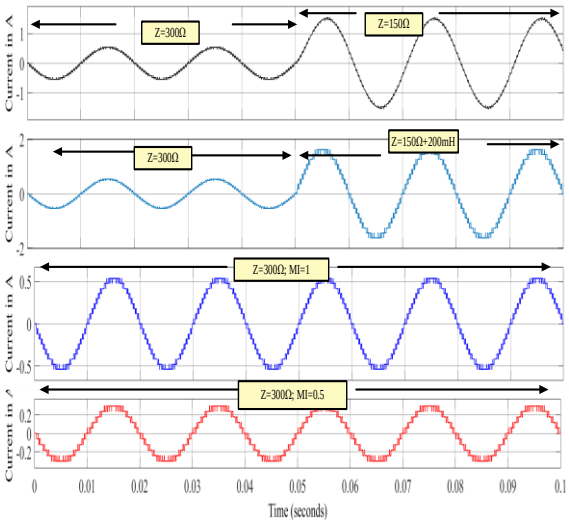

Fig. 5 19-LI Current outcomes for all the four loading conditions

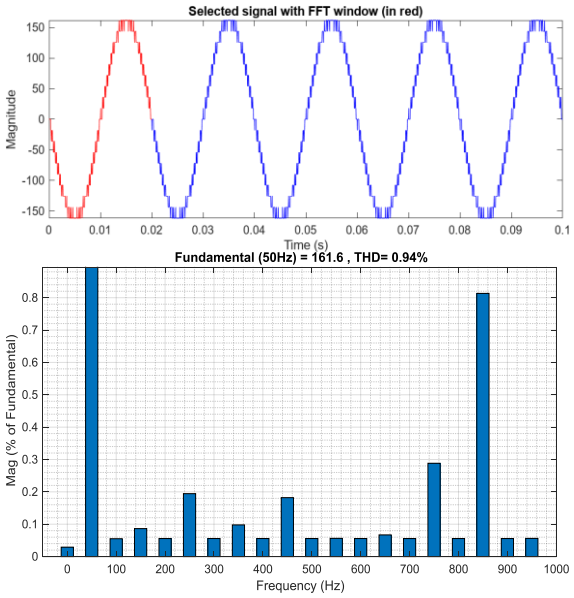

Fig.5 THD Profile

IV. CONCLUSION

This paper presents symmetrical topology of 19-level cascaded inverter with reduced switch count. The proposed topology of MLI is designed with 12 switches and the gate pulses for the switches is designed using sinusoidal carrier wave phase shift pulse width modulation technique. In total 4 DC sources are connected across the modular structure of the 19-level inverter. The first two dc sources are same, third one is the twice of the first two and the fourth one is five times of the first one. The obtained 19-level has lowest harmonics of 0.94% with respect to the fundamental frequency. Hence suitable for precise applications.

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