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A Survey of Low Voltage and Low Power Amplifier Topologies

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ABSTRACT:
Although lowering the voltage supply is an excellent strategy for conserving energy, it also presents difficult decisions for analogue designers. The advantages and potential uses of many distinct topologies that are well-suited for low voltage and ultra-low voltage supply are detailed and compared in this study. All of the designs are implemented using the industry-standard 180 nm technology.
Keywords: amplifiers; CMOS integrated circuits; ultra low voltage; bulk-driven amplifers; inverter-based amplifiers; rail-to-rail amplifiers

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I. Introduction

The voltage supply may be lowered, which is one of the most efficient methods of power conservation. However, low and extremely low voltage design provide unique difficulties, particularly for analogue circuits. There has been and continues to be a lot of effort put into satisfying the needs of DC gain, bandwidth, and slew rate, all of which are constrained by the low voltage state, with the operational transconductance amplifier (OTA) being the most prevalent and utilised block. For instance, due to insufficient voltage headroom, cascading is prohibited. As a result, analogue designers are using unconventional circuit topologies such inverter-based amplifiers [1–5], bulk-driven and self-cascode topology [6,7], hybrid-mode input stage [8,9], and rail-to-rail amplifier with cross-coupled output stage [10,11]. In this study, we examine and evaluate these innovative topologies while maintaining the same industry-standard 180 nm CMOS technology. In addition, a low-voltage supply-specific nMOS-only amplifier design [10] has been validated. There is a clear structure to the document, which goes as follows: Amplifier designs will be shown in Section 2, simulated and contrasted in Section 3, with benefits and potential applications discussed in Section 4, and conclusions given in Section 5.

II. Amplifier Topologies

Recent CMOS amplifier designs are shown in this subsection. Using the UMC Design Kit for CMOS technology, we scale and simulate the schematics (United Microelectronics Corporation) 180 nm.

2.1.Amplifier using Inverter Technology

Innovation scaling is beneficial for advanced circuits since it supports speed and diminishes dynamic power dispersal. To further complicate matters, the voltage supply is continually being lowered, which is a need for the analogue architecture.

The use of low-voltage analogue circuits that rely on inverters is becoming more popular in this setting. Recently published examples [1–5] show how inverter technology may be used to create OTAs. The first design is a current-starved speaker [5], the second is a three-stage inverter-based enhancer with feed-forward remuneration [4], and the third is a totally differential intensifier with a single inverter stage [1–3].

III. Tunable Inverter-Based Amplifier

The inverter-based enhancer is fundamentally indistinguishable from the CMOS computerized inverter, however it runs on a typical mode (CM) voltage that keeps the nMOS and pMOS semiconductors in their immersion locales. As a consequence, the dc gain and gain bandwidth are both maximised, while the transconductance and output resistance are both increased (GBW). It is true that the gain of the inverter stage may be represented as:

$$A_v = \frac{gmn + gmp}{gdsn + gdsp} \quad (1)$$

where gm is the trans conductance and gds is the little sign result obstruction rearranging constant. When the inverter is used as an amplifier, however, the dc gain and gain bandwidth (GBW) are very sensitive to temperature and process corners, which is a major drawback. Fortunately, inverter-based amplifiers may be tuned across process and temperature fluctuations using a straightforward circuit method. Figure 1 shows a conceptual schematic of the inverter-based amplifier, and [1 provides a thorough explanation of the amplifier's operation.

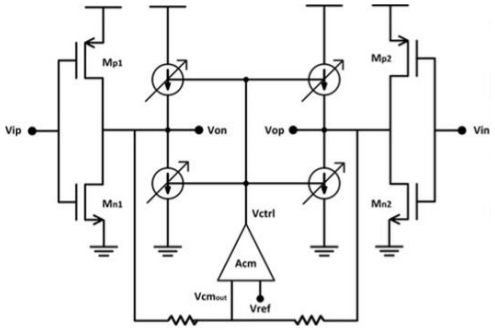

Figure 1 shows an amplifier that uses a tunable inverter.

Essentially, the tuning method consists of a CM feedback (CMFB) circuit that uses four regulated current sources to regulate the current flow through the inverter based on the measured output CM voltage. In fact, the inverter topology's common mode (CM) output voltage is also the drain-to-source voltage drop (Vds), which has a significant impact on the tiny signal parameters gm and gds. For a straightforward inverter-based OTA, settling the result CM likewise balances out the dc gain, such that changes to the dc gain are constrained by shifts in the threshold voltage. By locking in the Vds of both the nMOS and pMOS transistors, the tuning circuit ensures that the OTA continues to operate reliably despite tiny dc-gain fluctuations across temperature and process corners. The actual tuning circuit construction is shown in Figure 2. Since there wouldn't be enough place for a tunable current source to be stacked inside the principal OTA without eating into the accessible voltage headroom, the ongoing sources that are under the order of the OTA are outside.

To the OTA yield semiconductors, a CMFB enhancer (Acm) is associated in equal. The OTA's CM is estimated against a reference voltage (Vref) set at a portion of the stockpile voltage utilizing the speaker Acm found in Figure 3. The nMOS and pMOS current sources are under the command of the amplifier's output (MI1–MI4). In either direction, the CMFB current sources might source or sink current into the essential OTA. An easy example of a pseudodifferential amplifier is the Acm amplifier. If the CM voltage at the output (Vcmout) is less than the reference voltage (Vref), then the control voltage (Vctrl) drops to a low value at a specific temperature and cycle corner. To draw Vcmout nearer to Vref, semiconductors MI3 and MI4 should source extra current into the essential OTA. At the point when Vcmout is more prominent than Vref, the inverse transformation takes place.

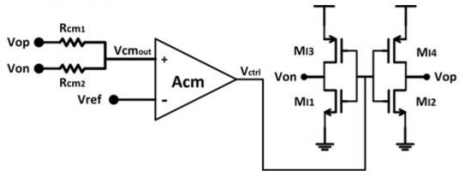

Figure 2 shows the CMFB's schematic.

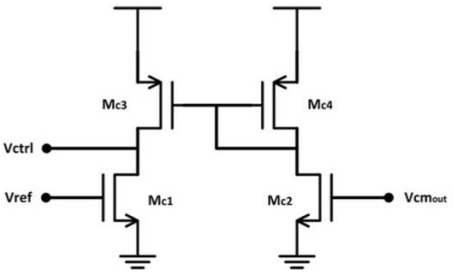

Figure 3. amplifier for acm.

The suggested circuit keeps the inverter-based amplifier's CM output unchanged without adding any more voltage headroom to the fundamental inverter plan. In this way, the low-voltage capability is realised.

2.1.1. Inverter-Based Amplifier with Feed-Forward Compensation

Using a different kind of inverter, [2] proposes and discusses a new amplifier design. Three stages are cascaded together with feed-forward rectification to create a good increase without lessening the accessible data transfer capacity. Figure 4 portrays the reasonable schematic, though Figure 5 portrays the excessively long schematic in more detail: The three-stage enhancer gives an addition of around (AO)3 at low frequencies, yet at high frequencies, the speaker just uncovers the increase of the single stage in the criticism circle, since route B is quicker (AF). So that everything is clear, here is the formula for the low frequency gain:

$$\frac{A^3}{\frac{\alpha + gm\ rds}{1+\alpha}}$$

where gm is the all out of the transconductances of the nMOS and pMOS gadgets, rds is the equal mix of the result protections of the nMOS and pMOS gadgets, and is the proportion between the calculation of the semiconductors in course B and the relating in way A. As was recently referenced, the inverter's AC properties (dc endlessly gain transmission capacity (GBW)) shift generally over temperature and cycle corners,which is a major negative when the inverter is employed as an amplifier. Since manufacturing, temperature, and power supply fluctuations all affect the CM voltage that the pMOS transistors operate at, a biassing circuit is added (displayed in Figure 6) to predisposition the n-well of the pMOS semiconductors, considering high increase at a proper CM voltage. To get the ideal phase margin, we adjust the number of transistors in each of paths A and B.

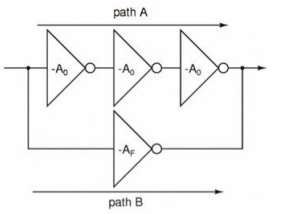

Figure 4 shows a conceptual design for an amplifier that uses an inverter and has feed-forward correction.

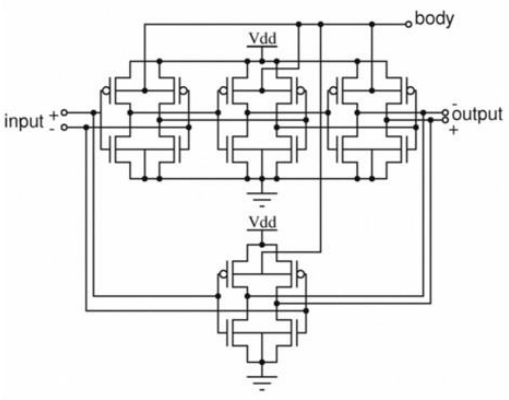

Figure 5. Three-stage amplifier with frequency compensation.

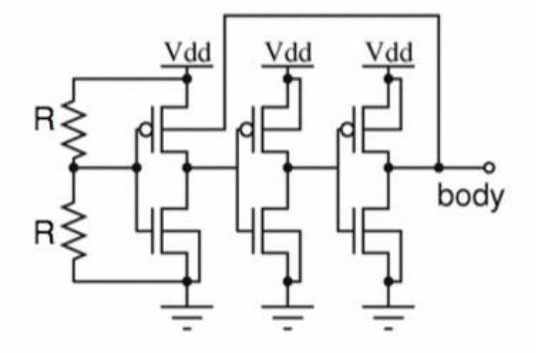

Figure 6 shows the N-well biasing circuit.

Current-Starved Inverter-Based Amplifier

Using an inverter-based architecture to construct an amplifier that can operate off a very low voltage source is an appealing alternative. Low supply voltage implementations of inverter-based amplifiers force transistors to operate in the sub-threshold region, lowering bias currents, power consumption, bandwidth, and the amplifier's capacity to drive loads. To further reduce power consumption, it is suggested in [5] that the conventional inverter-based amplifier be modified by adding a couple of tail current sources (both N and P type) to the novel input stage. This considers more exact guideline of the ongoing through the inverters, which thus powers the semiconductors more profound into the sub-limit locale. By giving an additional contribution to well known mode criticism, the tail sources assist the speaker with upgrading its CMRR (Familiar mode dismissal proportion) and fix the issues with the inverter-based design. Also, the tail allows for the power utilization and information offset voltage to be controlled freely, allowing the inverters to be designed correctly to manage the offset voltage while the tail handles the total power output.

Figure 7 depicts the suggested architecture, which uses four extra load inverters to power the "active load" (M2, M3). As can be seen in Figure 7, M2 is connected in a cross-coupled plan, and the external sets of inverters (M3) is associated through diodes. The negative obstruction of 2/gm3 results from the cross-coupled pair's positive criticism. Diode-associated matches give a positive opposition of 2/gm2. The DC inclination steadiness for the info and cross-coupled inverter matches is given by this positive opposition, which likewise settles the negative impedance of the cross-coupling. Because of the presence of both positive and negative impedances, the dynamic burden circuit encounters a huge result impedance relative to the backwards of (gm2-gm3). Thus, we can

communicate the complete voltage gain of the enhancer's half-circuit as:

$$A_v = \frac{gm1}{gm2 - gm3}$$

to use transistors with relatively long lengths (usually more than 1 m) and high W/L ratios (generally more than 16)..

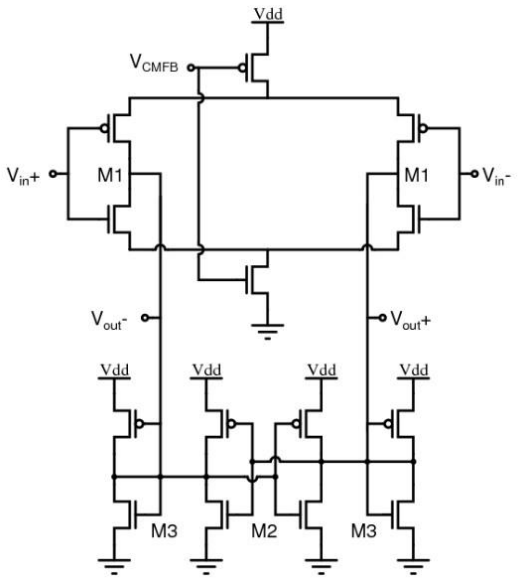

Figure 7. A current-starved amplifier built on an inverter.

2.2. Bulk-driven Ampliifer

An info differential pair, an electrical flow source, an electrically-dynamic burden, and a typical source stage are the fundamental pieces of a mass driven Mill operator speaker. Since the mass transconductance (gmb) is a fundamentally more modest sign boundary than the door transconductance (gm), increased by the result opposition, the endlessly gain transfer speed result of the mass driven geography are less concerning the regular entryway driven geography. The input signals in the bulk-driven Miller OpAmp come from the differential pair's bulk rather than the gate, and the transistors' gates, sources, and drains are biassed by the corresponding voltages. The low power consumption and relatively low voltage supply required for biomedical applications make this method attractive. Furthermore, a big gain-bandwidth product is not often necessary for such applications. As an added bonus, the mass driven strategy permits the info stage to have a more extensive well known mode input range than the entryway driven design would somehow permit. In [11], we can see that the mass driven enhancer likewise has a lesser aversion to the Electromagnetic Obstructions. Nonetheless, in the event that the well known mode voltage is to some degree near the negative rail, just like with a P-type mass driven input stage, the circuit is said to have poor linearity. Since the active load begins to turn off while the differential pair is present, signal distortion is certainly produced. To a comparable degree, on the off chance that the well known mode voltage is close to the positive rail, the N-type input stage will act in much the same way. A dc moving on the sign might be accomplished by interfacing two batteries in series with the dynamic burden; this allows the active load to continue functioning at a constant voltage even when the input signal's magnitude decreases, hence solving the issue and avoiding non-linearity situations. It is possible to use a common-gate.

Without a doubt, in dc examination, the semiconductor in diode setup might be addressed by an opposition whose not entirely set in stone by the reverse of its transconductance, similar as a battery. In any case, in ac examination, the joined semiconductor Q3-Q4 is a functioning burden and gives an addition. Since this is the situation, in [6] we see a changed mass driven Mill operator enhancer with a composite collapsed dynamic burden. Since the composite transistor provides a higher gain compared to a single transistor without requiring more voltage headroom, it is a crucial arrangement for MOS transistors used in feeble reversal and for the most part for low voltage applications.

2.3. Hybrid Mode Amplifier

Likewise, a voltage controller is an essential simple structure part that depends on a mistake enhancer and a power semiconductor to drive the heaps. The primary difficulty is balancing a strong dynamic responsiveness with a low quiescent current in low voltage and low power applications. Because of this, the adaptive biassing technique is implemented, whose quiescent current is negligible in the no-load state and large in the high-load state. Because of this, a little overshoot occurs at the output at the point when the heap current changes from high to low. This is on the grounds that the more prominent peaceful current during high-load condition at first offers speedy charging of the entryway hub of the power semiconductor connected to the mistake enhancer. A bigger undershoot is provided by the low quiescent current for the transient transition from low to high load because of the power transistor's gate node's sluggish discharge. In order to do this, a hybrid-mode operational transconductance amplifier (HM-OTA) has been developed; this OTA has a rapid

discharge slew-rate, an excellent dynamic response, and does not need any extra silicon area or power to realise. Comparison of the hybrid-mode amplifier's architecture with that of the common-mode (CM-OTA) and differential-mode (DM-OTA) OTAs illustrated in (a) and (b) may be seen in Figure 9c, which is shown in [8].

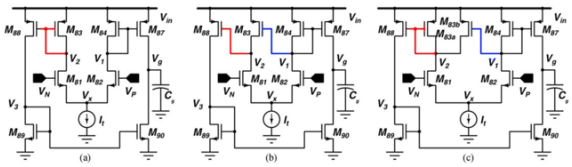

Figure 9. Schematics of CM-OTA (**a**), DM-OTA (**b**), HM-OTA (**c**).

The first of them is the common-mode amplifer (Figure 9a), which, owing to its single-pole nature, makes frequency correction simpler and is therefore a viable option for incorporating the error enhancer into the voltage controller. Every one of the inside hubs have a low impedance, consequently the dc gain is exceptionally low. Likewise, the charging/releasing slew rate is symmetric and reasonably constrained for big signal operation. In case you were wondering, the CM-gain OTA's Av is roughly provided by :
since it functions in a similar way to an amplifier with a single gain stage. As shown in Figure 9b, a typical differential-mode OTA (DM-OTA) is the preferable design because it offers both high dc gain and unbalanced slewing activity in huge sign circumstances. ZAcquire Av is, truth be told:
it's the gain of a two-stage amplifier. Low quiescent current and a tiny amount of output compensating capacitor provide a stability problem for the regulator due to the high impedance from the inward hub. Steadiness might be reestablished by expanding the worth of the result capacitor. Joining the CM-OTA with the DM-OTA, as represented in Figure 9c, results in the hybrid OTA (HM-OTA), which benefits from the features of both designs. The M83 transistor differs from the CM-OTA in that it consists of two distinct pieces, M83a and M83b. In addition, the proposed HM-OTA has the gate of M83b linked to node V1 rather than node V2. The delta/difference currents of I81 and I83b are routed via I83a as a result of the differential stage formed by this alteration. For the HM-OTA to keep its dc current balanced, the M84:M83b and M83a:M83b ratios are set at 1: and (1-):, respectively. Since 0 1, the HM-OTA is the product of the xCM-OTA and the (1)xDM-OTA. In this situation, the difference benefit is:

this is the increase of a one-stage enhancer that has been upgraded. Presently we discuss the large number rate execution of the proposed HM-OTA. Charging slew rate SR+ is tantamount to that of customary CM-OTA/DM-OTA during enormous sign activity. The tail current is carried entirely by M81 and M83a while the other transistors, M82, M84, and M83b, are turned off during the discharging procedure. Since M83a is wider than M88, the negative SR is greater than that of a regular CM-OTA by a factor of 1/(1). While HM-SR-value OTA's is lower than that of regular DM-OTA, the last option actually presents a security issue for the controller, as was recently demonstrated. Controlling the dc gain, circle data transfer capacity, slew rates, and circle dependability with the worth of is the vital advantage of the HM-OTA over the CM-OTA and the DM-OTA. Additionally, this adjustment doesn't call for any extra room or quiescent current.

IV. Results and Comparison

Typical UMC 180 nm CMOS technology has been used for sizing and designing all of the aforementioned designs. A schematic representation of the layout that is comparable to its extracted view has been simulated. As a mature technology with a solid set of design tools, the UMC 180 nm process is extensively adopted for usage in analogue design. It includes ordinary furthermore, low edge, triple-well nMOS (notwithstanding the mass gadgets) and a zero limit nMOS semiconductor, as well as gadgets for medium and low voltage supply (3.3 V and 1.8 V, individually). This technique includes high-resistance poly and metal-metal capacitors, as well as six different metal levels. The Figure of Merit (FOM) for a classical amplifier has also been analysed alongside the most important AC properties. To avoid any misunderstanding

IV.1. Tunable Inverter-Based Amplifier

The intensifier's customizable inverter depends on standard semiconductors from the UMC 180 nm innovation, with an ostensible limit voltage of 340 mV (for the N-type semiconductors) and 500 mV (for the P-type semiconductors) (for the P-type).Accordingly, a 1 V supply voltage, denoted Vdd, is used to power the circuit. The suggested amplifier, which utilises the CMFB circuit, is looked at against a clear inverter-based completely differential stage for the reason of thoroughness. The latter has pMOS transistors with dimensions of 350 m x 2 m x 2 m, and nMOS transistors with dimensions of W = 100 m x 2 m x 2 m. Table 1 instead provides the transistor values for the CMFB-based inverter amplifier.

Table 1 shows the transistor sizes for the Figure 1 Tunable Inverter-based Amplifier.

	Width [µm]	Lenght [µm]	Finger Number
Mn1, Mn2	100	2	10
Mp1, Mp2	350	2	24
Mi1, Mi2	4	2	2
Mi3, Mi4	16	2	2
Mc1, Mc2	1	4	2
Mc3, Mc4	4	4	2

Simulating and comparing the basic inverter-based amplifier and the amplifier with CMFB reveals that they have extremely comparable nominal AC characteristics, which are shown below. a gain of 45 dB, a GBW of 200 MHz, a phase margin of 80, and a cutoff frequency of roughly 1.5 MHz. The power consumption of each amplifier is comparable, at 129 W for the essential intensifier and 134.5 W for the CMFB-prepared model. The CMFB intensifier circuit shows gotten to the next level performance when taking process and temperature change into account, and the amplifier's common mode range is roughly 100 mV, which is much wider than the 9 mV scope of the essential inverter-based speaker. Via delineation, while considering corner examination, the addition of the speaker with CMFB is consistently north of 40 dB, yet the fundamental enhancer doesn't work in one corner condition. A comparative end turns out as expected when the temperature is modified in the scope of 40 C to +80 C. Subsequently, we might presume that the enhancer in view of the flexible inverter is a more dependable circuit than the fundamental one. The inverter-based intensifier with CMFB takes up a last design area of approximately 120 m 40 m, and its processed FOM is of 1.6.

IV.2. Inverter-Based Amplifier with Feed-Forward Compensation

The inverter-based enhancer with feed-forward revision has been built for a 1.2 V voltage supply to test its suitability, however its presentation has likewise been evaluated for endlessly lower Vdd (down to 0.4 V). With a length of 240 nm, a pMOS width of 18 m, and a nMOS width of 6 m, the three inverter phase of course A has been optimised for size. The dimensions of the B path inverter stage are as follows: length = 240 nm, width = 270 m, and width = 90 m for the nMOS. R is 10 k, all transistors are once again 240 nm in length, the pMOS width is 24 m, and the nMOS width is 6 m in the mass voltage reference circuit.

The whole circuit design takes up a space of roughly 60 µm × 40 µm.

The extracted layout's equivalent circuit has been simulated for Vdd values between 0.4 V and 1.2 V, with the well known mode held consistent at Vdd/2. The qualities for gain, gain-transfer speed item, and stage edge (PM) are displayed in Table 2. The endlessly gain data transfer capacity are additionally shown versus the voltage supply in Figure for ease of viewing.

The chart shows that the amplifier performs effectively even when powered by a very low voltage source, and it's important to remember that these simulations were run using the same amplifier design (the one designed for 1.2 V) without making any changes to the dimensions or layout. The FOM was calculated using1.2 V of Vdd, and the outcome was 4.24. At last, a corner study was completed under the ostensible Vdd state, where the increase shifts by only 4 dB and the GBW remains reliably more than 10 GHz with a sound stage edge. This intensifier's medium addition and very wide transmission capacity make it ideal for low-voltage, high-data-rate applications like capturing and processing biological images.

Table 2. Main AC characteristics.

Vdd	Gain	GBW	PM
0.4 V	8.8 dB	0.6 GHz	120°
0.5 V	49 dB	2.5 GHz	46°
0.6 V	58.6 dB	5.3 GHz	18°
0.7 V	52.9 dB	8 GHz	30°
0.8 V	48.8 dB	9.9 GHz	39°
0.9 V	45.7 dB	11.5 GHz	48°
1 V	43 dB	13.1 GHz	55°
1.1 V	41 dB	14.2 GHz	60°
1.2 V	39.6 dB	15 GHz	65°

IV.3. Current-Starved Inverter-Based Amplifier

The amplifier, which is based on a current-starved inverter, was developed using UMC's 180 nm technology. For this design, a nominal voltage supply of 1.1 V was used, and a 15 pF capacitive load was chosen as the minimum driving capacity at 1.1 V Vdd. The capacity to reject common-mode signals and a stable voltage gain are other necessary. Additionally, the power need must be less than few tens of microwatts (W). Table 3 provides information on the aspects of the semiconductors.
The circuit configuration takes a space of around 40 m 40 m. It was taken out, and the recreated enhancer shows an increase of 53 dB, a GBW of 3.6 MHz with a stage edge of 90, a CMRR of 233 dB, and a power utilization of 21 W.

Table 3 shows the transistor size for Figure 7's Current-Starved Amplifier.

	Width [µm]	Lenght [µm]	Finger Number
nMOS1	2	1	2
pMOS1	4	1	8
nMOS2	2	4	4
pMOS2	1	2	2
nMOS3	3	3	6
pMOS3	1	2	2
N-CMFB	5.5	7.5	1
P-CMFB	3	1	1

It was further investigated by simulating the same amplifier (with the same transistor sizes) under various biassing situations, in particular with a voltage supply of 0.9 V and 0.7 V, to see how it might do in ultra-low voltage applications. Therefore, Table 4 summarises the most salient features of the amplifier under varying power supply voltages. Based on the data in the table, it seems that this amplifier exhibits acceptable behaviour even when fed a very low voltage. Furthermore, the figure of merit (FOM) is 1.93 for 0.7 V Vdd, 3.45 for 0.9 V Vdd, and 2.87 for 1.1 V Vdd, depending on the magnitude of Vdd.

IV.4. Bulk-Driven Amplifier

For the UMC 180 nm CMOS technology, the bulk-driven amplifier presented in [6] has been scaled down to meet the following specifications: a voltage supply of 0.5 V, a gain of 30 dB or more, a GBW of 100 kHz and a 10 pF capacitive load. Table 5 lists the dimensions of the amplifier using Figure 6 as a reference.

Table 5. Semiconductors' estimating of the Mass driven Enhancer in Figure 6.

	Width [µm]	Lenght [µm]	Finger Number
Q1, Q2	2.4	0.6	2
Q3a, Q4a	1.5	0.6	2
Q3b, Q4b	4.5	0.6	2
QP, Q5	2.4	0.6	2
Q6	6	0.6	2
Q7	12	0.6	2
Q8, Q9	1.8	0.6	2

In addition, a biassing current of 140 nA has been selected, CC is set to 1 pF, and RC is optional for maintaining a healthy phase margin. The final configuration was retrieved and the comparable circuit was recreated, taking up an area of 50 m2 by 20 m2. In this section, we will briefly go over the amplifier's most important features. A 10 pF load brings about an increase of 36 dB, a GBW of 277 kHz, and a stage edge of 70. The enhancer's power utilization is 554 nW, and it displays amazing familiar mode and power-supply commotion dismissal; the CMRR is 75 dB, while the PSRR for both positive and negative power is close to 80 dB. As an added bonus, the FOM is 1.03. Because of its low power consumption and strong rejection of common mode signals and noise, this amplifier is ideal for use in biomedical applications that analyse physiological data at low to medium frequencies.

IV.5. Hybrid-Mode Amplifier

The 1.8 V nominal supply voltage for the UMC 180 nm CMOS technology used in [8]'s hybrid-mode amplifier design. The layout has been retrieved and replicated, and it was developed with matching difficulties in mind. When driving a 5 pF capacitive load, the corresponding circuit that was derived displays an increase of 45 dB, a GBW of 20 MHz, and a stage edge of 50. We've chosen a worth of 0.5 for the boundary. Thus, the large number rate is two times that of the CM intensifier and the recurrence conduct is better than that of the DM speaker. Since the well known mode input range is essentially rail-to-rail due to the exemplary differential pair in the regular info stage. The speaker's aspects are displayed in Figure 9 and Table 6.

Table 6. Transistors' sizing of the Hybrid-mode Amplifier in Figure 9.

	Width	Lenght	Finger
M81, M82	10	1	2
M84,M87,	90	1	4
M83a,	45	1	2
M89, M90	30	1	8

The last format possesses an area of 60 µm × 40 µm and the FOM is 1.21.

3.6. Rail-To-Rail Speaker with Cross-Coupled Result Stage

The cross-coupled yield phase of the rail-to-rail speaker was planned considering UMC 180 nm innovation. The plan limitations are the voltage supply of 0.5 V and the capacitive heap of 40 pF. The voltage gain must be in excess of 70 dB, the addition transmission capacity item should be more noteworthy than 10 kHz, and the power utilization should be under 1 W. Every semiconductor works in the frail reversal locale at an overdrive voltage of around 100 mV, and its aspects are displayed in Table 7 regarding Figure 10.

Table 7. Semiconductors' estimating of the Rail-to-Rail Enhancer in Figure 10.

	Width [µm]	Lenght [µm]	Finger Number
M1, M2	18	2	4
M3,M4	11	2	4
M5, M6	11	2	4
M7, M8	18	2	4
MN3a, MN3b	44	2	4
MP3a, MP3b	72	2	4
MB1a, MB1b	11	2	4
MB2a, MB2b	18	2	4
NM1, NM2	11	2	1
PM1, PM2, PM3	18	2	1

We have extracted the layout and simulated the corresponding circuit; it was meticulously developed taking matching difficulties into account

and takes up 160 m40 m. Due to the absence of Montecarlo models in the baseline design tool, a corner analysis was also conducted. The primary AC and DC parameters of the amplifier are shown in Table 8, demonstrating that it consistently meets the criteria.

Table 8. Corner examination of the Rail-to-Rail Speaker in Figure 10.

	Gain	GBW	PM	Power Consumption
TT	96 dB	11.4 kHz	61°	240 nW
FF	95 dB	13 kHz	68°	920 nW
SS	94 dB	8.5 kHz	48°	68 nW
SNFP	98 dB	12 kHz	60°	260 nW
FNSP	93 dB	11 kHz	63°	244 nW

against power consumption, respectively, for easier reading.

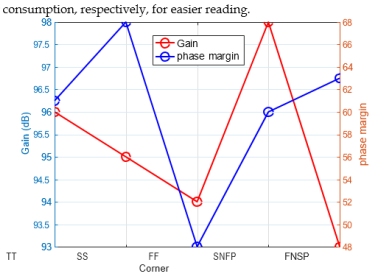

Figure 14. Acquire and stage edge of the Rail-to-Rail Speaker, mimicked in the corner examination.

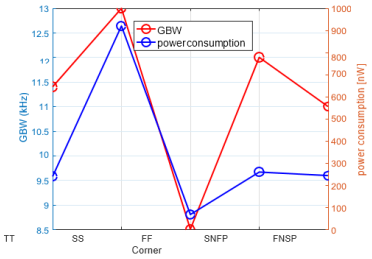

Figure 15. GBW and power utilization of the Rail-to-Rail Speaker, reenacted in the corner examination.

Figures 14 and 15 plot gain and phase margin against power consumption and bandwidth

Also, the FOM has been determined, and it is 1.34. In light of its high addition and expansive familiar mode input range, this enhancer is appropriate for use in ultra low voltage and low power applications.

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