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RESEARCH ARTICLE OPEN ACCESS

DifferentTypes of Shift Register Based on Linear Feedback System and Reversible Gate

Ramswaroop Patidar
M. Tech. Scholar
Department of Electronics and Communication Engineering
Technocrats Institute of Technology, Bhopal

Prof.Divya Jain
Associate Professor
Department of Electronics and Communication Engineering
Technocrats Institute of Technology, Bhopal

Abstract-This paper reviewof Bit Linear Feedback Shift Register which generates pseudo-random test patterns as the input bit is a linear function of its previous state. The total number of random state generated on LFSR depends on the feedback polynomial. As it is simple counter so it can count maximum of 2n -1 by using maximum feedback polynomial. Here in this paper we studyof 16-bit different types of shift register on FPGA by using VHDL and analysis the behaviour of randomness. The analysis is conceded out to find number of gates, memory and speed requirement in FPGA as the number of bits is increased. Also, the simulation problem for long bit LFSR on FPGA is presented. The design is simulated and synthesized in Xilinx software.

Keywords—Serial in Serial Output (SISO), Serial in Parallel out, Parallel in Serial out, Parallel in Parallel Out

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I. INTRODUCTION

A digital circuit plays a vital role in the present communication era, use transistors to produce logic gates in order to realize various arithmetic and logical expressions. The benefits of digital circuits are better noise margin and quality than analog circuits. The error detection and correction is also easier with digital signals. One of the basic components in the digital circuit is a shift register. In many applications such as digital filters, processor in personal computers, communication receivers and image processing Integrated Circuits (IC) is a generally used instance [1, 2]. In recent days the requirement of the shift register is increased in terms of word length, to handle the large size and high quality images in the image processing ICs. A 4K-bit and a 2K-bit shift registers are utilized in the image extraction as well as vector generation in VLSI chips and 10-bit 208-chain Liquid Crystal Display (LCD) column driver IC respectively. It is fairly simple to design a shift register by connecting the required number Flip-flops in series based on its length up to N-bits. There is no circuit between the Flip-flops in the shift register; Flip-flops have superior speed than area and power consumption. The smallest Flip-flop is ideal to reduce area and power consumption by using the shift register. In many applications, pulsed latches have recently replaced Flip-flops, as a pulsed latch is much smaller than a flip-flop. However, due to the existence of timing problem, the pulsed latches cannot be used in a shift register [3].

A linear feedback shift register is a combination of series of flip flop and XOR or XNOR logic gates. Its output is pseudo randomly cycle through a sequence of binary values after certain number of clock cycle [4, 5]. The repetition of random output depends on the number of stages in the LFSR. Therefore, it is an important component in communication system where, it play important role in various application such as cryptography application, CRC generator and checker circuit, gold code generator, for generation of pseudorandom sequence, for designing encoder and decoder in different communication channels to ensure network security, Design for Test (DFT) and Built in Self-Test design (BIST).

A linear feedback shift register is linear in the sense that its input bit is a linear function (XORing or XNORing) of LFSR previous state [6].

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation for VLSI circuits. The power dissipation during the test mode is 200% more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges. Linear feedback shift registers have multiple uses in

digital systems design. Here we have implemented a 32 bit length sequence on FPGA using VHDL with maximum length feedback polynomial to understand the memory utilization and speed requirement. Also, we have presented the comparison of performance analysis based on synthesis and simulation result as well identify the simulation problem for long bit LFSR. The target device we have used Xilinx Spartan 3A and performed simulation and synthesis using Xilinx ISE. The HDLs are VHDL and Verilog. We prefer VHDL for programming because it is widely used.

II. LITRATURE REVIEW

SonamGour et al. [1],in the process of large scale integration lot of transistors are implemented in a very minimum area. Combinational logic has very useful in quantum and many industrial designs. Reducing the power and delay is the principle object in VLSI design. Suppressing sub-threshold leakage current in large scale integration is essential for achieving green computing and facilitating the more usage of power electronics. In this paper the shift register is implemented with or without MTCMOS technique. The Cosmos Scope tool is used to analyze the power delay with the simulation in HSPICE. The Shift Register is fabricated by using the 32nm and 45nm BPTM model file. With the help of MTCMOS technique in Shift Register a reduction in leakage power is 44% in 32nm with the applied voltage of 0.7V and 57% in 45nm with the applied voltage of 0.9V. Energy is reduced by the 5% for 0.7V for 32nm and 21 % for 0.9V at 45nm.

Karthik. B et al. [2], high-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. This classification is based on how to prevent or reduce the redundant internal switching activities. A new flip-flop is introduced: the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small -to-delay characteristics. With a data-switching activity of 37.5%, the proposed flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops.

G. Prakash et al. [3], Quantum-dot Cellular Automata (QCA) is emerging nanotechnology that can represent binary information using quantum cells without current flows. It is known as a promising alternative of Complementary Metal–Oxide Semiconductor (CMOS) to solve its drawbacks. On the other hand, the shift register is one of the most widely used practical devices in digital systems. Also, QCA has the potential to achieve attractive features than transistor-based technology. However, very small-scale and Nano-fabrication limits impose a hurdle to the design of QCA-based circuits and necessitate for fault-tolerant analysis is appeared. Therefore, the aim of this paper is to design and simulate an optimized a D-flip-flop (as the main element of the shift register) based on QCA technology, which is extended to design an optimized 2-bit universal shift register. This paper evaluates the performance of the designed shift register in the presence of the QCA fault. Collected results using QCADesigner tool demonstrate the fault-tolerant feature of the proposed design with minimum clocking and area consumption.

ParthoGhose [4], reversible logic is an emerging technology that plays an important role in the fields of low power computation and can be applied in cryptography, communications, quantum computing etc. Reversible shift registers are one of the most important elements in fabricating reversible memory circuits. In this paper, we present efficient design of different reversible shift registers such as Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out and Parallel In Parallel Out registers. We have also outlined appropriate lemmas to illustrate different properties of the proposed designs. Suitable algorithms for designing the reversible shift registers are also mentioned. Comparative analysis reveals that our proposed design requires minimal number of reversible gates and constant inputs, and also produces less number of garbage outputs than the state-of-theart design. Furthermore, to clarify the validity of our design, all the proposed circuits have been simulated using DSCH3.

Mishra Shivshankar et al. [5],this paper focus on the implementation ofconfigurable linear feedback shift register (CLFSR) in VHDL and evaluate its performance with respect to logic, speed and memory requirement in FPGA. Behavioral implementation of CLFSR in VHDL is configurable in terms of number of bits in the LFSR, the number of taps; positions of each tap in the shift register stage and seed value of LFSR.The target device used for implementation of CLFSR is Xilinx Virtex-4 FPGA. For simulation and synthesis of CLFSR Xilinx ISE 9.2i tool is used. The output waveforms and timing report are also discussed.

SharmaRadhika et al. [6], in chip manufacturing technology, reduction inchip size

possess great concern for power dissipation. Low power testing has become an important issue as power dissipation during testing mode is very high as compare to normal mode. LFSR is used in testing of ASIC chips by generating pseudo random patterns. This paper deals with design of low power LFSR by using GDI technique. GDI technique is one of the low power technique used for implementing various digital circuits.

This technique uses only two transistors to design fast and low power circuits with improvement in power characteristics. LFSR has been implemented by conventional and GDI technique in Cadence Virtuoso at 90nm technology. Comparative analysis is carried out between the two methods showing up to 45.4 % and 20 % reduction in power and area respectively in GDI technique. Simulation and variation of power with frequency and voltage is also discussed.

HathwaliaShruti et al. [7],this paper proposes a 32 Bit Linear Feedback Shift Register which generates pseudo-random test patterns as the input bit is a linear function of its previous state. The total number of random state generated on LFSR depends on the feedback polynomial. As it is simple counter so it can count maximum of 2n -1 by using maximum feedback polynomial. Here in this paper we implemented 32-bit LFSR on FPGA by using VHDL to study the performance and analysis the behaviour of randomness. The analysis is conceded out to find number of gates, memory and speed requirement in FPGA as the number of bits is increased. Also, the simulation problem for long bit LFSR on FPGA is presented. The design is simulated and synthesized in Xilinx 14.5 ISE and Model Sim 10.1b.

III. LINEAR FEEDBACK SHIFT REGISTER

Linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. An LFSR is a class of devices known as state machine. It is a shift register whose input bit is a linear function of its previous state. The only linear functions of single bits are XOR and XNOR. Thus it is a shift register whose input bit is driven by XOR or XNOR of some bits of overall shift register value.

Theory of Operation: -Feedback around an LFSR's shift register comes from a selection of points (taps) in the register chain and constitutes XORing these taps to provide tap(s) back into the register. Register bits that do not need an input tap, operate as a standard shift register. It is this feedback that causes the register to loop through repetitive sequences of pseudo-random value. The choice of taps determines how many values there are in a given sequence before the sequence repeats. The implemented LFSR uses a one-to-many structure, rather than a many-to-one structure, since this structure always has the shortest clock-to-clock delay path.

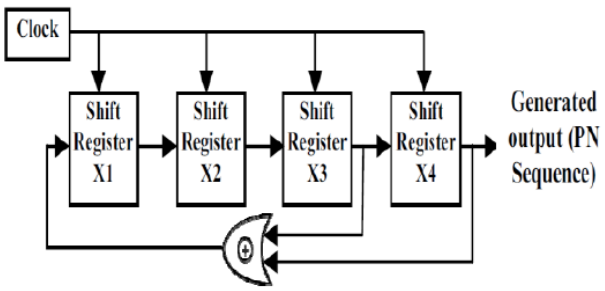

Figure 1 Basic block diagram of LFSR [2]

Pseudo random number sequence generator is generated in VHDL according to the following circuit in Figure 1 based on the concept of shift register.The bits in the LFSR state which influence the input are called taps. A maximum-length LFSR produces an m- sequence (i.e. it cycles through all possible 2n -1 state within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change. The sequence of numbers generated by this method is random. The period of the sequence is (2n - 1), where n is the number of shift registers used in the design.

IV. REVERSIBLE GATE

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gate available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli

gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 2, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

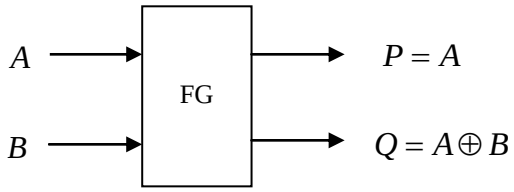

Figure 2: Feynman gate

In figure 3, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

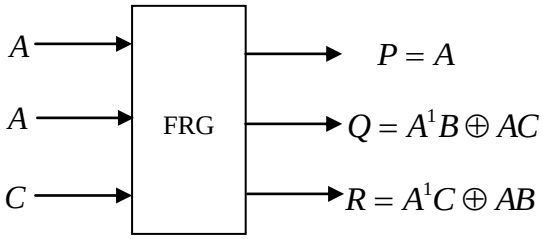

Figure 3: Fredkingate

Figure 4 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

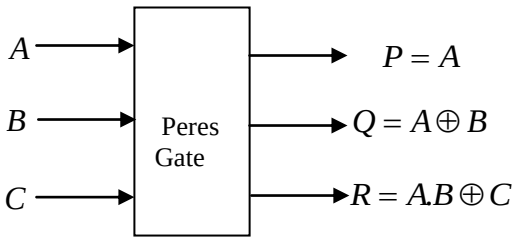

Figure 4: Peres gate

The HNG gate, presented in fig, produces the followinglogical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 5.

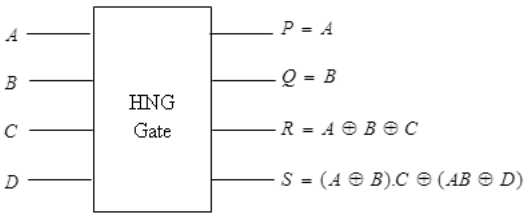

Figure 5: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PAOG) gate – is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Fig. 6 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

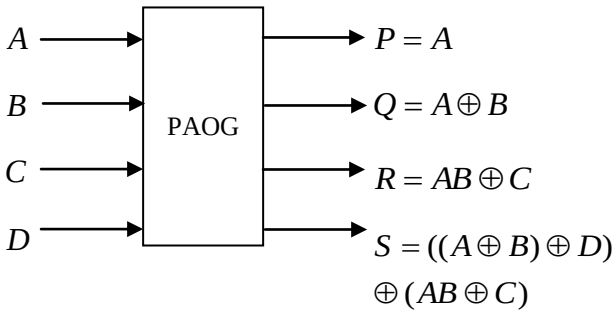

Figure 6: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low costand delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the followinglogical output calculations:

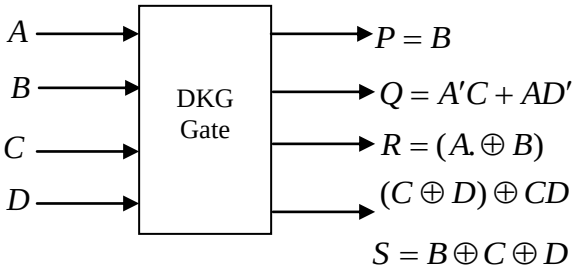

Figure 7: DKG Gate

$$P = B \quad (9)$$

$$Q = A'C + AD' \quad (10)$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \quad (11)$$

$$S = B \oplus C \oplus D \quad (12)$$

V. PROPOSED METHODOLOGY

This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name Shift Register.

A shift register basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.

The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches.

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift register IC's are generally provided with a *clear* or *reset* connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

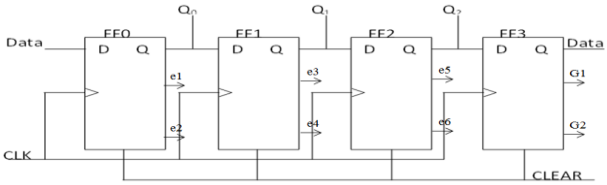

Figure 8: Flow Diagram of Serial in Parallel Output Shift Register

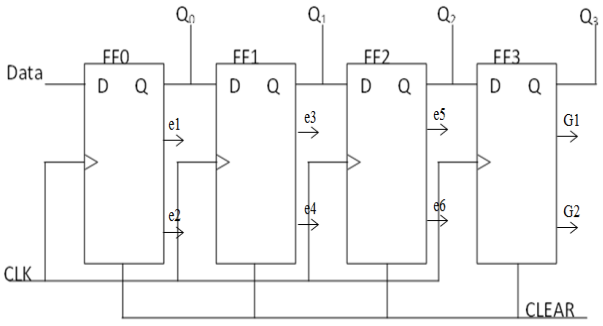

Figure 9: Flow Diagram of Parallel in Serial Output Shift Register

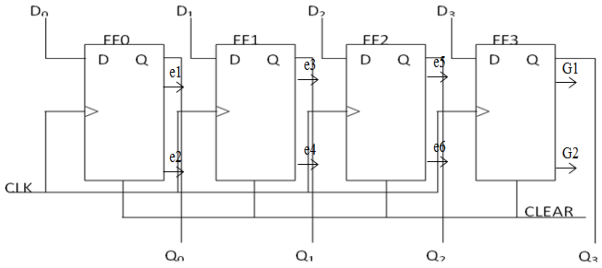

Figure 10: Flow Diagram of Parallel in Parallel Output Shift Register

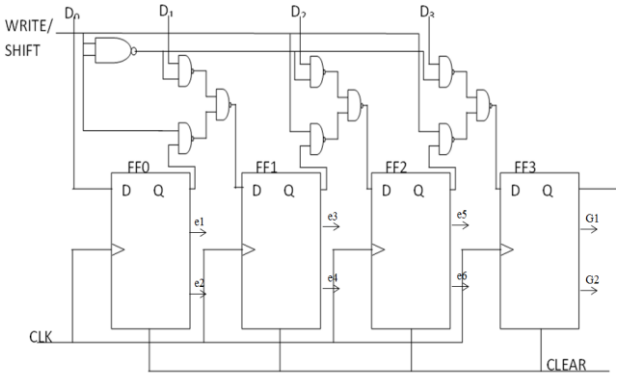

Figure 11: Block Diagram of Reversible Parallel in Serial out Shift Register

VI. EXPECTED RESULT

The proposed implementation is programmed (Described) and implemented using VHDL language which is a Hardware Description Language that was developed by the Institute of Electrical and Electronic Engineers (IEEE) as a standard language for describing the structure and behavior of digital electronic systems. It has many features appropriate for describing the behavior of electronic components ranging from simple logic gates to complete microprocessors and custom chips. The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

- Design 4-bit, 8-bit and 16-bit register with the help of logic gate and flip flop.
- All design are implemented using Xilinx Software for different device family and calculate various parameter i.e.
- Number of Slice
- Number of LUTs
- Number of Flip Flop Pair
- Number of Input Output
- Delay

All design will be compared with the previous base paper (2020) in different device family and achieved good result.

VII. CONCLUSION

Design of a random testing circuit based on LFSR for the external memory interface is discussed in this paper. The random test patterns can improve testing efficiency, and reduce the artificial dependence in testing process in any circuit. Definitely 16-bit LFSR with maximum length feedback polynomial will generate large sequence which is more secure than other but because of simulation difficulties modification in long bit LFSR is needed.

REFERENCES

[1]. SonamGour and Gaurav Kumar Soni, "Reduction of Power and Delay in Shift Register using MTCMOS Technique", Fourth International Conference on Trends in Electronics and Informatics, IEEE 2020.

[2]. Karthik. B, Sriram. M, Jasmin. M. "Low Power and High Performance MT CMOS Conditional Discharge Flip Flop" International Journal of Engineering and Advanced Technology (IJEAT), Volume-8, Issue- 6S2, August 2019.

[3]. G. Prakash , Mehdi Darbandi , N. Gafar, Noor H. Jabarullah and Mohammad Reza Jalali "A New Design of 2-Bit Universal Shift Register Using Rotated Majority Gate Based on Quantum-Dot Cellular Automata T echnology" Springer International Journal of T heoretical Physics, PP-1-19, June 2019.

[4]. ParthoGhose and MdNaimur Rahman, "Design of Reversible Shift Registers Minimizing Number ofGates, Constant Inputs and Garbage Outputs", International Conference on IEEE 2018.
[5]. Shivshankar Mishra, Ram RackshaTripathi and Devendra Kr. Tripathi, "Implementation of Configurable Linear Feedback Shift Register in VHDL", International Conference on Emerging Trends in Electrical, Electronics and Sustainable Energy Systems (ICETEESES–16).
[6]. Radhika Sharma and Balwinder Singh, "Design and Analysis of Linear Feedback Shift Register(LFSR) Using Gate Diffusion Input(GDI) Technique", 978-1-5090-0893-3/16/$31.00 ©2016 IEEE.
[7]. ShrutiHathwalia, Meenakshi Yadav: Design and Analysis of a 32 Bit Linear Feedback Shift Register Using VHDL. International Journal of Engineering Research and Applications, Vol. 4, Issue 6 (version 6), pp. 99-102, June 2014.
[8]. KhushbooSewak, Praveena Rajput and Amit Kumar Panda, "FPGA Implementation of 16 bit BBS and LFSR PN Sequence Generator: A Comparative Study", 2012 IEEE Students' Conference on Electrical, Electronics and Computer Science
[9]. Lenin Gopal, Nor SyahiraMohdMahayadin and AdibKabir Chowdhury, "Design and Synthesis of Reversible Arithmetic and Logic Unit (ALU)", 2014 IEEE 2014 International Conference on Computer, Communication, and Control Technology (I4CT 2014), September 2 -4, 2014.
[10]. Mr. Abhishek Gupta, Mr. UtsavMalviya and Prof. Vinod Kapse, "Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors", 2012 IEEE.
[11]. Akanksha Dixit and VinodKapse, "Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit", International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2012.
[12]. LekshmiViswanath and Ponni. M, "Design and Analysis of 16 Bit Reversible ALU", IOSR Journal of Computer Engineering (IOSRJCE), Volume 1, Issue 1, PP 46-53, June 2012.
[13]. M. Morrison and N. Ranganathan, "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," IEEE International Symposium on VLSI, pp. 126-131, 2011.
[14]. ShefaliMamataj, Biswajit Das, AnurimaRahaman, An Optimized Realization of ALU for 12-Operations by using a Control Unit of reversible gates, International Journal of Advanced Research in Computer Science and Software Engineering, Volume 4, Issue 1, ISSN: 2277 128X, January 2014
[15]. ShefaliMamataj, Biswajit Das, AnurimaRahaman, An Ease implementation of 4-bit Arithmetic Circuit for 8 Operation by using a new reversible COG gate International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, ISSN (Online): 2278 – 8875, Vol. 3, Issue 1, January 2014
[16]. R. Landauer, "Irreversibility and Heat Generation in the Computational Process", BM Journal of Research and Development 5, pp. 183-191, 1961
[17]. C.H. Bennett, "Logical Reversibility of Computation", IBM Research and Development, pp. 525-532, November 1973
[18]. Ravish Aradhya H V, Praveen Kumar B V, Muralidhara K N, Design of Control unit for Low Power ALU Using Reversible Logic, International Journal of Scientific & Engineering Research Volume 2, Issue 9, ISSN 2229-5518, September-2011
[19]. Akanksha Dixit and Vinod Kapse, "Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit", 2012 IJEIT 2012 International Journal of Engineering and Innovative Technology, Volume 1, Issue 6, June 2012.