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RESEARCH ARTICLE OPEN ACCESS

Modified Reduced Count Cascaded Nine-Level Inverter Topology

Kripa Suman *, Rakeshwri Agrawal**, Deepak Agrawal***, Alok Kumar****
(Department of Electrical & Electronics Engineering, Trinity Inst. of Tech. and Res., Bhopal (M.P.)

ABSTRACT
In the class of inverters, multi-level topology is best suited since it has capability generated output wave nearest to the sine wave. Multi-level can be designed using numerous inversion topologies. But among all the topologies Cascaded H-Bridge (CHB) finds widest range of applications since it has the minimal component requirement and the compact circuit design. As the inversion level increases, the DC-bus requirement also increases in case of CHB. This limits its application for higher voltage levels. This paper presents the modified CHB topology which not only reduces the source requirement for each H-type cascaded circuit of CGB, but also reduces the switch requirements to generate the nine-level voltage output. Modification is done both in switching techniques as well as in the switch arrangement of each H-unit. The switching technique used for Modified CHB (MCHB) is sinusoidal carrier wave pulse width modulation i.e. SPWM with frequency shift and phase shift topologies both. While in case of conventional topology, pulse generator is used to generate gate pulses. A comparative analysis is presented in terms of harmonic percentages in case of conventional and MCHB topologies.
Keywords **-** Multi-Level Inverter (MLI), Flexible AC Transmission System (FACTS), Power System Stabilizer (PSS), Static Var Compensator (SVC), Voltage Stability.

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I. INTRODUCTION

The **headings** Inversion is a process of converting DC into AC of predefined voltage and frequency. Inverter is a Power Semiconductor Device which performs the function of inversion. The present structure of power system has inverter applications in numerous ways such as an interfacing medium for renewable resources, for DC-linking in high voltage DC transmission, for obtaining AC output with variable frequencies, in variable frequency drives, air-conditioning module for obtaining speed control of motor in accordance to the temperature control, etc. [1-3]. Hence inverter has high utilization in the utility system.

Conventionally when inverter was invented, they were two-level output voltage type [4]. Which generate AC with square waveform having positive and negative voltage magnitude as the AC peaks which is presented in figure 1. To obtain sinusoidal AC output, a filter unit is required. This type of topology has high harmonic content and with filter connected losses in the system increases. Also, when operating at high switching frequencies, the two - level inverter has high degree of electromagnetic interference as well as they are less efficient for higher ratings. To overcome all the above mentioned problems, the two level inverters were evolved into Multi-level Inverter (MLI) [5, 6]. MLI synthesizes the sine waveform with more levels in step-shaped with reduced non-sine area of generated output wave shape. This reduces the harmonics genuinely and is very efficient even at very high switching frequencies as on reducing the interference due to near-by magnetizing circuits. Hence conventional two-level are rapidly being replaced by MLI [7].

The simplest MLI topology is the one with three level of output voltage as shown in figure 1. The MLI circuit is obtained by connecting the switching devices in a revolutionary form with proper gating signal to control the output generated by the MLI. If switches are connected with clamping diodes and source balancing capacitors, it is termed as Neutral-point Clamped topology or NPC. If capacitors are connected in fixed proportion of the source it i.e. termed as fixed capacitor topology. If no additional devices other than the Power Semi-Conductor Switch (PSCS) is connected in H-shaped unit with cascaded structure, it is termed as H-bridge Cascaded topology. and the combination of above mentioned topologies are termed as hybrid topologies [8-10]. To reduce the harmonic content in

the output waveform, the number of levels is increases; like 5-level, 7-level, 9, 11, 13-level upto any number. But with the increased in the levels, the number of switching devices increases aw well as component requirement of the topologies also which makes the circuit very bulky and complicated too since simultaneously switching circuit to generate the gate pulse also become complicated [11]. This rase the need to reduce the switch count in order to reduce the switching requirement as well as simplify the gate circuit. This type of topologies is available in literature with reduced count or modified nomenclature such as modified cascaded topology or reduced count NPC topology etc. For MLI topology cascaded one has the minimal component requirement, hence it is widely adopted type [12].

This paper presents the modified topology for cascaded MLI with reduced switch count to obtain the nine level (9L) output voltage. The comparison among the conventional cascaded 9-Level (CC9L) topology with the modified one is also presented to justify the work. Also, the comparative analysis of both the topologies conventional and modified 9L cascaded MLI is present in terms of Total Harmonic Distortion (THD) in output voltage to test the efficiency of the proposed modified cascaded topology. the inverter size is compared with cost analysis of the work proposed.

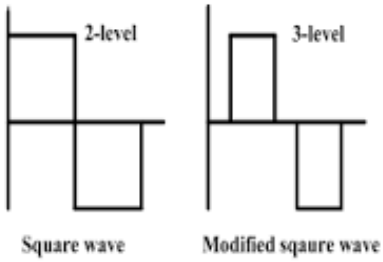


Fig. 1 Two-level and three-level inverter output

II. SINUSOIDAL PULSE WIDTH MODULATION (SPWM)

The output obtained from inverter depends upon the switching states of the switches connected in the circuit [8]. Hence control circuit for gate triggering is very important. In literature numerous topologies are available to design the gate-pulse such as; space vector modulation, selective harmonic elimination based, space vector control, Sinusoidal Pulse Width Modulation (SPWM), etc. SPWM is the widely adopted technique for gate pulse generation since it is simple to implement and robust too. It generates gate pulses in a way to produce output voltage of inverter very near to sinusoidal [13].

SPWM technique in which reference voltage waveform is a modulating wave and the modulated wave is the carrier wave. Here, the peak-to-peak value of the triangular carrier wave is given as the DC-link voltage V_{dc}. In this PWM technique, the necessary condition for linear modulation is that the amplitude of the voltage reference V_{ref} must remain below the peak of the triangular carrier V_C, i.e., $V_{ref} \leq V_{dc}/2$. Since this PWM technique utilizes a high-frequency carrier wave for voltage modulation, this kind of PWM technique is called a carrier-based PWM technique [14]. The graphical representation of SPWM is presented in figure 2. In SPWM, sinusoidal AC voltage reference V_{ref} is compared with the high-frequency triangular carrier wave V_C in real time to determine switching states for each cycle in the inverter. Positive or negative switch for each cycle is triggered by comparing V_{ref} and V_C;

- For $V_{ref} > V_C$; switch of positive cycle will be onn.
- For $V_{ref} < V_C$; switch of negative cycle will be onn.

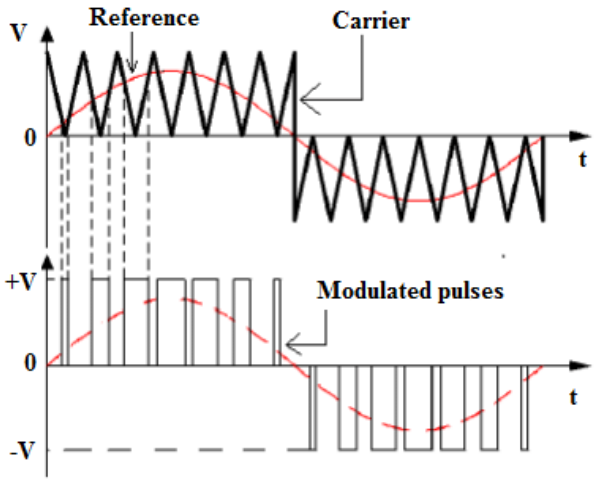


Fig. 2 Carrier based sinusoidal PWM

SPWM is further categorized as level shifted and phase shifted modulation. In Level-Shifted (LSPWM) switching angle of each carrier wave is

varied [15]. In case of phase shift amplitude of the carrier wave is varied. And another one is Variable Frequency based SPWM (VF-SPWM), in which switching frequency of the carrier wave is varied [16].

In this work triangular pulse based carrier wave is selected and the SPWM is designed using LS-SPWM and VF-SPWM. In LS-SPWM, phase shift of each carrier wave is carried by changing the switching angle of the wave as shown in figure 3. Also, VF-SPWM based modulation technique is employed to design the gate pulses of the switches of the inverter by varying the frequency of the carrier pulse as shown in figure 4.

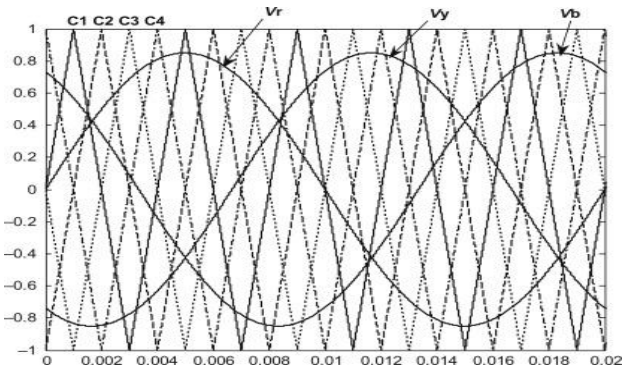


Fig. 3 Level-shifted SPWM

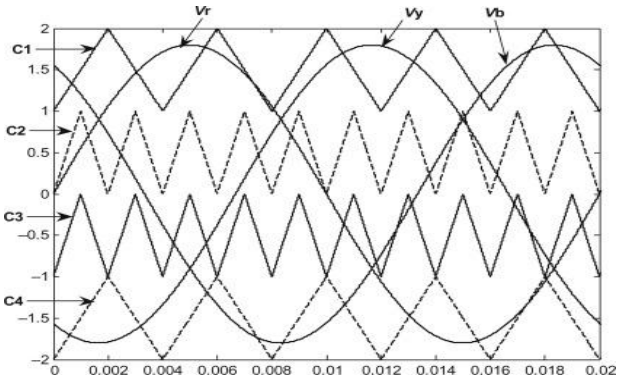


Fig. 4 Variable frequency SPWM

III. MODIFIED CASCADED H-BRIDGE (MCHB)

MLI are witnessing continuous research since they are used in various high power applications including interfacing medium for renewable sources, in FACTS system design, as a power compensating device, AC power high motor device etc. MLI is designed via series and shunt combination of PSCS in a passion to obtain equal voltage distribution across each switch which can generate step-waveform output voltages. The commutation of the PSCS permits the addition of the switch voltages and generates high voltage at the output [17].

MLI has basic three topologies namely; NPC, FC and cascaded structure. Each topology has its cons and pros [18]. And with the continuous research process going on numerous more topologies are invented with the combination and modification in the basic topologies. In this CC9L and modified cascaded topology is presented to generated the 9-level voltage output. The conventional cascaded H-bridge to generate nine level output voltage is designed using 16 PSCS as shown in figure 5. Over all four H-shaped unit is designed. One H-shaped unit is consisting of four switches connected in H shape. Individual DC-source is required across each H unit. Hence over all four DC-source is required to generate 9-level form conventional topology. All the four H-shaped unit of cascaded MLI topology are connected in series with each other.

In Modified Cascaded H-Bridge MLI (MCHB-MLI) only eight switches are required to generate 9-level output voltage. Only three DC-sources are used. In this work SPWM technique is used to trigger the switches of the MLI. In this work results are presented for level-shifted and variable frequency based SPWM to analyse the change in output voltage. The MCHB-MLI topology is presented in figure 6.

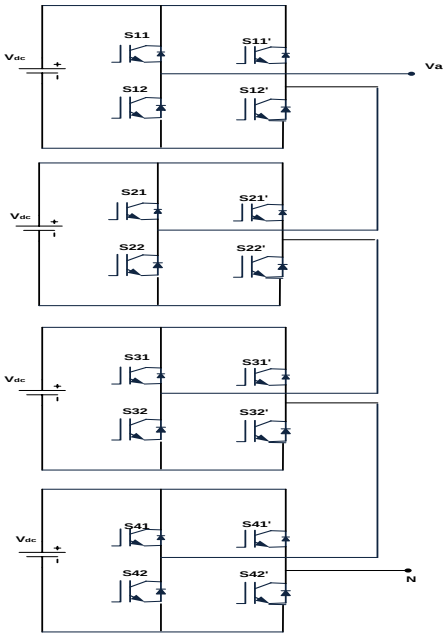


Fig. 5 Conventional 9-level topology

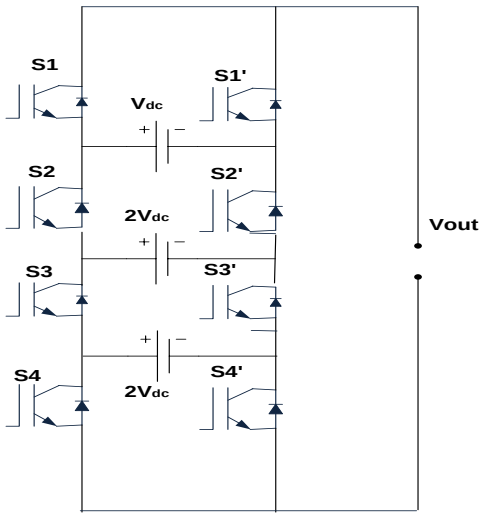


Fig. 6 Modified 9-level CHB topology

IV. SIMULATION MODEL AND RESULTS

In this work performance analysis of CC9L and MCHB topology is presented to generate the 9-Level voltage output. The proposed work is carried out in MATLAB software. Firstly, performance analysis of CC9L is presented. The CC9L is designed with 16 MOSFET switches. Gate pulses to the switches are given using pulse generator with 40 % pulse width and phase delay varying between 0.1-0.4 % for each switch. The complete simulation model for conventional topology is presented in figure 7. The system is analysed for single phase with overall aprox. 480 V. The conventional topology is designed with four H-bridge unit and each unit has a DC source of 145 V to obtain in total 580 V. The 580 V input generates 480 V staircase ML single phase output as shown in figure 8. The harmonic analysis of the output wave form has 18.9 % THD in conventional topology as shown in figure 9.

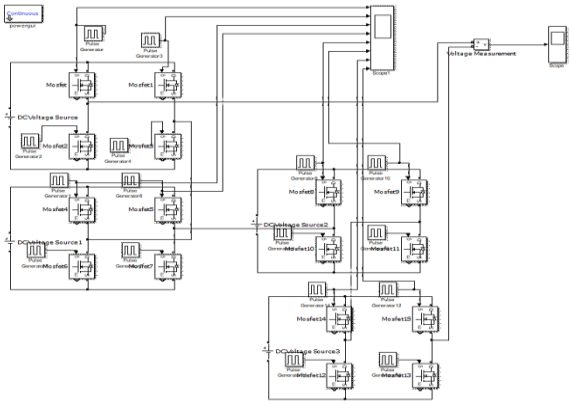


Fig. 7 Simulation model for conventional cascaded MLI

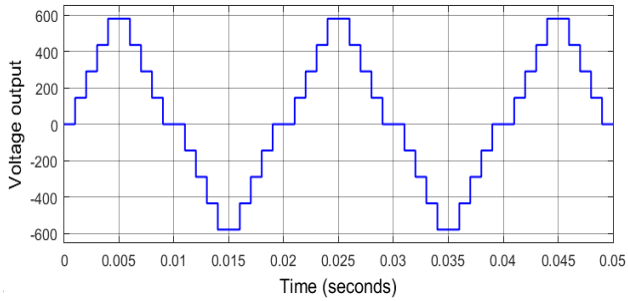


Fig. 8 Output voltage of conventional cascaded MLI

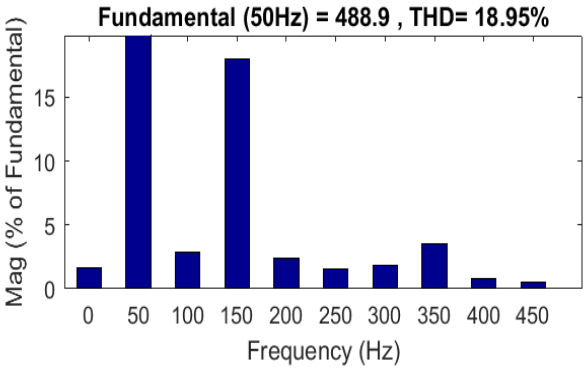


Fig. 9 THD of output voltage of conventional cascaded MLI

Now performance analysis of proposed reduced count modified cascaded MLI is presented. This

topology is designed using only eight MOSFET switches. Switches are connected in continuous H-format and the MCHB does not contain any single H-unit, rather the PSCS switches are connected in continuous H-pattern as shown in figure 10. The gate pulses are designed using LS-SPWM and VF-SPWM. To generate nine level using MCHB, in the proposed topology 11-input signals are when employing SPWM technique. Ten triangular pulse generator which form the carrier wave and one sine wave is generated which is the modulating signal. In LS-PWM, switching frequency is kept constant at 5KHz and phase angle of the carrier wave is shifted. Where as in case of variable frequency based SPWM, phase angle as well as frequency of the carrier wave both is varied. The output voltage of LS-SPWM is shown in figure 11 and the respective THD percentage is shown in figure 12. The output voltage of VF-SPWM is shown in figure 13 and the THD percentage for the output of VF-SPWM is shown in figure 14.

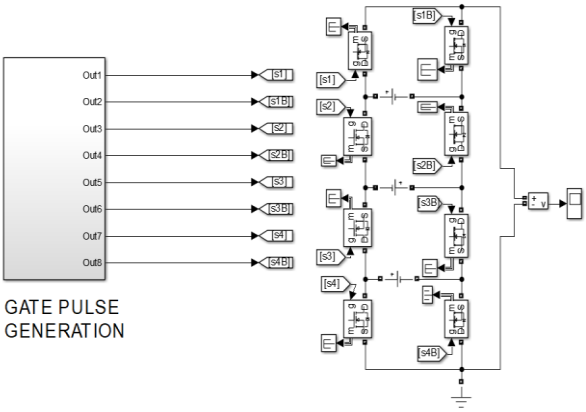


Fig. 10 Simulation model for modified cascaded MLI

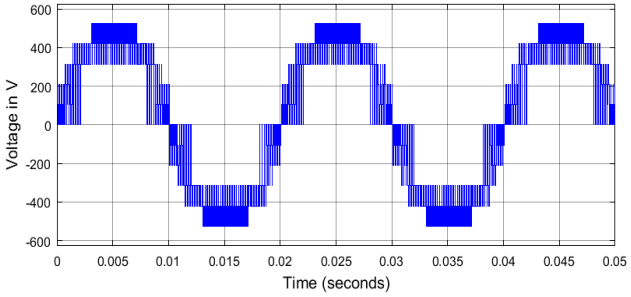


Fig. 11 Output voltage of MCHB-MLI with LS-SPWM

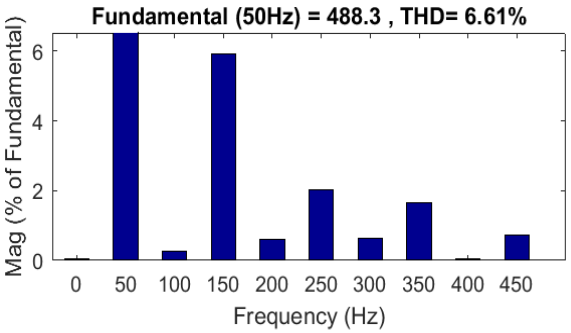
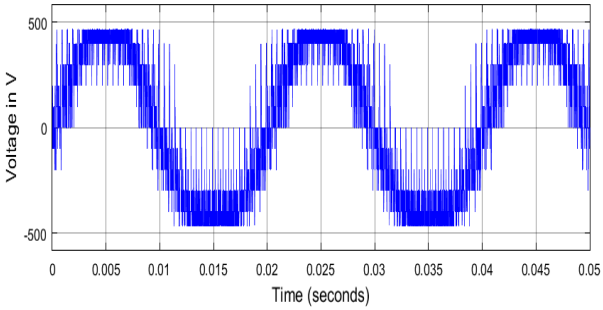


Fig. 12 THD percentage of output voltage of MCHB-MLI with LS-SPWM



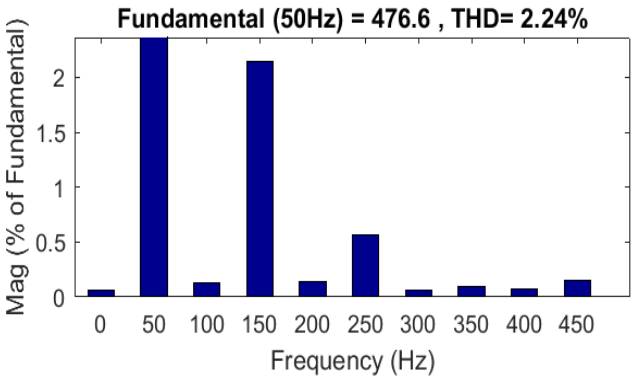


Fig.14 THD percentage of output voltage of MCHB-MLI with VF-SPWM.

V. RESULT DISCUSSION

This work presents the comparative analysis of conventional and modified cascaded 9-L MLI topology. Figure 7 presents the conventional topology of CHB-MLI and figure 10 presents modified topology. From the figure it can be seen that the conventional topology requires 16 MOSFET where-as MCHB-MLI is designed using 8 switches

which just half of the conventional topology. Also, the conventional one uses four DC source having 145 V capacity each. On the other-hand modified topology needs only three source having one 100 V and other two is rated with 200V. In this work modification in gate pulse generation for the MOSFETs used in MCHB-MLI. The voltage output generated with conventional topology as shown in figure 8 is simply stairs with 9 level where as in case of the modified topology output the width of the stairs are large and varied as per the gate pulse width. Also, in case VF-SPWM the output voltages as spikes with the stairs as shown in figure 13. Also the THD in case of conventional topology is very high having 18.9%, in case of LS-SPWM it reduces to 6.61 % and it is lowest in case of VF-SPWM with 2.2%.

VI. CONCLUSION

The MLI are widely used in numerous application, seeing to this continuous researches are going on to improve the performance efficiency of the various topologies in terms of reduction PSCS requirement and THD percentage in output voltage obtain for the specified levels. In this work a comparison is presented for conventional cascaded-H-Bridge 9L topology and modified cascaded topology. The modification is made in both the gate pulse generation technique and the switch arrangement of the CHB-MLI. The modification reduces the size of the MLI with half of the switch requirement in comparison to conventional topology, which also reduces the cost of the MLI. With the reduction in size improvement in harmonic profile is also witnessed. The proposed MCHB-MLI remarkably reduces the THD % in the output voltage waveform. Hence the proposed topology has better performance efficiency and reduced component and cost requirement which is economical too.

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