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RESEARCH ARTICLE OPEN ACCESS

Comparative Analysis of NPC-MLI and CHB-MLI Based DVR to Mitigate Voltage Sag/Swell

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ABSTRACT
Each component of power system is designed for a specific voltage rating. Voltage Sag/Swell (VSS) are the temporary events which results in voltage variations to the lower and upper side of the rated value. This voltage variation may damage the various voltage sensitive equipment connected to the network. Hence this paper presents the Dynamic Voltage Restorer (DVR) designed using Multi-Level Inverter (MLI) topology to regulate the voltage under the condition of VSS. In this work five-level Neutral Point Clamped and Cascaded H-Bridge (NPC-CHB) MLI is used to design the converter of DVR. The comparative analysis of THDs in voltage-current under the condition of VSS is presented for NPC-CHB MLI.

Keywords **-** Dynamic Voltage Restorer (DVR), Multi-Level Inverter (MLI), Neutral Point Clamped and Cascaded H-Bridge (NPC-CHB), Power Quality, Voltage Sag/Swell (VSS).

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I. INTRODUCTION

The Modern Power is a tassel of voltage sensitive loads having high precision control involving Power Electronic Device Interface (PEDI). These loads may collapse under the condition of voltage fluctuations. Voltage fluctuations are the results of Voltage Sag/Swell (VSS) which generates sever Power Quality (PQ) issues. Voltage sag are reduction in voltage between 0.1-0.9 pu for a duration of 0.5cycle to 1 min [1]. It is caused due to system faults, over loading with generation mismatch, switch-in of high power transformer or surge suppressor [2]. On the other hands voltage swell is increased voltage value for 10% or more for short duration of 0.5cycle to 1 min [1]. It is the result of unplanned bulk load shedding, cut-off of power transformer, capacitor switching, switch-in of high rating generator, etc. VSS are commonly occurring power system phenomenon which results in downtime, network outages or equipment failures [3]. They severely affect the Power quality (PQ) of the supply, hence needs a proper analysis and monitoring as well as mitigation of the same must be done then and there [4,5].

The Dynamic Voltage Restorer (DVR) is widely adopted in distribution side to protect the sensitive loads against VSS [6]. DVR is meant to regulate the load voltage by injecting required voltage of specific amplitude and angle in series with the load voltage. A lot of research is available regarding the utility of DVR to mitigate the condition of VSS [7]. In particular DVR is a series connected PEDI which employs Voltage Source Inverters (VSI) in order to control the load voltage. As the applications of DVR becoming popular, it attracted the attention of the researchers to improve its performance efficiency. Various topologies are available for designing the control architecture of DVR. One of them is MLI based DVR.

MLI has inherent advantage of generating AC output with reduced THD and are widely adopted for high power applications [8]. MLI are particularly employed for sensitive loads in order to acquire high efficiency even for low switchable frequency and results in approximately no electromagnetic interference. In this work DVR is designed using five-level Cascaded (CHB) as well as Neutral Point Clamped (NPC) MLI. The CHB-NPC is the widest adopted and the oldest conventional MLI topologies. Performance analysis of NPC-DVR and CHB-DVR is presented to mitigate sag which is created by applying system faults and the swell as a result of increase in supply for short duration. The comparative results are presented for component requirements, filter size and THD percent in voltage and current.

II. DYNAMIC VOLTAGE RESTORER (DVR)

The Dynamic voltage restorer (DVR) is the prominent option for power engineer in order to mitigate the voltage related PQ issues popularly adopted in distribution system [9]. The typical DVR-design is demonstrated in Figure 1, comprising PEDI based VSI, control unit, filter element, and series coupling transformer or injection transformer. The DVR attaches in series with power network and injects the required reactive demand to compensate VSS. The control circuit designs the gating signal for VSI which is passed through filter unit in order to regulate line voltages. The anti-sag/swell is filter out unwanted harmonics in injection voltage. The function of coupling transformer is to connect the DVR in series with the power network. The performance of DVR is governed by the selection of its control design for switching of semiconductor switches connected and its filter combination. This work presents the load voltage regulation topology with the help of DVR under the condition of VSS, and reduces the THD percentage when system is undergoing abnormal operation.

The conventional two-level inverter based DVR requires high switching frequency of the power converter to obtain a low total harmonic distortion (THD) of load voltage for VSS [10]. Inappropriately, the high switching frequency increases the controller computational burden and the switching losses. This loop in DVR topology can be overcome by employing MLI topology in designing DVR in place of two-level VSI (2-L-VSI).

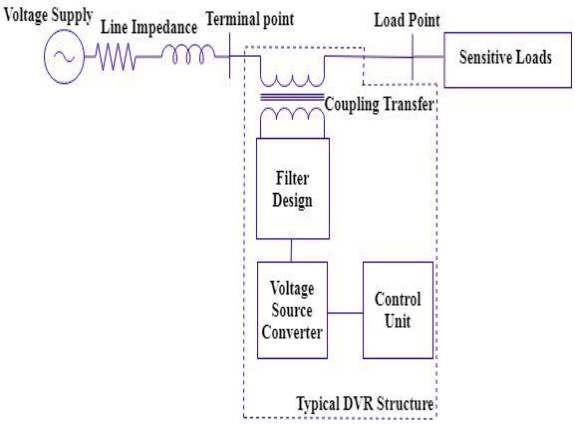

Fig. 1 General architecture of DVR

III. NPC-MLI AND CHB-MLI

As compared to 2-L-VSI, MLI operates at low switching frequency hence efficiency of the system is enhanced [11]. It is suitable for high voltage and current applications and has no-EMI effect due to component saturation. The commonly used MLI topologies are 3-level NPC and CHB [12]. In this work DVR is designed using 5-level NPC and CHB. Their comparative analysis is presented in terms of THD percentage to obtain the high performance capability. Also, the MLI-DVR is compared for the component requirement and the filter size. The schematic diagram of three-phase NPC-MLI is presented in figure 2 and for CHB-MLI is presented in figure 3. For designing 5-L-NPC-MLI, total 24 switches, 8 switches per phase is required [13]. 12 balancing capacitors, 4-per phase is required for equal voltage distribution across each switch. Six clamping diodes per phase, i.e., 24 diodes are also required with one DC-source. On the other hand, 5-L-CHB-MLI is also designed using 24 switches, 8-per phase, but it does not required any additional diodes or capacitors [14]. The switches are arranged in H-shape that is, single unit of CHB is designed using 4 switches arranged in H-structure. One phase of 5-Level consists of two such units connected in series as shown in figure 3. For equal distribution of voltage across each switch, each H-unit is supplied by equal DC-source. Hence over all DC-source requirement is six in case of 5-L-CHB-MLI, two per phase basis [14]. The three-phase voltage output for 5-level MLI is shown in figure 4.

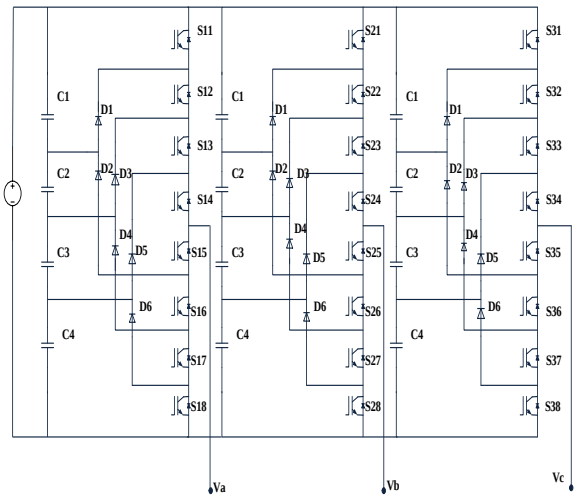

Fig. 2 Three-phase 5-level NPC-MLI

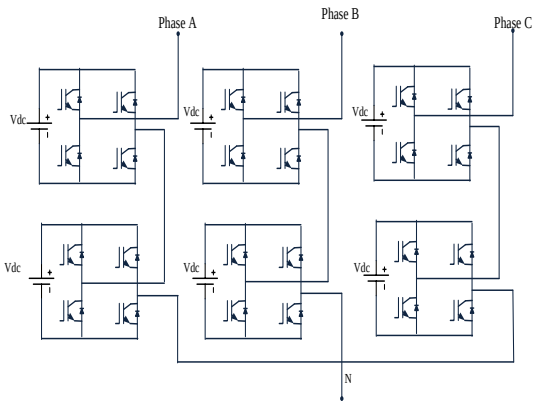

Fig. 3 Three-phase 5-level CHB-MLI

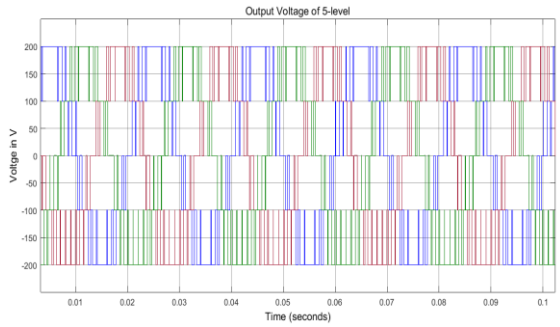

Fig. 4 Output voltage of 5-level MLI

To obtain gate pulses for triggering the switches of the MLI, In-phase Sinusoidal Pulse Width Modulation (SPWM) technique is used. In this technique, sin pulse is obtained by referencing the grid signals as shown in figure 5 and also it forms the envelope to generate the gate pulse for the triangular pulse generator. The phasor diagram of SPWM is shown in figure 6.

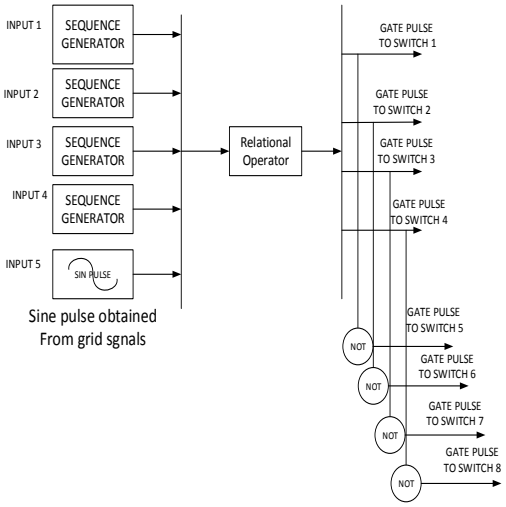

Fig. 5 Circuit topology for 5-level SPWM

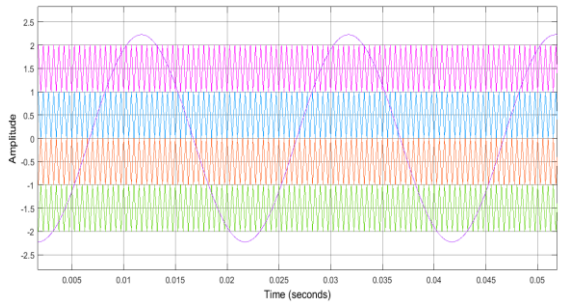

Fig. 6 Gate pulse generation using In- phase SPWM

IV. SIMULATION RESULTS

In this work performance analysis of MLI-DVR to mitigate VSS is presented. The matlab simulation model is designed for 5-L-NPC-MLI and 5-L-CHB-MLI. DVR regulates the load voltage by injecting required voltage under the condition of voltage sag as well as swell. In this work simultaneous sag/swell condition is analysed so as to check the performance of the designed MLI-DVR under dynamic condition of random voltage fluctuation. To create the condition of voltage-sag, a three phase fault is introduced grid side for the duration of 0.2-0.3 sec and swell in voltage is created with the help of programmable three phase source for the duration of 0.4-0.5 sec. Firstly, performance analysis of 5-L-NPC-MLI-DVR is analysed. The general block diagram of MLI based DVR topology is presented in figure 7. The design parameter for 5-L-NPC-MLI-DVR is presented in table-1 below.

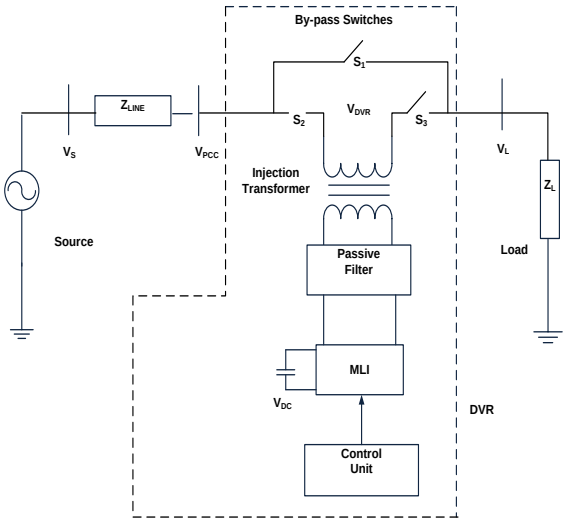

Figure 7 MLI based DVR topology

TABLE I. DESIGN PARAMETERS

S. No.	Parameter	Value
1.	RMS Voltage	415V
2	Frequency	50 Hz
3	Linear load	10kW, 100VAR
4	Vdc	170 V
5	Transformer resistence	100 Ω
6	Transformer impedance	0.05
7	Turns ratio	1
8	Filter resistance	0.1 Ω
9	Filter Inductance	20 mH
10	Filter capacitance	570 μ F
11	Balancing Capacitance of NPC-MLI	1μ F

For linear load connected under stable operation, load as well as source voltage is completely sinusoidal as shown in figure 8. When system undergoes simultaneous VSS at grid side resulting in voltage fluctuation as shown in figure 9.

The 5-L-NPC-MLI-DVR is connected at load side. Hence the voltage fluctuations at grid side will not affect the load voltage as shown in figure 10. The system has also been analysed for harmonics to observe that the grid side fault or swell in voltage injects the harmonics (voltage harmonics is 20 %) as shown in figure 11, but 5-L-NPC-MLI-DVR mitigate the condition of VSS and also reduces the system harmonics upto 2.2 % and 1.9 % as shown in figure 12 and figure 13 for voltage as well as current.

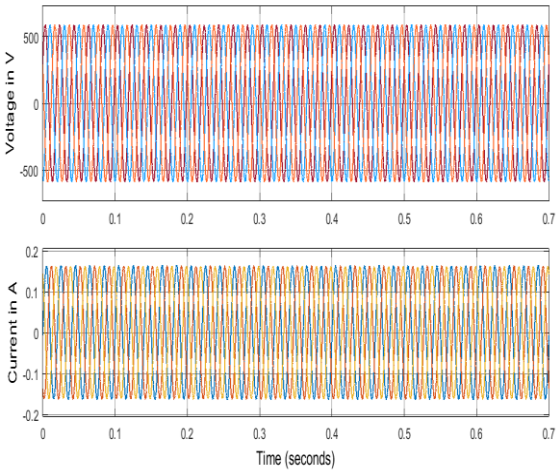

Fig. 8 Voltage and current under normal operating condition

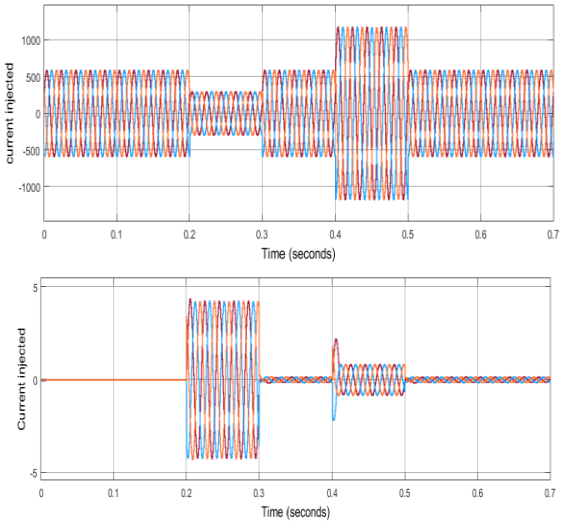

Fig. 9 Voltage and current source side under the condition of VSS

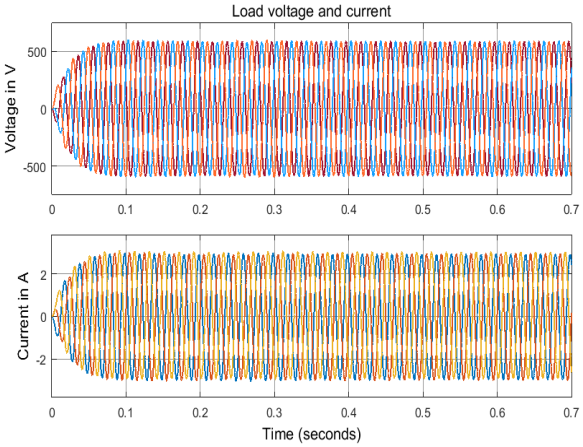

Fig. 10 Voltage and current load side under the condition of VSS with 5-L-NPC-MLI-DVR

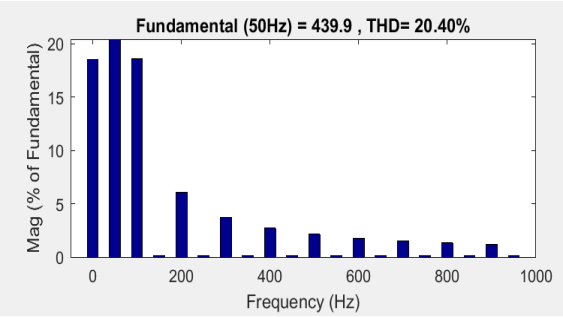

Fig.11 Source voltage THD under the condition of VSS

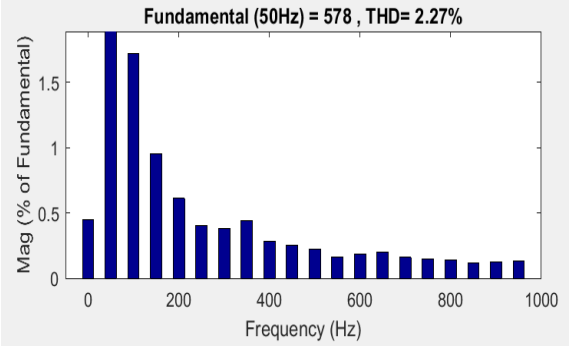

Fig. 12 Load voltage THD under the condition of VSS with 5-L-NPC-MLI-DVR

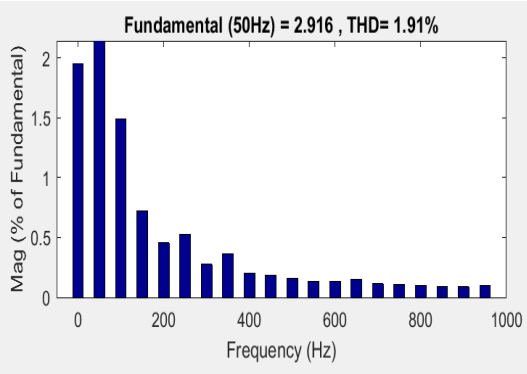

Fig.13 Load current THD under the condition of VSS with 5-L-NPC-MLI-DVR

The performance analysis of 5-L-CHB-MLI-DVR is also analysed. The grid parameters are same as presented in table-1, but the for designing CHB-MLI no additional diodes or balancing capacitor is required. The 5-L-CHB-MLI needs six DC-sources, each DC-source has rating of 100V hence overall 600 V dc supply is required to energize the circuit of 5-L-CHB-MLI. The only additional component required in filter which has values of 0.1 Ω for resistance, 21mH for inductance and 210 μ F for capacitance.

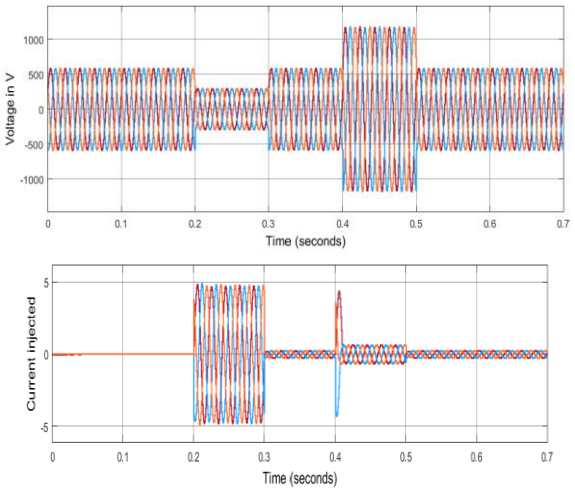

Fig. 14 Voltage and current source side under the condition of VSS

The voltage wave-shape under VSS grid side and current injected by DVR is shown in figure 14. With 5-L-CHB-MLI connected in series with the system the load voltage-current are constant with smooth sine-shape even under the condition of sever voltage fluctuations at source side as shown in figure 15. The THD percentage for voltage at load side is 0.9 %, and THD percentage for current at load side is 0.79 % as shown in figure 16 and figure 17.

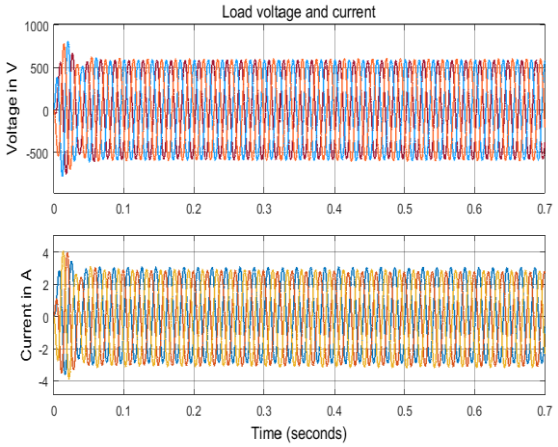

Fig. 15 Voltage and current load side under the condition of VSS with 5-L-CHB-MLI-DVR

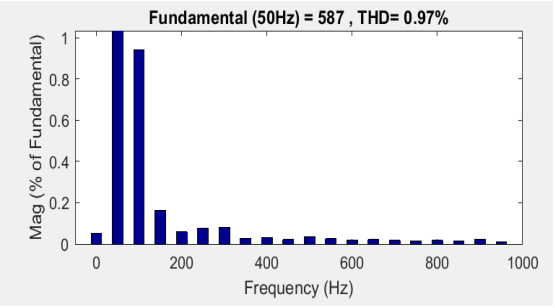

Fig. 16 Load voltage THD under the condition of VSS with 5-L-CHB-MLI-DVR

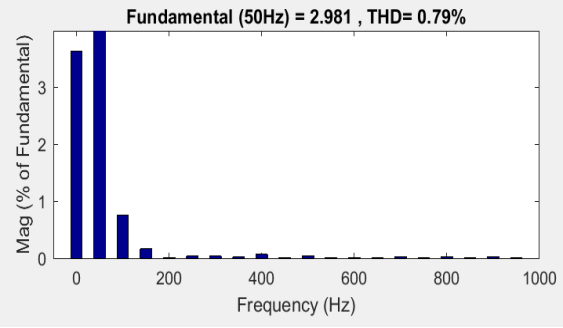

Fig. 17 Load voltage THD under the condition of VSS with 5-L-CHB-MLI-DVR

V. RESULT DISCUSSION

The THD percent of voltage and current under VSS in case of 5-L-NPC-MLI-DVR is more than 2% while in case of CHB it is near about 1%. Though THD percentage in both the cases is competent, but if both the topologies are compared in terms of component requirement then NPC has high number in comparison to CHB. Also, the size of filter is large for NPC. The capacitance size for NPC is 570 μ F on the other hand for CHB it is 210 μ F, which is three time smaller than NPC.

VI. CONCLUSION

The work presents the PQ issues mitigation generation due to voltage fluctuation caused by the occurrence of voltage sag/swell particularly at source side. DVR is widely adopted in distribution system to protect the sensitive loads against wide-voltage fluctuations. In this work MLI based topologies for DVR using neutral point clamped and cascaded-H-bridge based MLI-DVR is designed. The comparative analysis is presented on the basis of harmonic reduction, component requirement and filter size. From the analysis it can be concluded that CHB has better performance efficiency, since it has better THD percentage, low component requirement and small filter size in comparison to NPC.

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