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Single Phase Transformer less Switched Capacitor Inverter with Low Common –Mode Current

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ABSTRACT
Now a day's transformers less topology are employed in single phase PV inverter, a galvanic connection between the grid and the PV array exists. The circulation of leakage currents (common-mode currents) through the stray capacitance between the PV array and the ground would be enabled. However, these common-mode (CM) currents of the transformer less PV inverter will lead to serious electromagnetic interference, insecurity, and reduce the reliability of the PV inverter systems. By introducing the clamping topology that is adding diode clamp circuit to the H5 topology the CM current is maintains constant, and it also eliminates the voltage fluctuations in the system. Along with this H5-D topology adding the switched capacitor multi-level inverter which boosts up the output voltage levels with less number of components. The advantage of the switched capacitor cell is to obtain multiple level of output voltage with less number of switches. Simulation study of this H5D-SC topology inverter is carried out in MATLAB/Simulink R2017a.

Keywords - common mode current, clamp circuit, h5D-SC topology, inverter, switched capacitor

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I. INTRODUCTION

Energy from renewable sources is becoming a common interest of research due to the rapid increase of energy demand and the exhaustion of global resources. Among renewable power sources, photovoltaic (PV) energy source is known as one great alternative all over the world due to the inexhaustible and pollution-free nature of solar power [1]. However, the common-mode (CM) currents of the transformer-less PV inverters could flow through the parasitic capacitor between the PV array and the ground, which will lead to serious electromagnetic interference and insecurity, and reduce the reliability of the PV inverter systems in practice, such as the hybrid energy storage systems[2].

In real PV systems, there are stray capacitances that Provide electrical paths for the ground current, known as the common-mode current I_{cm}. The value of the common-mode current is a function of the common-mode voltage. However, the value of I_{cm} cannot be directly deduced from the value of V_{cm} because I_{cm} is also affected by other voltage sources and by elements such as the system parasitic elements [3]. So this common mode voltage and current is minimized by the H5-D topology. Also increase the level and gain of output voltage with minimum number of switches. In normal inverter the magnitude of output voltage is same as input voltage when Modulation Index (MI) is equal to one [4].

Multilevel inverter is mainly controlled by Multi-carrier Pulse Width Modulation method and the harmonic contents can be reduced by PWM technique [7]. The multi carrier pulse width modulation enhances the power quality. The modulation strategy employed in this system is Phase Disposition PWM (PDPWM). The Switched Capacitor Multilevel Inverter (SC-MLI) is a novel MLI structure introduced recently which requires a reduced number of power supplies in comparison with the conventional multilevel inverters. In SC-MLI, capacitors are used as alternative dc sources. Further, SCMLI possesses the voltage boosting capability and self-capacitor voltage balancing ability [9]. In-order to overcome the problems in inverters and Improved H5D-SC Topology with Low Common-mode Current, for Transformer-less PV Grid Connected Inverter is introduced to reduce the common mode current [10].

II. SWICHED CAPACITOR MULTILEVEL INVERTER WITH LOW COMMON MOE CURRENT

A. H5D TOPOLOGY WITH COMMON MODE CURRENT

The common mode current measured by the capacitor C_{PV} is the equivalent ground parasitic capacitor. Its capacitance is determined by the material, size and frame of the PV array, the air humidity etc. However, the common-mode (CM) currents of the transformer less PV inverters could flow through the parasitic capacitor between the PV array and the ground, which will lead to serious electromagnetic interference and insecurity, and reduce the reliability of the PV inverter systems in practice, P and N are the positive and negative terminals of DC bus voltage. A and B are the midpoints of bridge arms. In this topology V_{COM} and V_{DIF} that is common-mode and differential mode voltage are measured, this two voltages are related to the voltage between the points A, B and the point N (V_{AN} and V_{BN}).

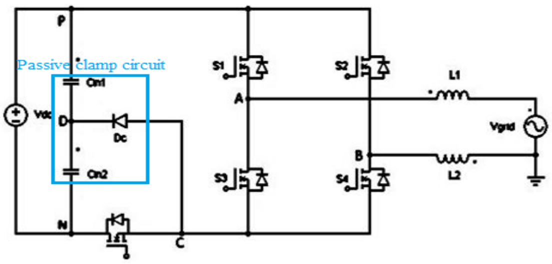

Figure 1. H5-D inverter circuit

Common mode voltage V_{COM}

$$V_{COM} = \frac{V_{AN} + V_{BN}}{2}$$

Differential mode voltage V_{DIF}

$$V_{DIF} = V_{AN} - V_{BN}$$

Total common mode voltage V_{TOTAL}

$$V_{COM-DIF} = V_{COM} - V_{DIF} = \frac{V_{AN} + V_{BN}}{2} * \frac{L_2 - L_1}{2 * (L_2 - L_1)}$$

$$V_{TOTAL} = V_{COM} + V_{COM-DIF}$$

$$V_{TOTAL} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} * \frac{L_2 - L_1}{2 * (L_2 - L_1)}$$

$$I_{COM} = C_{PV} \frac{dV_{TOTAL}}{dt}$$

It is obvious that I_{COM} is related to the CM voltage V_{TOTAL} and the equivalent parasitic capacitor C_{PV}. And there is $V_{TOTAL} = V_{COM}$ when $L_1 = L_1$ with sufficient condition

For $I_{COM} = 0$ is that the CM voltage VCM is constant. When there are high frequency fluctuations in V_{COM}, the CM current I_{COM} will occur.

B. Switched Capacitor Five Level Inverter

A Switched Capacitor (SC) circuit is used in order to obtain a boost multilevel DC voltage. Between the source and the full bridge inverter a capacitor cell is inserter. The output of the multilevel inverter becomes staircase voltage waveform with the output voltage higher than the input voltage. By adding number of SC cells makes the output voltage become sinusoidal and it eliminates the harmonic content in inverter. Figure 2 shows the circuit diagram of switched capacitor five level inverter. Each SC cell consists of a capacitor and diode with two switches. Main advantage of the proposed MLI is that with less number of components the gain and level of output voltage is increased.

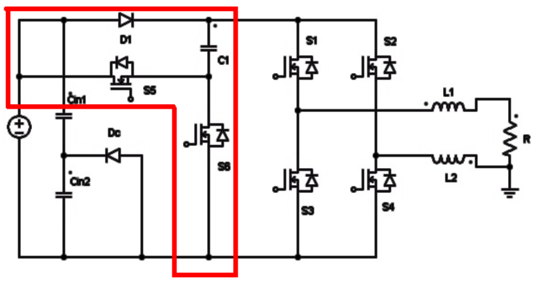

Figure 2. Switched Capacitor Five Level Inverter

C. Modes Of Operation

There are 5 modes of operation. The basic operation of the inverter is based on positive and negative cycle for the multilevel output. Output voltage level is larger than the input voltage by means of switching capacitor in parallel with voltage source.

• Mode 1

During this mode, switches S_3, S_4 and S_6 are conducting and switches S_1, S_2 and S_5 are turned OFF. Diode D_1 and D_c is forward biased. The input capacitor C_{in1} and C_{in2} are charged to the voltage $\frac{V_{DC}}{2}$. The switched capacitor C_1 is charged to V_{DC}. As shown in the Fig. 3 the output voltage $V_0 = 0$. Switches in same upper limb conduct either S_3 and S_4 or switches in the lower limb S_1 and S_2 are conducting to produce the same level of output voltage. Fig. 3 shows the equivalent circuit diagram and also different current paths are shown. The theoretical waveform of all modes is shown in Fig. 8.

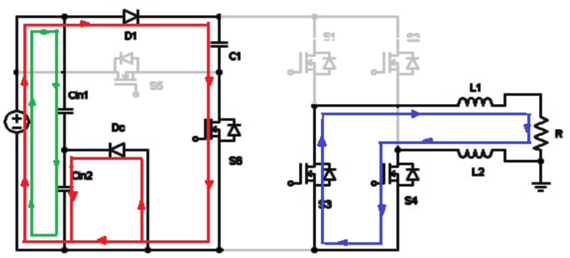

Figure 3. Operating Circuit of Mode 1

• Mode 2

It is the power transfer mode during this mode the input power will be transmitted to the grid. During this mode, switches S_1, S_4 and S_6 are conducting and switches S_2, S_3
and S_5 are turned OFF. Diode D_1 and D_C is forward biased. The input capacitor C_{in1} and C_{in2} are charged to the voltage $\frac{V_{DC}}{2}$. The switched capacitor C_1 is charged to V_{DC}. Based on the Fig. 4 the output voltage Vo = V_{DC}. Fig. 4 shows the equivalent circuit diagram of the inverter and current paths for this mode is also shown.

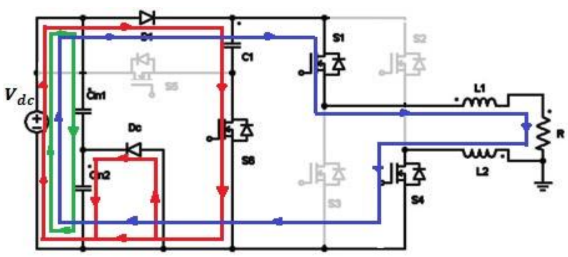

Figure 4. Operating Circuit of Mode 2

• Mode 3

It is the power transfer mode during this mode the input power will be transmitted to the grid. During this mode, switches S_1, S_4 and S_5 are conducting and switches S_2, S_3
and S_6 are turned OFF. Diode D_1 is reverse biased and D_C is forward biased. The input capacitor C_{in1} and C_{in2} are charged to the voltage $\frac{V_{DC}}{2}$. The switched capacitor C_1 is discharges to load through the switches $S_1$and S_4. Based on the Fig. 5 the output voltage Vo = $2\,V_{DC}$. Fig. 5 shows the equivalent circuit diagram of the inverter and current paths for this mode is also shown.

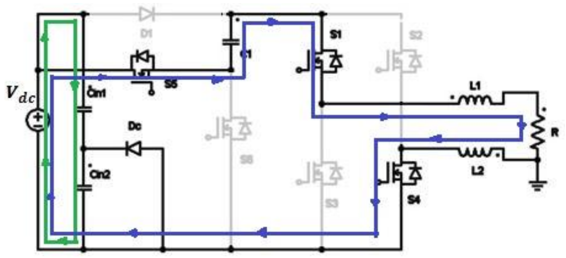

Figure 5. Operating Circuit of Mode 3

• Mode 4

It is the power transfer mode during this mode the input power will be transmitted to the grid. During this mode, switches S_2, S_3 and S_6 are conducting and switches S_1, S_4
and S_5 are turned OFF. Diode D_1 and D_C are forward biased. The input capacitor C_{in1} and C_{in2} are charged to the voltage $\frac{V_{DC}}{2}$. The switched capacitor C_1 is charges to V_{DC}. Based on the Fig. 6 the output voltage Vo = $-V_{DC}$. Fig. 6 shows the equivalent circuit diagram of the inverter and current paths for this mode is also shown.

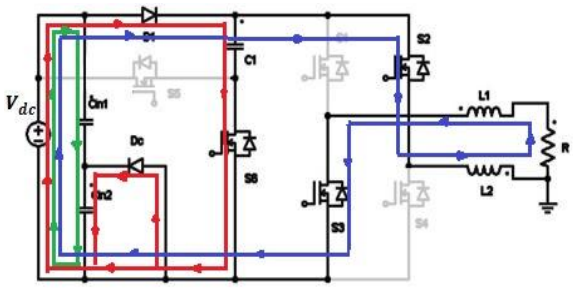

Figure 6. Operating Circuit of Mode 4

• Mode 5

It is the power transfer mode during this mode the input power will be transmitted to the grid. During this mode, switches S_2, S_3 and S_5 are conducting and switches S_1, S_4
and S_6 are turned OFF. Diode D_1 is reverse biased and D_C is forward biased. The input capacitor C_{in1} and C_{in2} are charged to the voltage $\frac{V_{DC}}{2}$. The switched capacitor C_1 is discharges to load through the switches S_2 and S_3. Based on the Fig. 7 the output voltage Vo = $-2\,V_{DC}$. Fig. 7 shows the equivalent circuit diagram of the inverter and current paths for this mode is also shown.

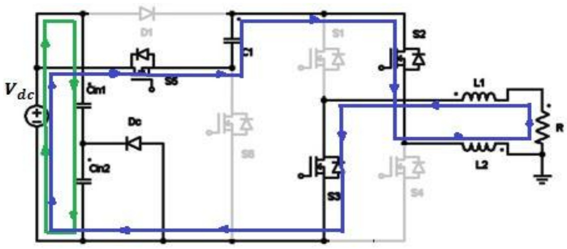

Figure 7. Operating Circuit of Mode 5

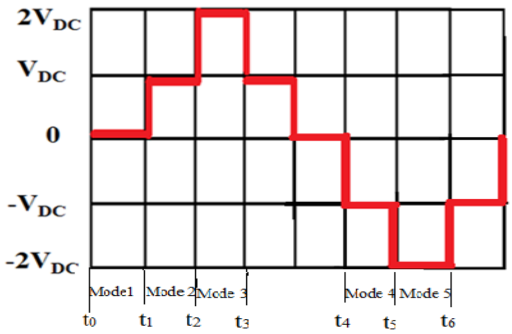

Figure 8. Theoretical wave form

III. CONTROL STRAGY

To synthesize the multilevel AC output voltage using different level of DC inputs. Semiconductor devices must be switched ON and OFF in such a way that minimize harmonics. The carrier based Phase Disposition PWM (PDPWM) modulation scheme is employed. The principle of PDPWM is to use the multiple carriers with single modulating waveform. In the PDPWM all the carrier is in phase disposition. In PDPWM all the carrier are in phase with each other and the entire carrier have the same frequency and amplitude. In this method M-1 carrier that is four carries used to generate the five level output voltage, where M is no of output voltage level. Fig. 9 shows the sinusoidal phase disposition PWM. Here four triangular waves are compared with one sinusoidal reference wave. By performing various relational and logical operations the required gate pulses are generated.

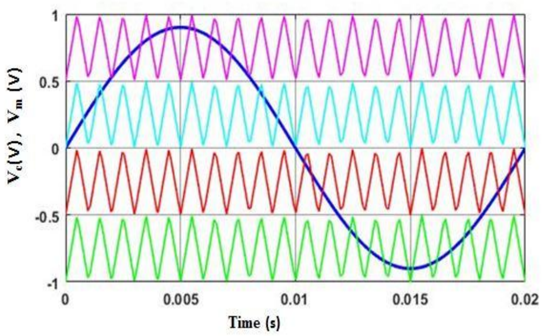

Fig. 9. Sinusoidal phase disposition PWM

The switching states of the H5-D topology with switched capacitor MLI inverter is shown in the TABLE 1. Based on the switching pattern the required gate pulses to the each switch are generated.

TABLE 1
SWITCHING STATES OF H5D-SC MLI.

V_{OUT}	S_1	S_2	S_3	S_4	S_5	S_6
$2V_{dc}$	1	0	0	1	1	0
V_{dc}	1	0	0	1	0	1
0	0	0	1	1	0	1
	1	1	0	0	0	1
$-V_{dc}$	0	1	1	0	0	1
$-2V_{dc}$	0	1	1	0	1	0

By considering the advantages of various conventional MLI topologies a new topology is being introduced. Here number of switches required for the MLI is reduced. The above theoretical explanation is verified in software by the simulink model in MATLAB.

IV. SIMULINK MODEL WITH RESULTS

MATLAB is a graphical programming language which offers modeling, simulation and analyzing of multi domain dynamic systems under Graphical User Interface (GUI) environment. It gives a real time application of the physical system by choosing the required electrical parameters for the switched capacitor multilevel inverter are listed in Table 3 the simulations are cared out. An input voltage V_{in} of 380 V is given. The switches are MOSFET/Diode with constant switching frequency of 20 kHz. Capacitor C_{in1} and C_{in2} have the same value. Also inductor L_1 and L_2 also having the same value.

TABLE 2
SIMULATION PARAMETERS

Parameters		Specification
Input voltage V_{in}		380 V
Grid voltage V_{grid} (rms)		220 V
Switching frequency f_s		20 kHz
Load resistor		150 Ω
Output Inductors	L_1, L_2	1 mH
Capacitors	C_{in1}, C_{in2}, C_1	650 μF

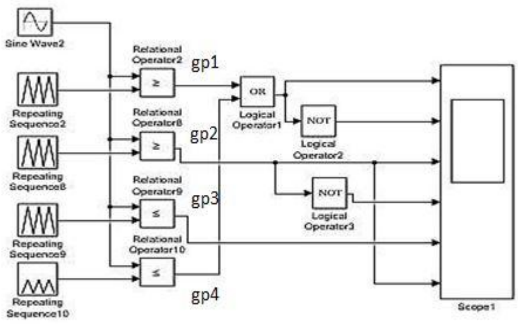

Fig. 10. Simulink Model Of the Switching Pulse Generation for improved H5D-SC

Here the triangular carrier comparing with sinusoidal reference at fundamental frequency. Triangular carrier signal which are at high frequency. Here switching frequency is 20 kHz. The simulink model is shown in Fig. 10.

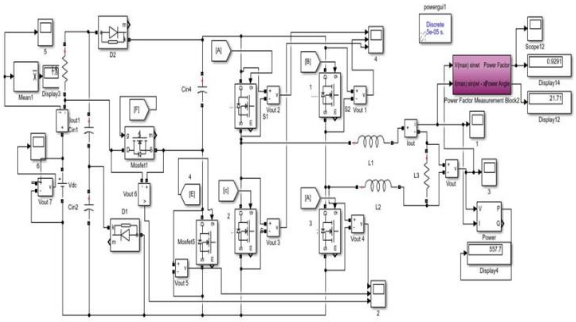

Fig. 11. Simulink Model Of the improved SC topology for transformerless PV grid connected inverter

The simulation results of the improved SC topology for inverter are simulated. Based on the design considerations. Simulation of input voltage, input current, output voltage, output current, switching pulses, common mode current are obtained from the simulink model figure 11 .

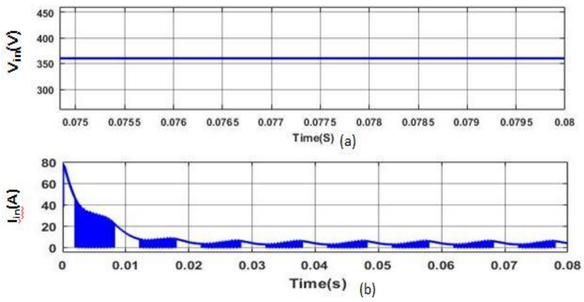

Fig. 12. (a) Input Voltage (V_{in}) and (b) Input Current (I_{in})

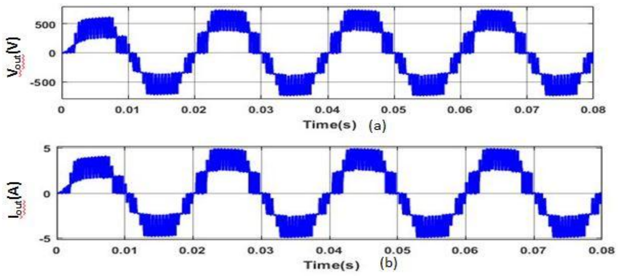

Fig. 13. (a) Output Voltage (V_{out}) and (b) IOutput Current (I_{out})

From the Fig. 12 and 13 It verifies the DC to AC conversion.

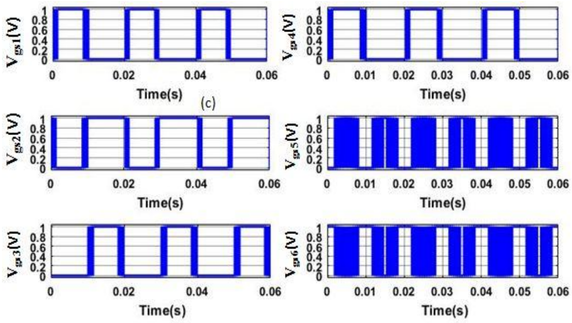

Fig. 14. Voltage across switches (a) S_1, (b) S_2 (c) S_3 (d) S_4, (e) S_5 and (f) S_6

The switching pulse based on the PWM technique. The switches are triggered accordingly to produce five level output voltage.

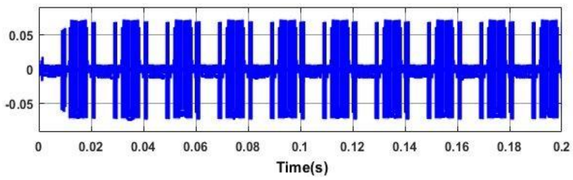

Fig. 15. Common mode current I_{cm}

The common mode current is reduced to 0.06 A.

V. ANALYSIS

The analysis is done based on the simulation studies of H5-D topology and switched capacitor boot multilevel inverter. By considering parameter like efficiency, THD, MI, power factor the analysis between these inverters is carried.

A. Efficiency Vs Output power

Efficiency is defined at any load as the ratio of the power output to the power input. The efficiency tells us the fraction of the input power delivered to the load. A typical curve for the variation of efficiency as a function of output power is shown in figure 16 and 17. For R load in H5-D inverter efficiency is around 96.5% and switched capacitor Inverter the efficiency is around 97%. For RL load in H5-D inverter the efficiency is around 96% and switched capacitor inverter the efficiency is around 96.5% respectively.

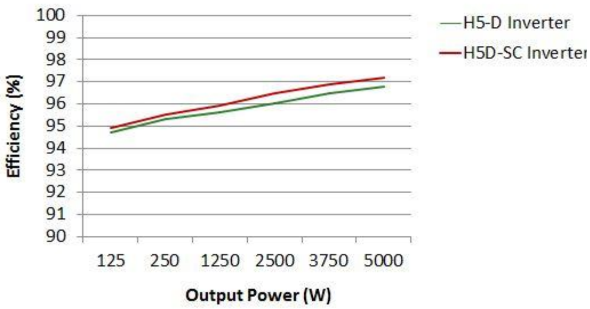

Fig. 16. Efficiency Vs Output Power R load

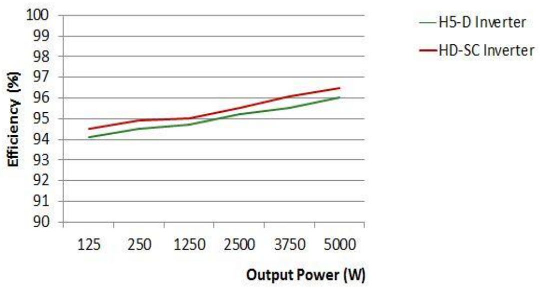

Fig. 17. Efficiency Vs Output Power RL load

B. *Power Factor Vs Output Power*

Power factor is defined as the cosine of resulting angle between the current and voltage. Taking distortion factor as unity, it is found that the maximum power factor of H-SC inverter is 0.989 and for the H5-D inverter is 0.987. The plot between power factor and output power is shown in figure 18.

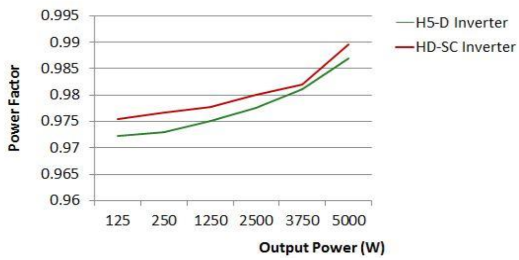

Fig. 18. Power Factor Vs Output Power

C. *FFT Analysis*

The FFT analysis is shown in Fig. 19. The THD of the H5-D inverter is obtained as 21.54 % . It shows that total harmonic distortion in the H5D-SC is 41.41% less than the H5-D topology.

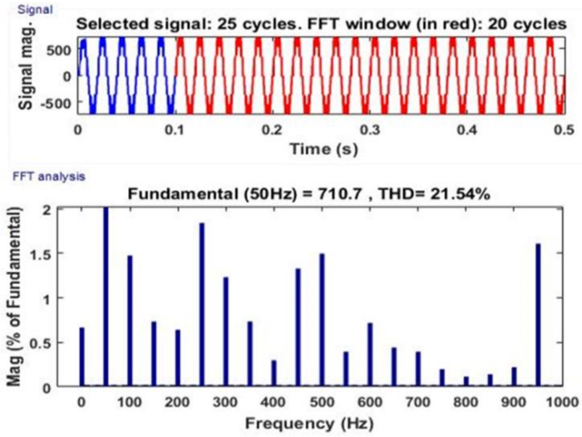

Fig. 19. THD for H5D-SC inverter

D. *Comparision*

The comparison between conventional boost converter and fly back boost converter is given in TABLE 3.

TABLE 3
COMPARISION

	Conventional Inverter	H5-D Inverter	H5D-SC Inverter
No of Switches	5	5	6
No of diodes	--	1	2
Inductor	2	2	2
Capacitor	1	2	3
Efficiency	94 %	96 %	97%
Total harmonic distortion	70.3 %	62.95%	21.54%
Common mode current	0.6 A	0.03 A	0.05A
Voltage level	V_{dc} to $-V_{dc}$	V_{dc} to $-V_{dc}$	$2V_{dc}$ to $-2V_{dc}$
Voltage stress across switch	480 V	380 V	620 V

It is observed from the above discussions that H5-D inverter has improved efficiency with less THD and also reduced the common mode current for H5-D inverter from 0.6A to 0.03A and for H-SC inverter the common mode current is reduced from 0.6A to 0.05A.

E. *Modulation Index*

The modulation index m_a is given by

$$m_a = \frac{2 * A_m}{(M-1) * A_c}$$

where A_m is the amplitude of the reference waveform and A_c is the amplitude of the carrier waveform. M is the number of level in output voltage. The output level can be controlled by ma. When M is equal to zero no modulation occurs. When M is greater than 1 it gets over modulated. So ma can be varied from 0 to 1. When m is less than 0.2 output varies from V_{DC} to -V_{DC} that is a two level output is only obtained as shown in Fig. 20.

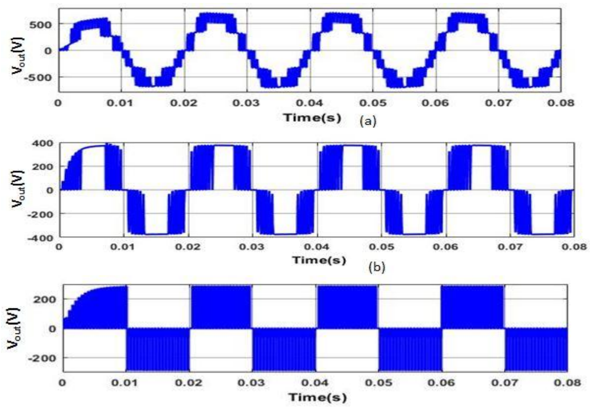

Fig. 20. Modulation index ma=1, ma=0.5 and ma=0.1

TABLE 4
COMPARISON OF THD WITH MI

LEVEL	MI	THD
TWO	0.1	311.38%
THREE	0.5	53.01%
FIVE	1	21.54%

VI. CONCLUSION

In this work, a switched capacitor multilevel inverter with low common-mode current is designed and implemented. This H5D-SC multilevel inverter uses less number of switching devices compared to conventional inverter. A H5D-SC topology and its modulation strategy can effectively suppress the CM currents of the PV inverters. Simplified method of multi-carrier modulating signal is generated. The H5D-SC inverter has a peak efficiency of 97%. THD for the improved H5D-SC multilevel inverter is minimized from 62.95% to 21.54% and reduced harmonic content in output voltage. Therefore, H5-D topology provides a good choice for single phase transformer-less PV inverters due to its simplicity and practicality. The switched capacitor multilevel inverter is suitable for different industrial applications such as in power grid application and variable frequency drives.

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