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A High Gain Bidirectional DC-DC Converter with Reduced Voltage Stress

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ABSTRACT
A 200W/1 MHz high voltage-gain two-phase bidirectional DC-DC converter can be operated in the charging mode from the DC bus to the battery and in the discharging mode from the battery back to DC bus. An interleaved topology is being used in the two phase circuit, along with a clamping capacitor that helps to reduce the voltage stress of switches. Even at very high voltage gain, voltage stress of switches can be controlled by setting the number of phases needed. Irrespective of the number of phases, the voltage stress across switches can be reduced by adding a combination of a LC^2 and a switch. The simulation and analysis of the high gain bidirectional DC-DC converter with reduced voltage stress for the forward mode (Buck mode) and the reverse mode (Boost mode) are carried out under the condition of $D \leq 0.5$. The input bus voltage is considered to be 400 V to get the output battery voltage as 35 V. In the modified reduced stress converter, voltage gain is improved. The peak efficiency is increased to 97%. The performance study of the converter is carried out in MATLAB/SIMULINK R2017a environment. Switching pulses were generated using TMS320f28335 microcontroller.

Keywords: *bidirectional converter, high voltage gain, low voltage-stress, two phase converter.*

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I. INTRODUCTION

Due to the rapidly increasing economy and enormous demand for energy, the global energy crisis has been aggravated. To deal with this energy problem, researches on environmental friendly system such as the electric vehicles and distributed power system have been carried out. In these applications, an energy storage system like a battery system must be needed to save and use energy. Thus, a bidirectional DC-DC converter (BDC) which allows transfer power between two DC sources becomes an important topic of power electronics. The BDC is categorized into an isolated converter and a non-isolated converter [1]-[7]. The demands of BDC are smaller size, lighter weight and higher efficiency etc. In order to minimize the size of BDC, the switching frequency must be increased. Batteries and ultra-capacitors are Energy storage systems (ESSs) used to store energy when there is an over-supply of power, these then serve as power supplies when the supply from the renewable energies is low [8]. ESSs can be charged via a bidirectional converter which is in the charging mode and ESSs can be discharged to a DC load through the same converter which is now operated in discharging mode. Many applications such as electric vehicles and the distribution systems uses low-voltage ESSs. Due to high efficiency and low cost, the bidirectional buck-boost converter has been discussed in both low and medium applications. But, for some applications that require high voltage, this converter cannot operate well because of the limitation of the duty ratio systems uses low-voltage ESSs. The voltage stress on the switches is also a big issue because of the requirement of high input voltages for many applications. A bidirectional three-level DC-DC converter has been proposed in [10], in which the voltage gain is limited and requires a complicated controller to balance the clamping capacitor voltage.

This paper proposes a new topology of the high voltage-gain bidirectional two phase converter which uses the interleaved methodology. The voltage stresses of switches can be higher due to the higher input voltages. However voltage stress is reduced because of the clamping capacitor and the two phases. The more phases employed, the lower voltage stress of power switches is. Voltage stress on these switches can be further reduced by adding a combination of LC^2 and a switch. Also it helps to

improve the voltage gain.

II. HIGH-GAIN BDC WITH REDUCED VOLTAGE STRESS

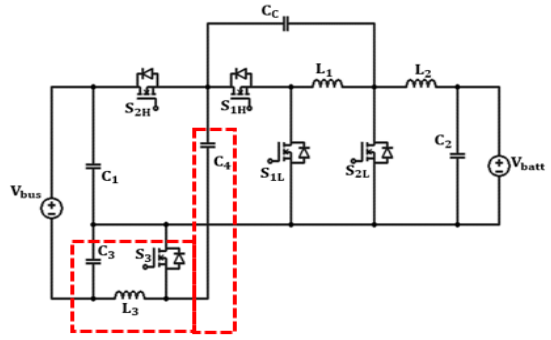

Fig. 1. High Gain Bidirectional DC-DC Converter with Reduced Voltage Stress

The schematic diagram of the high voltage gain BDC is shown in Fig. 1. The converter features three inductors (L_1, L_2 and L_3), five switches (S_{1H}, S_{2H}, S_3, S_{1L}, and S_{2L}), a clamping capacitor C_C, and the input and output capacitors. The DC bus voltage and battery voltage are denoted by V_{bus} and V_{batt}, respectively. The The duty ratio of the high side switches S_{1H}, S_{2H} and S_3 is denoted as D, whereas the ON time of the complementary switches is (1-D)T_s. The voltage stress across the switches increase with rise in the bus voltage. In order to reduce the voltage stress across the switches, a combination of LC^2 and a switch S_3 are added to get the high-gain bidirectional DC-DC converter with reduced voltage stress as shown in Fig. 1.
Operating modes of the converter are discussed below with the theoretical waveform shown in Fig. 6.

A. BUCK MODE (FORWARD MODE)

MODE 1 [t_0 – t_1], MODE 2 [t_1 – t_2] : In mode 1, the switches S_{2H}, S_3 and S_{1L} are ON and switches S_{1H} and S_{2L} are OFF, as shown in Fig. 6(a). Inductor L_1 is demagnetized by the voltage (V_C - V_{bus}) and inductor L_2 is magnetized by the voltage (V_{bus} - V_C - V_{batt}). Inductor L_3 is magnetized. The battery V_{batt} is supplied from the two inductors. Fig. 2 shows the equivalent circuit diagram of mode 1 and mode 2 along with the current paths.

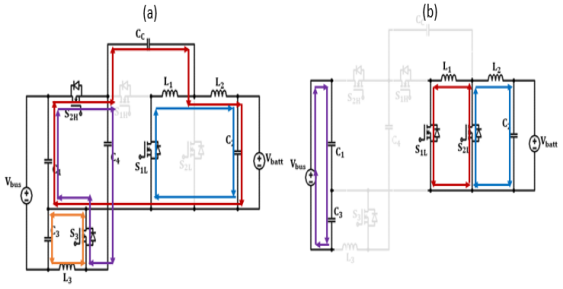

Fig. 2 Operating circuit in a)Mode 1, b)Mode 2

During mode 2, the high-side switches S_{1H} and S_{2H} are turned OFF. Therefore, the low-side switches S_{1L} and S_{2L} are ON as shown in Fig. 6(a). The voltage stress on inductor L_1 is zero, and this current is then circulated. Inductor L_2 is demagnetized by the voltage ($-V_{batt}$). Moreover, the voltage stress on the switches S_{1H} and S_{2H} is V_C and (V_{bus} - V_C), respectively.

MODE 3 [t_2 – t_3], MODE 4 [t_3 – t_4] : Switch S_{1H} is turned ON, and S_{2H} is turned OFF, as seen in Fig. 6(a). Inductor L_1 is charged by the clamping capacitor C_C and inductor L_2 remains demagnetized by the voltage ($-V_{batt}$). Fig. 3 shows the equivalent circuit diagram of mode 3 and mode 4 along with the current paths. Mode 4 is the same as mode 2 with the reverse flow direction of $i_L(t)$.

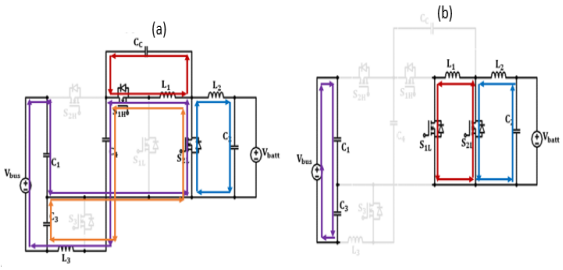

Fig.3 Operating circuit in a)Mode 3, b)Mode 4

B. BOOST MODE (REVERSE MODE)

MODE 1 [t_0 – t_1], MODE 2 [t_1 – t_2] : In mode 1, switches S_{2H} and S_{1L} are ON and switches S_{1H} and S_{2L} are OFF, as shown in Fig. 6(b). Inductor L_1 is magnetized by the voltage (V_C -V_{bus}) and inductor L_2 is demagnetized by the voltage (V_{bus} - V_C - V_{batt}). The battery V_{batt} is supplied from the two inductors. Fig. 4 shows the equivalent circuit diagram of mode 1 and mode 2 along with the current paths.

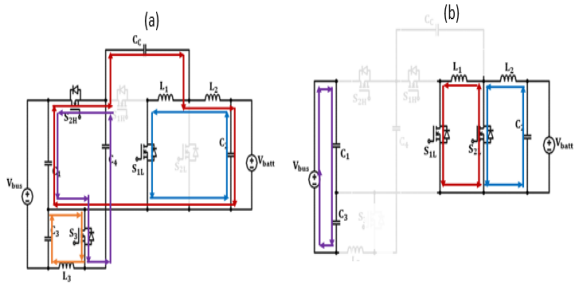

Fig.4 Operating circuit in a)Mode 1, b)Mode 2

During mode 2, the high-side switches S_{1H} and S_{2H} are turned OFF. Therefore, the low-side switches S_{1L} and S_{2L} are ON as shown in Fig. 6(b). The voltage stress on inductor L_1 is zero, and this current is then circulated. Inductor L_2 is demagnetized by the voltage ($-V_{batt}$). Moreover, the voltage stress on the switches S_{1H} and S_{2H} is V_C and (V_{bus} - V_C), respectively.

MODE 3 [t_2 _ t_3], MODE 4 [t_3 _ t_4] : Switch S_{1H} is turned ON, and S_{2H} is turned OFF, as seen in Fig. 6(b).

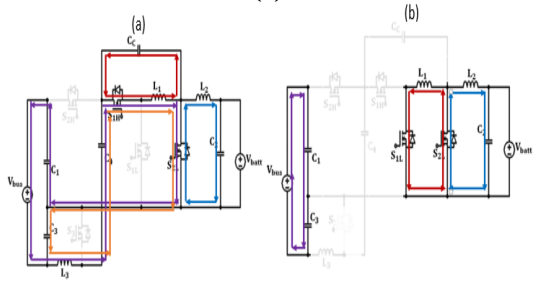

Fig.5 Operating circuit in a)Mode 3, b)Mode 4

Inductor L_1 is discharged by the clamping capacitor C_C and inductor L_2 remains magnetized by the voltage ($+V_{batt}$).Fig. 5 shows the equivalent circuit diagram of mode 3 and mode 4 along with the current paths. Mode 4 is the same as mode 2 with the reverse flow direction of $i_{L2}(t)$ as seen from Fig. 6(b).

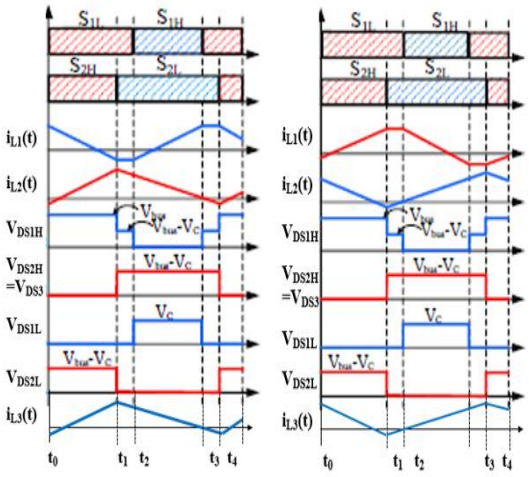

Fig. 6 Theoretical Waveform of the Converter (a)Buck mode (b)Boost mode

III. DESIGN OF COMPONENTS

The input voltage is taken as 400 V. The pulses are switched at the rate of 1 MHz with a duty ratio of 0.24 for S_{1H}, S_{2H}, S_3. S_{1H} is phase shifted by 180^0 from S_{2H}. S_{1L} and S_{2L} are complimentary switches of S_{1H}, S_{2H} with a duty ratio of 0.76. The design is done so as to get an output of 48V/200W.

A. Duty Ratio, D

Taking V_{bus} as 400 V, V_{batt} as 48 V. Take f_{sw} as 1 MHz, P_{max} as 200 W. Duty ratio of switches S_{1H} and S_{2H} is calculated as,

$$D = 2 * \frac{V_{batt}}{V_{bus}} = 0.24 \qquad (1)$$

Hence the duty ratio of switches S_{1H} and S_{2H} is set at 24% duty ratio of complimentary switches S_{1L} and S_{2L} is set at
76 % .

B. Design of inductors L_1, L_2, L_3

At the transition of 40 % output power, the output current can be defined as,

$$I_{out} = \frac{40\% P_{max}}{V_2} = 1.67\ A \qquad (2)$$

$$L_1 = \frac{V_C D T_S}{I_{out}} = 28.7\ \mu H \approx 22\ \mu H \qquad (3)$$

$$L_2 = \frac{V_{batt}(1-D)T_S}{2I_{out}} = 10.9\ \mu H \approx 11\ \mu H \qquad (4)$$

Design of inductor L_3 is same as that of inductor L_2. Thus the value of inductor L_1 is set as 22 µH, L_2 and L_3 is set as 10µH.

C. Design of Clamping Capacitor cc

Assuming maximum output voltage ripple as 1 V,

$$C_C > \frac{I_c * \Delta t}{\Delta V_c} = 0.5\ \mu F \approx 1 \mu F \quad (5)$$

Thus the value of clamp capacitor is set as 1 µF.

D. Design of Capacitance c1,c2,c3,c4

Taking ripple current as 20 % of actual output current and ripple voltage as 0.8 V.

$$C = \frac{I_{high}(1-D)}{F_S * \Delta V_O} = 1.58\ \mu F \quad (6)$$

$C_1=C_2=C_3=C_4=C$

Hence set the value of capacitors as 1.58 µF.

E. Design of R0

Taking P_o as 200 W and output voltage as 48 V, the load resistance is calculated as,

$$R_O = \frac{{V_O}^2}{P_O} = 11.52\ \square \quad (7)$$

IV. SIMULINK MODEL AND SIMULATION RESULTS

The simulation parameters for the high gain BDC with reduced voltage stress is given in Table 1.

Table-I: Simulation Parameters

Parameters	Specification
DC-bus voltage	400 V
Battery voltage	35 V
Maximum power	200 W
Switching frequency	1 MHz
Inductor	22 µH, 10 µH, 10 µH
Filter inductor	1.5 H
Clamp capacitor	1µF
Capacitor	1.6 µF

In buck mode, an input voltage V_{bus} of 400 V gives an output battery voltage V_{batt} of 35 V for an output power P_o of 200 W. In boost mode, the reverse occurs and V_{batt} of 35 V yields an output V_{bus} of 400 V. The switches are MOSFETs with constant switching frequency of 1 MHz and duty ratio of 0.24 for S_{1H}, S_{2H}, S_3, 0.76 for their complimentary switches S_{1L}, S_{2L} respectively. Gate pulses of S_{1H}, S_{2H} are phase shifted by 180^0. The high voltage gain BDC with reduced voltage stress in buck mode is simulated in MATLAB/SIMULINK by choosing the parameters listed in Table 1. Simulink model is shown in Fig. 7.

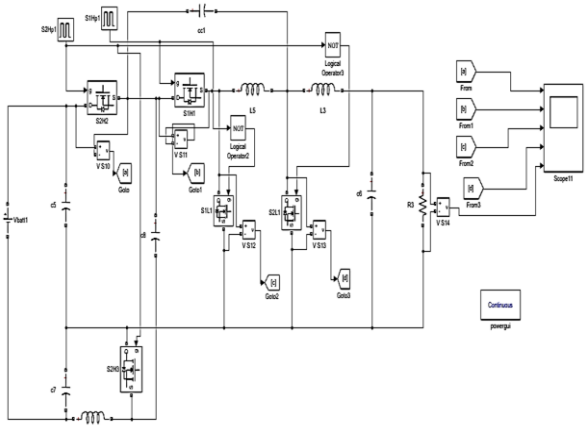

Fig. 7. Simulink model of high gain BDC in buck mode

The simulation results of the high gain BDC with reduced voltage stress in buck mode are shown in the following figures.

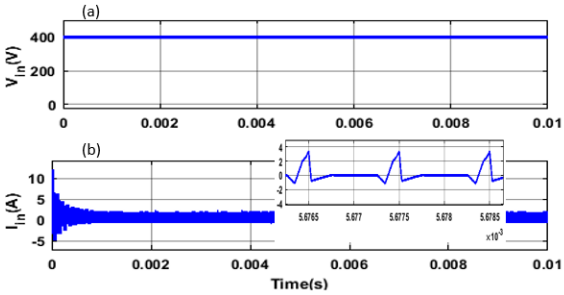

Fig. 8. (a) Input Voltage (V_{in}) and (b) Input current (I_{in})

In buck mode, an input bus voltage of 400 V is given, so the input current circulated is about 2 A as seen from Fig. 8. It can be seen that a 400 V is stepped down to get 35 V at the output side as seen in Fig. 9. Output voltage ripple is observed to be 0.4 V. The output current waveform is same as that of I_{L2}.

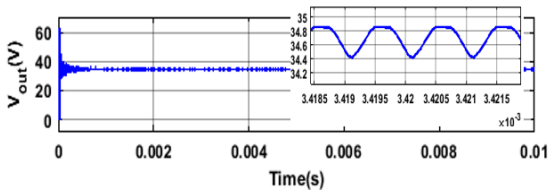

Fig. 9. Output Voltage (Vout)

The switching frequency is kept at 1 MHz. The gate pulse of S_{1H} and S_{2H} has a fixed duty cycle of 24 % with a magnitude of 10 V as shown in Fig. 10 and 11. For an input of 400 V, the voltage stress across the switch S_{1H} of two levels are reduced to 300 V, 150 V as seen from Fig. 10(b). The voltage stress across S_{2H} is 150 V as seen from Fig.11(b).

Gate pulse to switch S_3 is same as for S_{2H}.

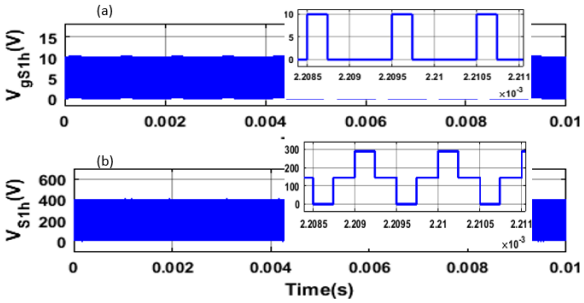

Fig. 10. (a) Gate pulse to switch S1H (b)Voltage across switch S1H

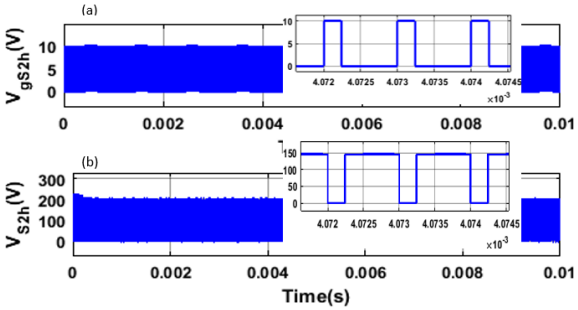

Fig. 11. (a) Gate pulse to switch S_{2H} (b) Voltage across switch S_{2H}

Since the switches S_{1L} and S_{2L} are the complimentary switches of S_{1H} and S_{2H}, their gate pulses are of with duty ratio of 76 %. The voltage stress across the switches S_{1L} and S_{2H} is 150 V.

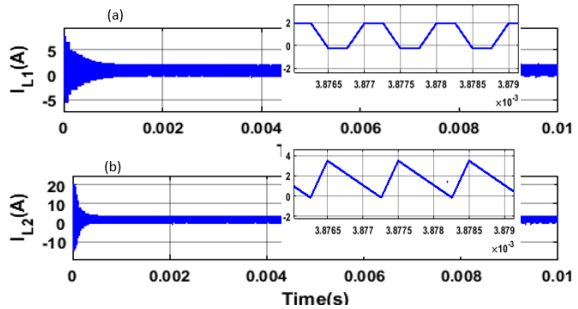

Fig. 12. (a) Current through inductor L_1 (b) Current through inductor L_2

Inductor current waveforms in the forward mode are shown in Fig. 12(a) and (b). The average inductor current I_{L1} is always equal to half of the output current, whereas the average inductor current I_{L2} is same as the output current. I_{L1} and I_{L2} are measured as 9 A, 18 A respectively. Because of the inductor L_2 in the battery side, the current ripple of the output is very small and it is very safe for battery charging.

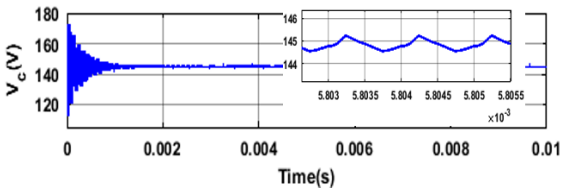

Fig. 13. Voltage across clamping capacitor C_C

I_{L1} forms a trapezoidal waveform since during modes 2 and 4, the voltage stress on inductor L_1 is zero and hence current is circulated. Current waveform through the inductor L_3 is similar to that of L_2. Clamping capacitor voltage V_C is half of the input voltage V_C is measured as 196 V as seen in Fig.13.
Simulink model of BDC in boost mode is shown in Fig. 14.

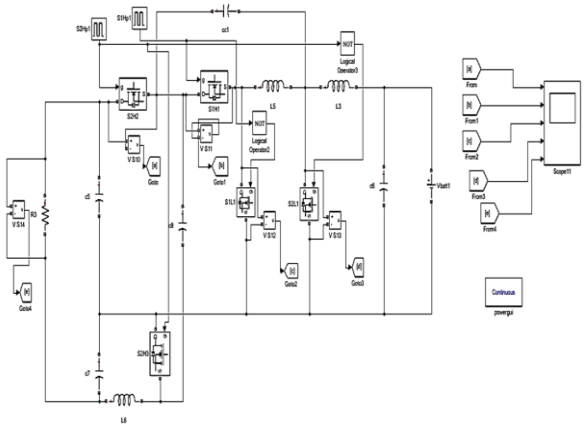

Fig. 14. Simulink model of high gain BDC in boost mode

The simulation results of the high gain BDC with reduced voltage stress in boost mode are shown below. During boost mode, an input battery voltage of 35 V is given, so the input current circulated is about 6 A as shown in Fig. 15(b).

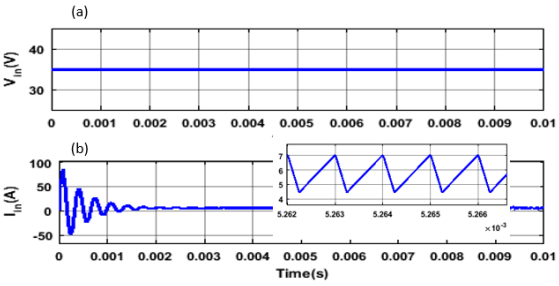

Fig. 15. (a) Input Voltage (Vin) , (b) Input current (Iin)

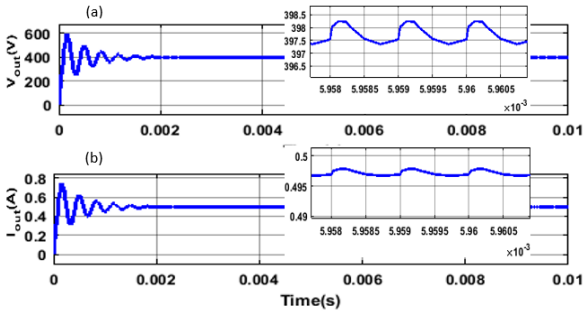

Fig. 16. (a) Output Voltage (V_{out}) , (b) Output Current(I_{out})

It can be seen that the 35 V is stepped up to get 393 V at the output side as shown in Fig. 16(a). Output voltage ripple is observed to be 1 V. Output current is measured to be 0.48A, output current ripple is measured to be 0.02 A as shown in Fig. 16(b). The gate pulse of S_{1H} and S_{2H} has a fixed duty cycle of 24 % with a magnitude of 10 V as shown in Fig. 17 and 18 same as given in buck mode.

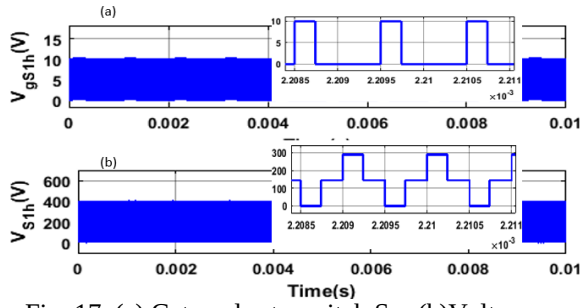

Fig. 17. (a) Gate pulse to switch S_{1H} (b)Voltage across switch S_{1H}

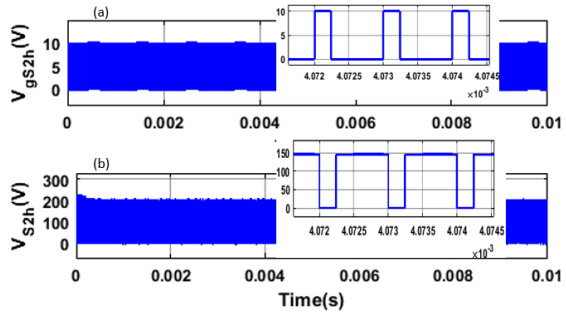

Fig. 18. (a) Gate pulse to switch S_{2H} (b)Voltage across switch S_{2H}

Since the switches S_{1L} and S_{2L} are the low side and complimentary switches of S_{1H} and S_{2H}, their gate pulses are of with duty ratio of 76 % same as given in buck mode.

The voltage stress across switch S_{1L} and S_{2L} are is 145 V 150 V respectively. Inductor current waveforms are shown in Fig. 19. Inductor current waveforms are reversed from that of the buck mode. I_{L3} is measured to be 4 A .

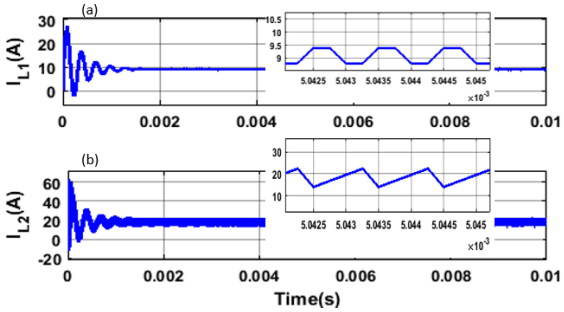

Fig. 19. (a) Inductor current (I_{L1}) (b) Inductor current (I_{L2})

V. ANALYSIS

The analysis of high - gain 1 MHz bidirectional DC-DC converter and high gain bidirectional DC-DC converter with reduced voltage stress is carried out by considering the parameters like P_{out} and efficiency.

A. Efficiency Vs Output power

Efficiency of a power equipment defined at any load is the ratio of output power to the input power. Comparison curves for the variation of efficiency as a function of percentage of output power for the conventional bidirectional converter and modified converter is shown in Fig. 20.

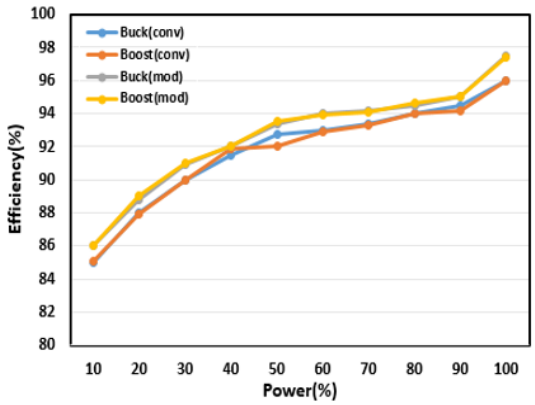

Fig. 20. Efficiency curves for buck and boost modes of conventional BDC and modified BDC for R load

For the conventional BDC, at nominal 400 V bus voltage and 48 V battery voltage, peak efficiency of around 96 % is obtained for both buck and boost modes. For the modified BDC, at nominal 400 V bus voltage and 35 V battery voltage, peak efficiency of around 97 % is obtained for both buck and boost modes.

B. Power Loss distribution

The plot of power loss calculated across the components of high-gain bidirectional DC-DC converter is shown in Fig. 21. A total power loss of 14.06 W is thus obtained.

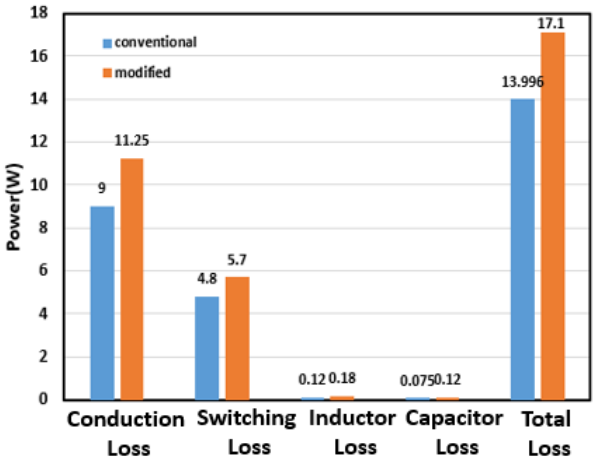

Fig. 21. Power loss distribution across converter

VI. CONCLUSION

The high-gain bidirectional DC-DC converter with reduced voltage stress offers superior overall performance over the conventional two phase bidirectional DC-DC converter. The voltage stress across the switches are significantly reduced. The peak efficiency can reach 97 % . The converter maintains the interleaved methodology and the two phase structure. The voltage gain for the boost mode is improved. The converter is operated at a high frequency of 1 MHz, hence the size of the components are less. This converter has many industrial applications. It can be used as an interface between battery and ultracapacitor in battery-ultracapacitor hybrid systems for electric vehicles. The converter allows stable charging and discharging of battery for electric vehicle applications. Another application is that, converter can be worked in the charging mode from PV system to the Energy Storage Devices (ESSs) and controlled to discharge energy back from ESSs to the DC-load.

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