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Survey on Power Optimization Techniques for Low Power VLSI Circuit in Active & Standby Mode of Operation

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ABSTRACT
CMOS technology is the key element in the development of VLSI systems since it consumes less power. Power optimization has become an overridden concern in deep submicron CMOS technologies. Due to shrink in the size of device, reduction in power consumption and over all power management on the chip are the key challenges. For many designs power optimization is important in order to reduce package cost and to extend battery life. In power optimization leakage also plays a very important role because it has significant fraction in the total power dissipation of VLSI circuits. This paper aims to elaborate the developments and advancements in the area of power optimization of CMOS circuits in deep submicron region. This survey will be useful for the designer for selecting a suitable technique depending upon the requirement.

KEYWORDS: leakage power, low power, voltage scaling, power gating, transistor stacking, adiabatic logic.

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I. INTRODUCTION

Energy efficiency is the critical feature of modern electronic systems, due to desirability of portable devices, demand for reliability and performance, to extend battery life, need to reduce package cost, to reduce Green cost etc. Advancements in scaling with reduced threshold and supply voltages lead to increased leakages in MOS transistors. Many studies presented that leakage power consumption is up to 40% of total power consumption in nanometre technology. To overcome the power dissipation problem many researchers have proposed different ideas from the device level to the architectural level. However, there is no universal way to avoid trade-offs between power, delay and area. Thus, designers are required to choose appropriate techniques that satisfy application and product needs. In VLSI circuits, to control the power consumption supply voltage plays an important role. Supply voltage scaling without scaling of threshold voltage degrades the performance of the device. The reduction of threshold voltage and supply voltages proportionally retains the performance. The threshold voltage reduction leads to five times higher leakage current. The requirements for power optimization continue to increase significantly and the motivations to optimise power differ from application to application. Power consumption has become primary design issue and needs suitable power management in the design of digital circuits where switching and standby mode affects the performance of system. The design of a low power circuits mainly focuses on a problem occurred due to the performance, power dissipation and chip area.

This paper is organised as follows in section I we discussed about the sources of power dissipation in CMOS. In section II we mention the power optimization at different levels of abstraction broadly. In section IIII we focussed on different power optimization techniques. In section IV we presented the advanced power recovery technique and in section V we concluded about the selection of different techniques for different approaches.

II. POWER DISSIPATION IN CMOS

Sources of Power Consumption

The main sources of power consumption, that affect CMOS circuits are dynamic power and standby power.

The following equations define the power within the device:

$P_{total} = P_{dynamic} + P_{short} + P_{leakage}$ $P_{dynamic} = \alpha * C * Vdd^2 * f$

$P_{short} = \alpha(\beta/2)(V-2V_{th})^3 * f * T_{rf}$ $P_{leakage} = (I_{diode} + I_{subthreshold}) * V_{dd}$

α = Switching Activity, C = Total Load Capacitance, V_{dd}= Supply Voltage f = clock Frequency, β= Gain Factor, T_{rf} = Rise/Fall Time

(gate inputs), Vth = Threshold Voltage.

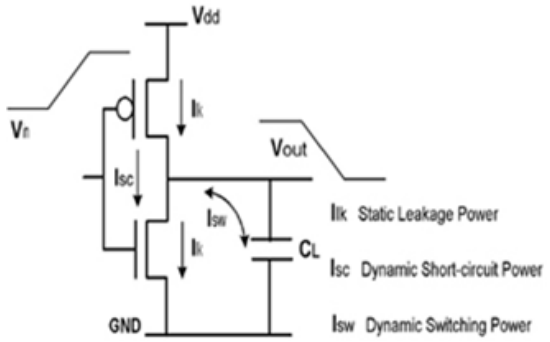

Fig:1 Sources of Power Consumption in CMOS

Dynamic power or active power is the power consumed by the device when it switches from one state to another state actively. It consists of switching power due to charging and discharging the loads on the device and short circuit power, consumed during output transitions due to current flowing from the supply to ground. Leakage power is actually consumed when the device is both static and switching, but generally the main concern with leakage power is during inactive state of device. This is the power which should be concentrated more in deep submicron design of device as it exponentially depends on size of the device. Fig.1 shows both dynamic power and leakage power consumption that occur in CMOS circuits. In deep submicron technology sub- threshold leakage current is problematic because it increases as transistor threshold voltages (Vth) decrease. At 90 nm, leakage power can represent as much as 50 percent of the total power consumed by a chip, depending on the design. In addition, high leakage power can exponentially increase reliability related failures, even in standby which is represented in fig 2.

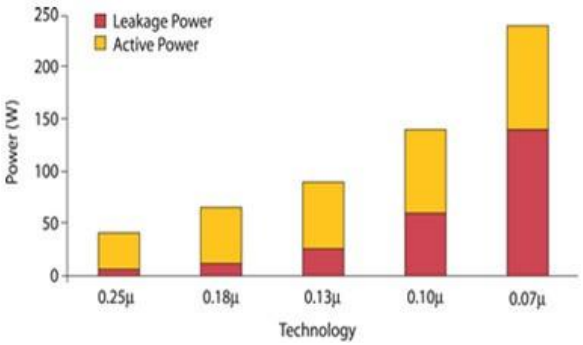

Fig.2 Leakage power and active power at different deep submicron CMOS technologies.

III. OPTIMIZATION AT DIFFERENT LEVELS OF ABSTRACTION

An integrated low power methodology requires optimization at all design abstraction levels as mentioned below.

3.1 System level

Qiaing Tong et al discussed about power optimization at system level. System level design consists of the mapping of a high-level system model on to an architecture. in order to achieve about 75 % of power optimization different processing algorithms and architectures are needed with proper executable specifications. The choice of algorithm used can impact the power cost because it determines the runtime complexity of a program. Some of the techniques used for system level power optimization are Adaptive Voltage Scaling (AVS), Memory access reduction, branching reduction, Loop unrolling and combining, Loop unrolling and combining Hardware are preferable.

3.2 Algorithm level

Chetan Sharma et al discussed that power consumption at algorithm level relates the proper choice of algorithm, word length, modular interfaces, technology implementation, software and hardware selection, and behavioural constrains and trade-off will minimise the power requirement. The algorithm which is more useful is which have minimum number of operations because it will require less hardware. By increasing concurrency, we can increase efficiency of that device.

3.3 Architecture level

Chetan Sharma et al discussed that impact of low-power techniques on the architecture level can be more significant than at the gate level. He mentioned the techniques parallelism, pipeline, distributed processing and power management, can be used to reduce the power dissipation at architecture level. The techniques like both parallelism and pipelining can optimise the power an at the expense of area while maintaining the same throughput. The combination of pipelining and parallelism can result in further power reduction, because the power supply voltage can be reduced aggressively and also, he mentioned by multiple frequency and voltage islands, reduction in switching activity and through logic transformations approaches can be implemented at architecture level to reduce the consumption of power.

3.4 Gate level

Amberly Babu et al discussed that at gate level we get accurate verification of power consumption. Up to 20%of power can be saved by

implementing clock gating, power gating, clock tree optimization techniques. at gate level also we can employ logic level transformations to reduce switching activity there by reducing power consumption.

3.5 Transistor level

Sumitha Gupta et al mentioned that advanced process can built transistors with different threshold voltages. Up to 30% of power can be saved by using a mixture of CMOS transistors with multiple threshold voltages. There are two different thresholds are available, generally called high Vth and low Vth. High threshold transistors are slower but leak less, and can be used in non- critical circuits.

Fig.3 shown below gives the details of power saving, speed and error trade off at different level of abstraction

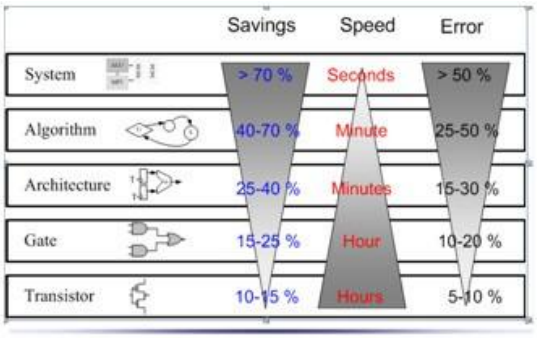

Fig.3. Power optimization at different levels of Abstraction with power saving speed and error [9]

IV. POWER OPTIMIZATION TECHNIQUES

4.1 Static Power Reduction Techniques

There are various leakage power reduction techniques based on modes of operation of systems. The two operational modes are a) active mode and b) standby (or) idle mode. To minimize this power, technology scaling, voltage scaling, clock frequency scaling, reduction of switching activity, etc., were widely used.

4.1.1 Multi-Vth optimization/ (Multi Threshold - MTCMOS):

P. Sreenivasulu etal discussed that MTCMOS (Multiple Threshold CMOS) is very effective technique in reducing leakage currents in the standby mode. This technique utilizes transistor with multiple threshold voltages(V_{th})to optimise power and delay. Here low voltage devices were used in critical delay paths to minimize clock periods. Higher voltage devices were used on non-critical paths to reduce static leakage power without incurring a delay penalty.

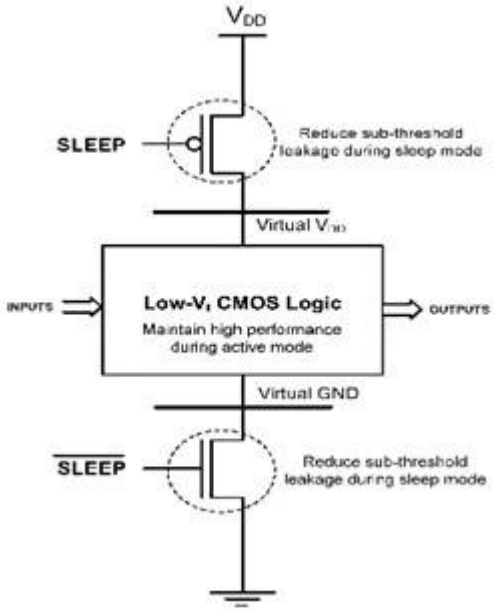

Fig.4 MTCMO Stechnique [10]

He also discussed that this technique reduces several orders of magnitude reduction in leakage power through two effects. First. if the original CMOS circuit effective leakage width is reduced to the width of the single "off" nMOS Transistor second the increase in an exponential reduction in leakage power can be achieved due to increased threshold voltage. in this if the sleep transistor is turned off more strongly further reduction in leakage can be achieved.

4.1.2 Transistor Stacking

Narendra et al, showed that stacking of two OFF transistors which significantly reduce sub-threshold leakage compared to a single OFF transistor. It is an effective way toreduce leakage power in active mode. Transistor stacking technique uses the dependence of Isub on the source terminal voltage Vs. With the increase of Vs of the transistor, the subthreshold leakage current reduces exponentially. If natural stacking of transistors does not exist in a circuit, then to utilize the stacking effect a single transistor of width W is replaced by two transistors each of width W/2. This is called forced stacking as shown in Figure 5.

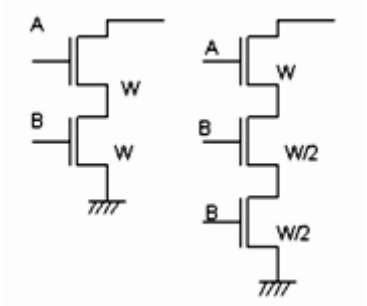

Fig.5 Forced Stacking Circuit

4.1.3 Sleepy Stack Approach

J.C. Park et al, described a sleepy stack technique which combines the sleep transistor approach during active mode and the stack approach during standby mode. In this technique, forced stacking is first implemented. Then to one of the stacked transistors a sleep transistor is inserted in parallel. Thus, during active mode, the sleep transistors are on thereby reducing the effective resistance of the path. This leads to reduced propagation delay during active mode as compared to the forced stacking method. During standby mode, the sleep transistor is turned off and the stacked transistor suppresses the leakage power. Figure 6 shows the circuit of a sleepy stack inverter, where the S and S' are sleep control signals.

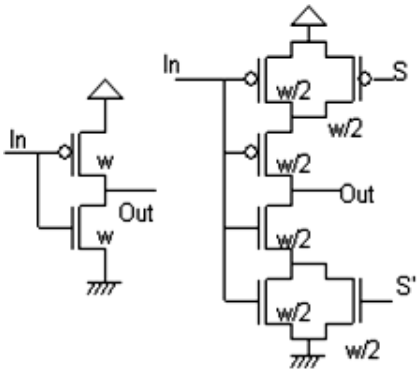

Fig.6 sleepy stack inverter circuit

4.1.4 Sleepy Keeper Approach

Ajay Kumar dadoria et al proposed sleepy keeper approach. In this approach two extra transistors are used in parallel with sleep transistor. Over the pull up network we are using MOS transistor which is drive by the feedback of the output circuit and PMOS transistor in pull-down network. In this technique two transistors are connected in parallel with sleep transistor. Above the pull up network NMOS transistor is used. For this input is given from the feedback of the output circuit. PMOS transistor is used in pull down network. It maintains proper output logic since it is using feedback technique and here we can use higher Vth transistors for further reduction of static power.

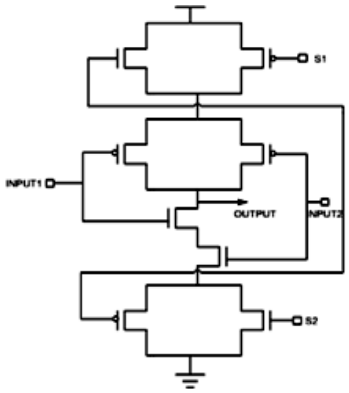

Fig.7. Two input NAND gate with sleepy keeper technique [13]

Then Ajay Kumar dadoria et al proposed Modified galeor with sleepy with low and high Vth transistors. in this the modifications are the gate of NMOS and PMOS galeor transistor has been connected to the drain and instead of using low Vth NMOS galeor transistors high Vth transistors are used. in this approach proper voltage swing is achieved by changing the position if inputs of galeor transistors and applying high threshold to sleep transistors. This advantage achieved by this technique.

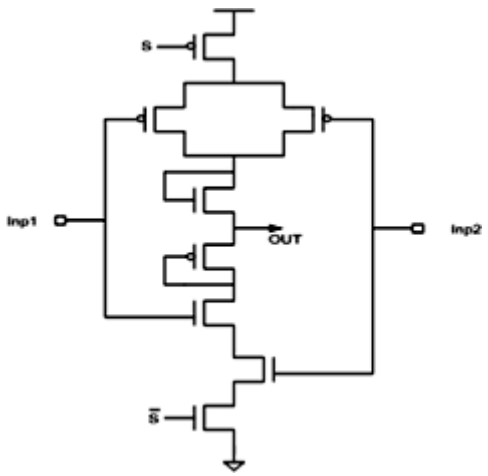

Fig.8 NAND gate with galeor with sleepy approach

4.1.5 Lector approach

Narender Hanchate et al, proposed a novel technique called LECTOR (Refer Fig. 6) for reducing leakage power in CMOS circuits. He introduced two leakage control transistors(LCT) a PMOS and NMOS within the logic gate. The gate terminal of each LCT is controlled by the source of the other. In this arrangement, one of the LCT's is always near its cut off voltage for any input combination. This increases the resistance of the

path from Vdd to ground leading to significant decrease in leakage currents. This technique works effectively in both active and idle states of the circuit, resulting in better leakage reduction. The experimental results indicate an average leakage reduction of 79.4% for MCNC "91benchmark circuits.

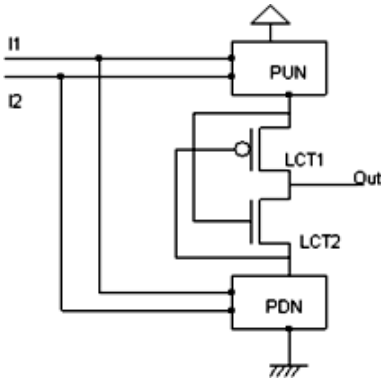

Fig.9 LECTOR technique

4.1.6 Body Bias Technique

Xin He Al-Kadry et.al, proposed a novel concept to control power dissipation in VLSI processors. This paper emphasizes on adaptive leakage control using body bias technique to reduce the power dissipation of the 65 nm MOS devices. Through adding forward body biasing, the leakage is reduced in sub-100 nm CMOS devices (unlike above-100 nm devices) while slightly increasing the signal propagation delay. For the conditions where the circuit does not use up the entire clock cycle, this slack can be used to reduce the power dissipation without any loss in performance. The fact that the circuit delay remains less than the clock period provides the opportunity to reduce power consumption of VLSI circuits. The objective is to change the voltage of the body bias to reduce leakage, allowing the circuit to consume less power whenever the clock edge can be met as detected beforehand.

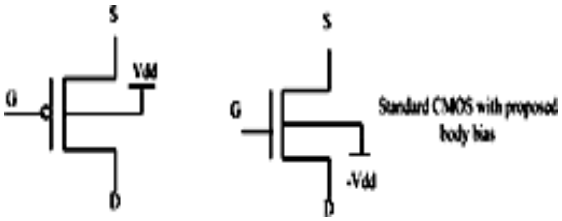

Fig.10 Body connections of MOS devices [15]

4.2 Dynamic Power Optimization Schemes

4.2.1 Clock gating

Dushyant Kumar Soni et al proposed clock gating which reduces dynamic power dissipation. in typical synchronous circuit such as general-purpose microprocessor, only some portion of the circuit is active at a given time. Hence by making remaining portion idle the power consumption can be reduced. one way is to masking the clock going to idle portion. He proposed a new scheme for the same purpose by using tri state buffer and gated logic is used which is designed by the combination of double gated with bundled inputs respectively.

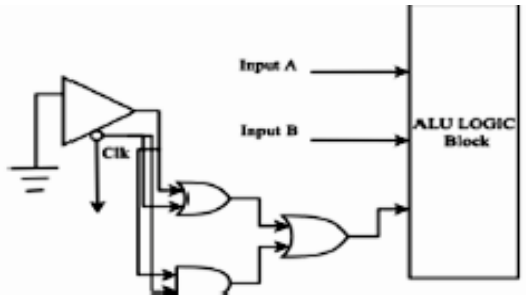

Fig.11. Clock Gating Technique [15]

The power is saves in such a way that if target device clock is ON the controlling devices clock is OFF and vice versa in this technique the clock and dynamic power is saved during negative edge of clock as this technique is designed for positive edge. This technique by implementing on synchronous circuits power is saved up to 20% and also reduces the hardware complexity.

4.2.2 Dual VDD

V.Sai Sri Harsha discussed A Dual VDD Configuration Logic Block and a Dual VDD routing matrix is shown in figure.12. In this technique the supply voltage of t e logic and routing blocks are programmed to reduce the power consumption .it can be done by assigning low-VDD to non-critical paths in the design. But whenever two di ferent supply voltages co- exist, static current flows at the interface of the VDDLv part and the VDDH part. Level converters can be used to up convert a low VDD to a high VDD.

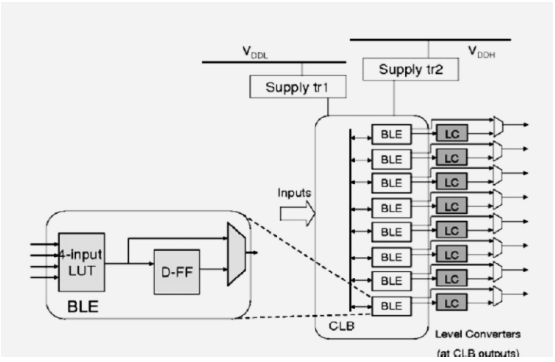

Fig.12 Dual VDD architecture[16]

4.2.3. Clustered Voltage Scaling (CVS)

Siva kumar et al discussed that this technique power can be optimised without compromising circuit performance by making use of two supply voltages. Gates in the critical path are run at the lower supply, as shown in Fig. 9. To minimize the number of interfacing level converters needed, the circuits which operate at reduced voltages are clustered leading to clustered scaling. Here only one voltage transition is allowed along a path and level conversion takes place only at flip-flops.

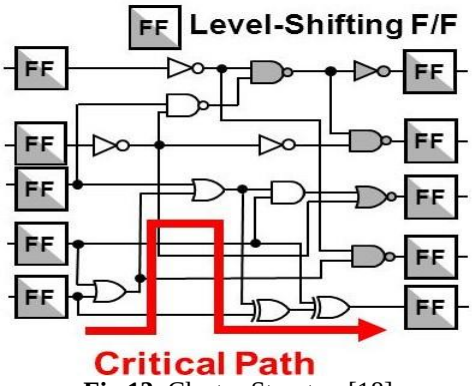

Fig.13. Cluster Structure[18]

4.2.4. Dynamic Voltage and Frequency Scaling (DVFS)

Siva Kumar et al discussed that many circuits have time varying performance requirements in such cases the power can be saved by reducing the clock frequency to a sufficient level to complete the task on schedule then reducing the voltage to that level. This is called dynamic voltage frequency scaling (DVFS). Fig.15 shows DVFS technique to save power. This technique can be implemented by proper controlling program.

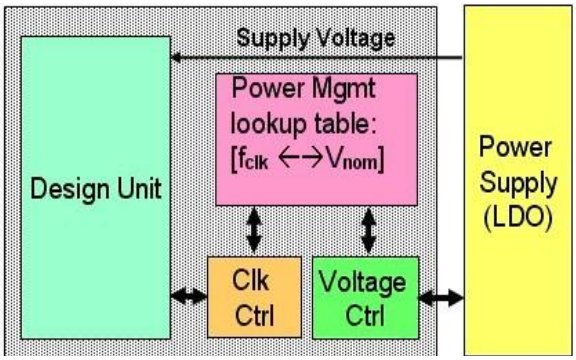

Fig.14 DVFS technique [18]

4.2.5. Adaptive Voltage Scaling (AVS)

This is an extension of DVFS where the control loop is used to adjust voltage and frequency for changing work load. The AVS loop regulates processor performance by automatically adjusting the output voltage of the power supply to compensate for process and temperature variation in the processor. When compared to open loop voltage scaling solutions like Dynamic Voltage Scaling (DVS), AVS uses up to 45% less energy as shown in Fig10. AVS is a system level scheme that has components in both the processor and power supply.

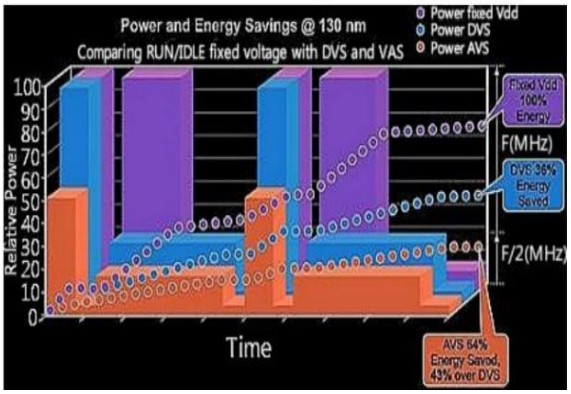

Fig.15 Comparisons of fixed voltage, DVS and AVS energy saving in a processor.

V. ADVANCED POWER OPTIMIZATION TECHNIQUES

Adiabatic Switching

Bhuvana et al discussed that an adiabatic switching is an alternative solution to reduce power dissipation in the digital logic shown in the Fig.12. Adiabatic offers reuse of energy stored in the load capacitor, rather than discharging the load capacitor to the ground and wasting this energy. Operations of adiabatic logic circuits are based on some basic rules such as never turn on a transistor when there is a voltage potential between the source and drain terminals, and never suddenly change the voltage across any of the transistor. The adiabatic logic is widely known as ENERGY RECOVERY CMOS logic as it uses reversible logic to conserve energy.

The energy stored in the output gets retrieved by reversing the current source direction.

Here, the constant current source is used to charge the load capacitance not a constant voltage source as used in the case of conventional CMOS circuits. Where, R represents the on resistance of PMOS network.

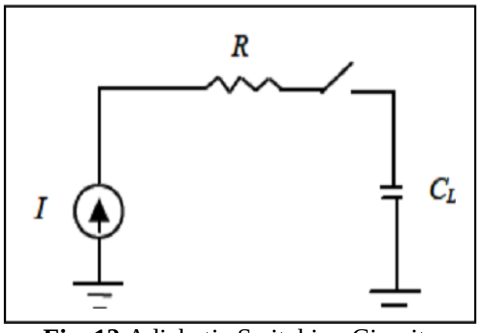

Fig. 12 Adiabatic Switching Circuit.

The constant current power supply is capable of retrieving the energy back from the circuit. Thus, adiabatic logic circuits require non-standard power supplies with time varying voltages such as pulsed power supplies. To meet today's power requirement, most research has focused on building adiabatic logic, which is a promising design for low power applications at present.

Classification of Adiabatic logic families

Adiabatic logic is broadly classified into two categories. They are partially adiabatic logic and fully adiabatic logic.

I. Partially Adiabatic logic

In partially adiabatic or Quasi adiabatic circuits, some charge gets transferred to the ground i.e. some heat is dissipated. Hence a part of the energy is only 4255being able to recover, but these circuits are easy to implement as compared to fully adiabatic logic circuits.

Some partially adiabatic logic families are: -

1. Efficient Charge Recovery Logic (ECRL)
2. 2N-2N2P Adiabatic Logic
3. Positive Feedback Adiabatic Logic (PFAL)
4. Clocked Adiabatic Logic

II. Fully Adiabatic

In fully adiabatic circuits, all the charges on the load capacitance gets recovered and feedback to the power supply. Due to which fully adiabatic circuits become slower and complex as compared to partial adiabatic circuits.

Some fully adiabatic logic families are: -

1. Pass Transistor Adiabatic Logic (PAL)
2. Two Phase Adiabatic Static CMOS Logic (2PASCAL)
3. Split-Rail Charge Recovery Logic (SCRL).

Yet some complexities in adiabatic logic design perpetuate. Two such complexities, for instance, are circuit implementation for time-varying power sources needs to be done and computational implementation by low overhead circuit structures needs to be followed.

There are two big challenges of energy recovering circuits; first, slowness in terms of today's standards, second it requires ~50% of more area than conventional CMOS, and simple circuit designs get complicated.

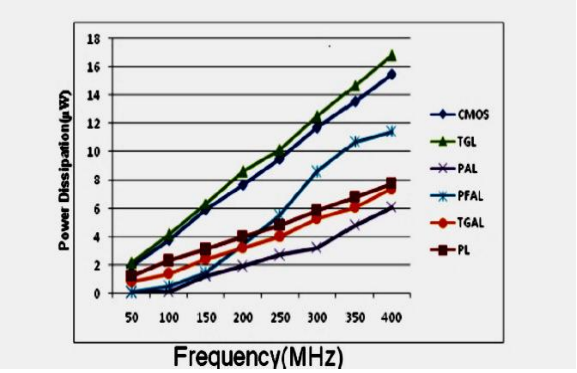

Fig.13 Variation of power dissipation with frequency for different fulladder circuits using different adiabatic logic [21]

Fig .13 shows the comparision of performance of different adiabatic logic adder circuits with traditional CMOS adder circuits for different full adder circuits. Y.sunil gavaskar reddy et al implemented and their analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits. So for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design.

VI. CONCLUSION

In this paper we presented various power optimization techniques almost in all levels of design. It can be concluded that the important performance parameters such as dynamic power, leakage power, propagation delay and the PDP are strongly inter related.

Table.1 Advantages and Disadvantages of Power Optimization Techniques

Technique	Advantages	Disadvantages
MTCMOS	Power efficient with no effect on speed	More area
Transistor Stacking	Easy to implement, leakage saving, easy to Fabricate	Propagation delay increases
Sleepy stack	Single threshold transistors, less delay compared to transistor stacking	Needs to control circuits, area increases, less power savings
LECTOR	Control circuit is not required. Best power savings in both the modes of operation	Delay increases
Body bias	More power savings	Complexity in implementation
Clock gating	Medium power savings, less effect on speed	Complexity in implementation
Dual V_{dd}	Medium power savings	Effects on speed, control circuitry is required
DVFS	More power savings	Complexity in implementation
Adaptive voltage scaling	Efficient in power savings, Improves performance compared to DVFS.	Effects in speed
Adiabatic	More power savings	More area

Optimization of one parameter needs trade-off of other 3 parameters. To meet today's power requirement, most research has focused on building adiabatic logic, which is a promising design for low power applications. We can say here that adiabatic approach is advanced technique for power reduction and it is giving better results than conventional methods. Domino logic is mainly applied to have high speed operation. For this also there are many reduction techniques and observed than power can be save for this logic also. Finally, we can conclude that this study provides an appropriate choice for power optimization techniques technique for a specific application by a VLSI circuit designer.

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