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RESEARCH ARTICLE OPEN ACCESS

Design of Multilayer Fractal Capacitor in 0.18µm RF CMOS process

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ABSTRACT: In this Paper, Multilayer capacitor is proposed based on chord fractal space filling curvein0.18µm RF CMOS process. The Proposed capacitor uses the both vertical and lateral electric fields. The capacitance density increases as number of layers increases with proper contact of vias in CMOS process. The design strategy is proposed for an on-chip area of 100 × 100 µm^2. The Proposed capacitor achieves a 50 % higher capacitance value than the standard chord capacitors of similar on-chip area with a reasonable Q factor and Self resonant frequency for RF applications.
Keywords*: Fractal Geometry, Chord Pattern, Lateral flux, Vertical flux*

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I. INTRODUCTION

Capacitor is an important passive component in wireless RF applications. Capacitors are often used in Filters [1], RF oscillators [2] and so on. Especially, the design of on-chip capacitor is a Challenging as it needs to keep compatible size with the active components on ICs.

Several varieties of capacitors are proposed over the years. High capacitive capacitors like Gate oxide [3] and Junction capacitors [4] are highly nonlinear. The Lateral flux contribution is popular with rapid change in technology scaling. Inter digital Capacitors (IDC) [5] are exploit the lateral flux capacitance and these capacitors are passive and highly linear. But have a low capacitance density due to inheritance inductance.

The introduction of fractal patterns in wireless components design brings the tremendous change in size [6-7]. The advantage of fractals in capacitor is to increase the capacitance density [8]. The capacitance increased in [8] using traditional fractal patterns. The estimation of capacitance is a challenge task for these types of capacitors. After several capacitors are proposed using MEMS [9] and fractal spiral capacitor with improved Q factor and self-resonant frequency values [10]. Recently, an efficient chord fractal is proposed [11], which effectively se the silicon on chip area compared fractal capacitors.

In this paper, Multilayer capacitor is proposed using 3rd iterative chord fractal reported in [11] as higher order fractal iterations are complex and provides lesser density at the edges of capacitor. The Proposed design exploits both lateral flux as well as vertical flux to maximize the capacitance density in a specified silicon area. To obtain maximum vertical flux number of layers is increased with straight connecting vias between the layers

The rest of the paper is organized as follows. Section II describes the flux capacitors; section III describes the chord fractal design in single and multilayer process. Section IV associated with simulation results and comparative analysis with standard fractal capacitor structures. Finally Conclusions are drawn in section V.

II. FLUX Capacitors

Lateral flux capacitors are built on single metal layer. Whereas vertical capacitors are built on different layers. The rapid changes VLSI technology gives more significance towards lateral flux than the vertical flux. In this paper the capacitance is improved by considering the both vertical as well as lateral fluxes. Figure .1 shows the combination of vertical and horizontal fluxes.

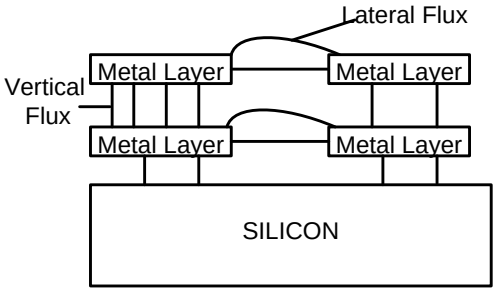

Fig.1: Lateral and Vertical flux capacitance

III. SECTION

a) Fractal Capacitor Design

Chord fractal [11] proven to effective capacitor in terms of area for RF CMOS technology. In this various types of initiators are used to construct the chord fractal. Fig.2 shows the Chord fractal after third iterations. The Chord fractal is having two plates separated by air as dielectric.

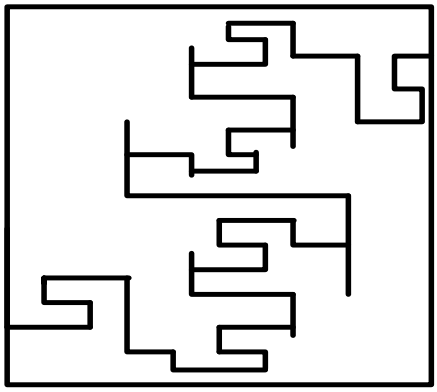

Fig.2 3rd Iteration chord fractal [11]

The Chord fractal capacitor in single metal layer with different initiators considered is shown in Fig 3. The Capacitor is designed on top metal layer M6. Metal layer is made of Copper with a relative permittivity of with a transparent passivation layer above the M6 metal layer. Two Capacitor plates are represented in different colors. The maximum outer edge of plate is considered as 100 µm with a dielectric separation of 2 µm. The thickness of outer capacitor plate is considered 2um.

b) Multilayer Capacitor Design

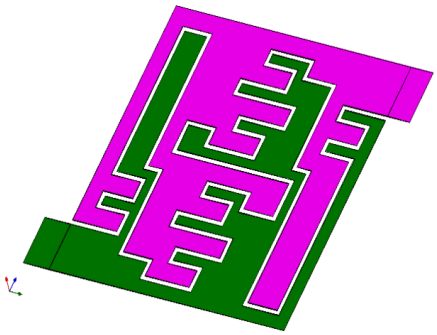

Fig.3: Single layer Fractal capacitor

180 nm RF Metal stacks for CMOS process is used for the design of Capacitor. Two layer capacitor is designed by utilizing the top two metal layers M6 and M5 and it can be extend to four layer capacitor. By proper joining of capacitor plates using vertical vias improves the capacitance density. The Proposed capacitor is as shown in Fig.4

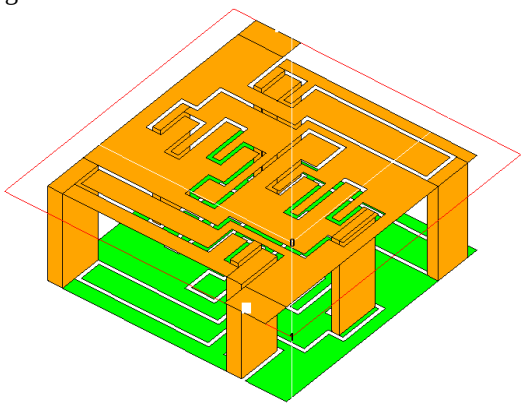

Fig.4: Multilayer Chord Capacitor Structure

The connection used is similar to the parallel combination of capacitor, where the capacitance almost double. Analysis of the designed capacitor is done next in the following section.

Section IV: Results and Discussion

The proposed Multilayer chord fractal capacitor and single layer chord fractal is designed using a HFSS software. In the simulator, the substrate and dielectric layers are considered as per the technology parameters to synchronize with capacitor fabrication process.

The capacitance of a proposed capacitor and standard chord fractal capacitor is calculated using Y-parameters and is given by

$$C = -\frac{Im(Y_{21})}{2\pi f} \quad (1)$$

And the Quality factor is given by

$$Q = \frac{Im(Y_{11})}{Re(Y_{11})} \quad (2)$$

Besides the Q, the Self Resonant Frequency is an important factor for the on chip capacitors**.**

The impedance of capacitor becomes inductive if the operational frequency exceeds the Self Resonant Frequency. The Self Resonant Frequency is given as

$$SRF = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

Fig.5 shows the simulated capacitance (C) Characteristics of proposed capacitor and chord fractal in single layer.

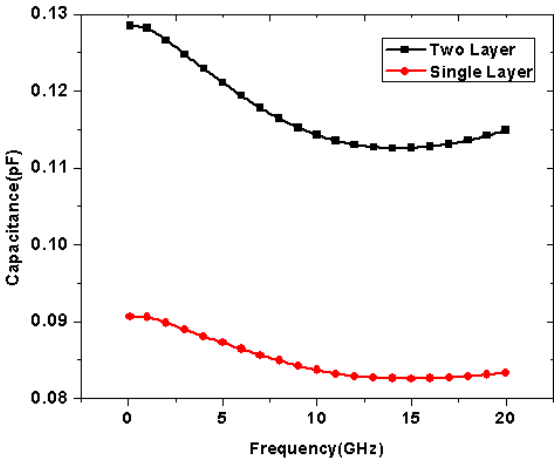

Fig.5: Simulated capacitance values for comparison

It is observed that the proposed capacitor is having a capacitance of 0.125pF at 2.4 GHz which is almost 50% higher than the single layer chord fractal capacitor with a negligible degradation in Q factor which is shown in Fig. 6.

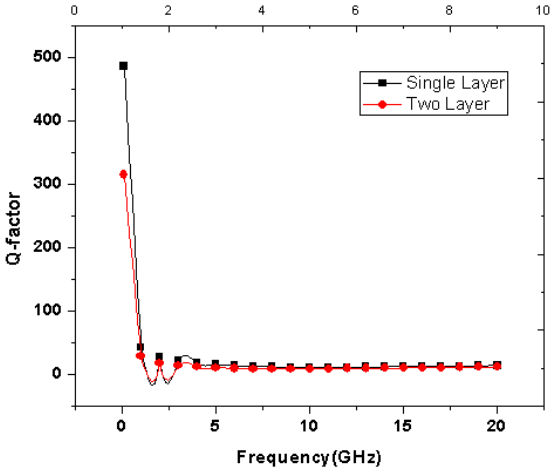

Fig.6: Simulated Q-factor values for comparison

From the fig.6, it is almost both the capacitors are having Q factor value of 50.

It is also observe from the two figureFig.5 and Fig.6. It is having a capacitance 0.12pF slight variation over the frequency range of 1GHz to 20 GHz. The improved in proposed capacitor with standard capacitor is due to parallel combination of

Two metal layers and are connected using Vias. The Q factor is maintain almost same is due to top metal layers are chosen for connection. If further increasing in parallel connection of metal layers increases the capacitance but the Q-factor values drastically reduced as metal layers are nearer to the silicon substrate.

IV. CONCLUSION

In this paper, a new multilayer fractal chord capacitor is designed. The performance between proposed inductor and standard chord fractal in single layer has been simulated and compared using HFSS. The results shows that there is a 50% improvement in capacitance is observed which is suitable for Standard RF applications

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