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RESEARCH ARTICLE OPEN ACCESS

A Comparative Analysis of SRAM Cells in 45nm, 65nm, 90nm Technology

Pinki Narah[1], Mrs. Sharmila Nath[2]
[1](*Department Of Electronics And Communication Engineering, Girijananda Institute Of Management And Technology, Guwahati, India*
[2] *(Department Of Electronics And Communication Engineering, Girijananda Institute Of Management And Technology, Guwahati, India*
Corresponding Author: Pinki Narah

ABSTRACT
Growth In The Semiconductor Industries Has Brought Greater Demand For Low Power Consumption Design For Integrated Circuits (IC). Static Random Access Memory (SRAM) Has Become One Of The Major Components Due To Their Large Storage Density And Low Power Consumption. This Paper Implements Different SRAM Topologies Such As 6T, 7T, 8T And 9T In Three Different Technologies And Its Main Objective Is To Evaluate Its Performance On The Basis Of Static Power Dissipation, Delay, Leakage Current And Static Noise Margin (SNM). This Would Help The Designers To Determine Which Topology To Use In Different Applications.
Keywords – SRAM, CMOS, Power Consumption, Static Power Dissipation, Static Noise Margin.

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I. INTRODUCTION

CMOS Circuits Have Inherent Advantages Of Low Power And Large Noise Margin. Therefore There Has Been A Great Demand For Memories Processing Not Only In Low Power And High Density But Also High Speed.[1].

SRAM Makes Up A Large Portion Of A System-On-Chip Area And Most Of The Time It Also Dominates The Overall Performance Of The System.[2]. In Addition To This The Tremendous Growth Of Popularity Of Mobile Devices And Other Emerging Applications Such As Wireless Body Sensing Network Necessitates The Requirement Of Low Power SRAM.

SRAM Uses Bi-Stable Latching Circuitry Made Of MOSFET To Store Each Bit [3]. Advances In Chip Design Using CMOS Technology Have Made Possible The Design Of Chips For Higher Integration, Faster Performance And Low Power Consumption To Achieve These Objectives The Feature Size Of The Devices Has Been Dramatically Scaled Down To Smaller Dimensions. However As Technology Scaled Down Standby Power Consumption Was Increased Exponentially With The Decrease Of Threshold Voltage Of MOSFET Devices. This Challenge Of Optimizing Power Consumption Gives Us The Very Need To Design Low Power SRAM.

The Goal Of This Paper Is To Determine The Effect Of Different Scaled Down Technologies On Four Different SRAM Topologies And The Performance Is Analyzed Considering The Parameters Such As Static Power Dissipation, Leakage Current, Delay, SNM.

II. CIRCUIT DESIGN AND ANALYSIS

2.1 Conventional Six Transistor (6T) SRAM

6T SRAM Cell Is Made Up Of Two Cross Coupled Inverters And Two NMOS Transistors As The Access Transistors.[4] These Access Transistors Are Connected Between The Bit Lines And The Cross Coupled Inverters. The Access Transistors Are Controlled By The Word Line (WL) And Two Bit Lines (BL And BLB). The Word Line Performs The Operation Of Read, Write And Hold And The Bit Lines Act As Input/Output.

For Write Operation The Ratio Between The Access Transistors To The Pull Up Transistors Must Be Large. The Bit Lines BL And BLB Are Applied With Complementary Voltage Levels And The Word Line Is Selected. The Input Is Given To The Bit Line (BL). The Access Transistors Are Accessed Through The Word Line (WL) And The Data Given Is Written In The Cell.

During Read Operation The Ratio Between The Pull Down Transistors And The Access Transistors Must Be Large. The BL And BLB Are Precharged To V_{dd} And The WL Is Pulsed To Low Level And The Data That Was Previously Written To The Cell Can Now Be Read.

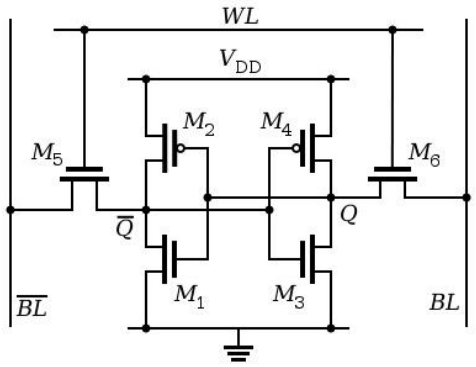

Figure 1: Conventional 6T SRAM

2.2 Seven Transistor (7T) SRAM

The Structure Of 7T SRAM Consists Of Seven Transistors With The Basic Structure Of The Cell Similar To The Conventional 6T SRAM. The Read Bit Line (RBL) Is Used For Reading Data From The Cell.

To Start The Write Operation, The Write Signal W Is Pulsed To V_{dd} And The Input Is Applied To WL While The Read Signal R Is Maintained At Ground Level. The Access Transistors Are Accessed Through The Write-Line (W) And The Data Is Written Into The Cell.

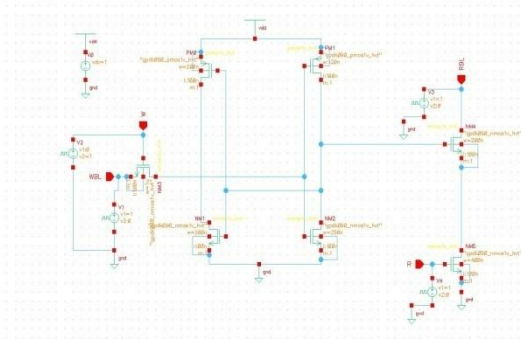

Figure 2: Seven Transistor (7T) SRAM

For The Read Operation, The RBL Is Precharged To V_{dd}. The Written Data Can Be Read Form The Cell By Precharging Both RBL And Read Line (R) To High Level And Maintaining Write Line To Zero Level. The Storage Nodes Are Completely Isolated From The Bit Line During The Read Operation.

2.3 Eight Transistor (8T) SRAM

The Left Sub-Circuit Of 8T SRAM Cell Is A Conventional 6T Memory Cell. The Write Operation Is Similar To Conventional 6T Cell. The Transistor Stack And Read Bit Line RBL Is Used For Reading The Stored Data From The Cell.

To Start The Write Operation The Input Is Given To The Write Bit Line1 (WBL1) And The Compliment Is Given To Write Bit-Line2 (WBL2). The Access Transistors Are Accessed Through Word Line (W) As This Is Pulsed To High Level. The Data Given To The Cell Is Written And The Write Process Is Complete.

For The Read Operation To Begin The Read Line Is Precharged To V_{dd} And The Read Transistor Is Turned On. To Read The Data From The Cell The Read Bit Line (RBL) Is Also Made High And The Write (W) Is Pulsed To Ground And The Read Process Is Complete.

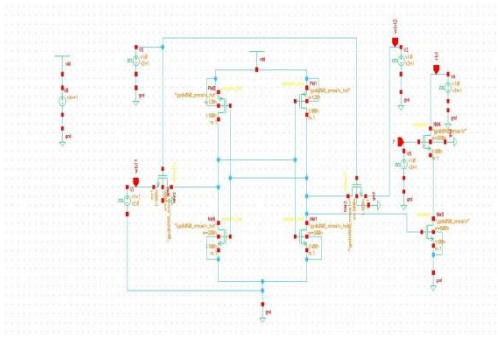

Figure 3 : Eight Transistor (8T) SRAM

2.4 Nine Transistor (9T) SRAM

The 9T SRAM Has The Upper Circuit Similar To 6T SRAM With Minimum Sized Transistors. The Two Access Transistors Are Controlled By The Write Line (W) And The Data Is Stored Within This Sub- Circuit. The Lower Sub-Circuit Consists Of One Read Access Transistor And Is Controlled By A Separate Read Signal (R).

To Begin The Write Operation, The W Signal Is Maintained At High And The Read Is Maintained At Low Which Makes The Read Access Transistor To Cut Off. The Inputs Are Given To The Bit Lines And The Access Transistors Are Accessed Through The Write Line (W) And The Write Operation Takes Place.

For The Read Operation The (W) Is Made Low And Read Line (R) Is Precharged To High Level. This Activates The Read Access Transistors In The Lower Sub-Circuit. The Bit Lines BL And BLB Are Pulsed To High Level And The Written Data Can Be Read From The Cell.

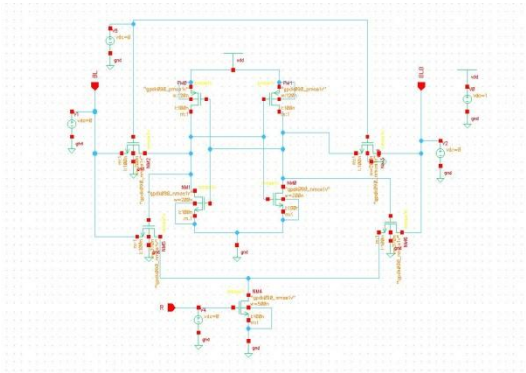

Figure 4: Nine Transistor (9T) SRAM

III. OBSERVATION

Table 1: 6T SRAM Operation

Hold Operation	WL Low, Inverter Reinforces The Data In Feedback
Read Operation	B And BL Is Precharged High, WL Is Assigned
Write Operation	B And BL Are Applied With Complementary Inputs. WL Is Accessed.

Table 2: 7T SRAM Operation

Hold Operation	WL Low, Inverter Reinforces The Data In Feedback
Read Operation	W And WL Is Low, R And RBL High
Write Operation	W And WBL High, Input Applied To WBL, R And RBL Made Low

Table 3: 8T SRAM Operation

Hold Operation	W Low, Inverter Reinforces The Data In Feedback
Read Operation	WL1 And WL2 Is Low, R And RBL High, W Assigned.
Write Operation	WL1 And WL2 Applied With Complementary Inputs , R And RBL Made Low

Table 4:9T SRAM Operation

Hold Operation	W Low, Inverter Reinforces The Data In Feedback
Read Operation	R Is High, BL And BLB Precharged To High
Write Operation	BL And BLB Applied With Inputs,R Made Low

IV. SIMULATION AND RESULTS

3.1 Transient Responses

The Below Figures 5(A),5(B),5(C),5(D) Shows The Transient Response Of Four SRAM Topologies In 45nm Technology.

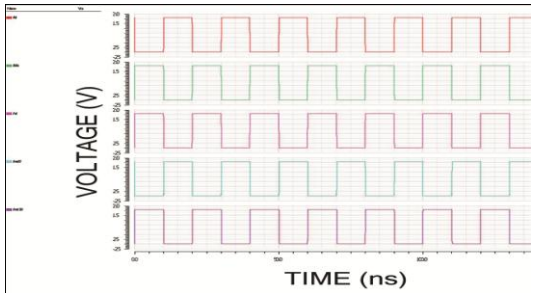

Figure 5(A): Transient Response Of 6T SRAM I 45nm

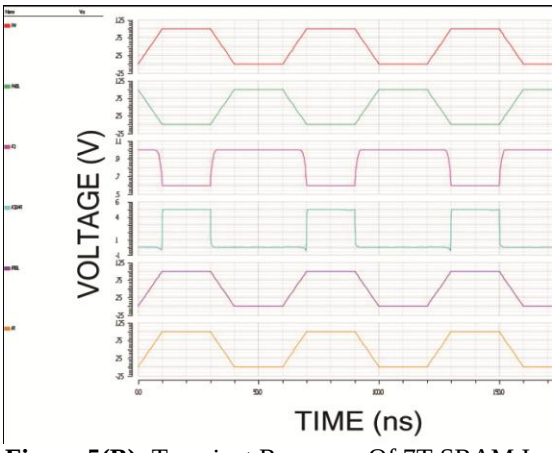

Figure 5(B): Transient Response Of 7T SRAM In 45nm

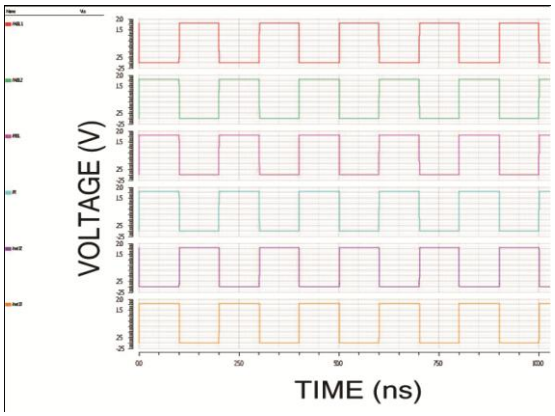

Figure 5(C): Transient Response Of 8T SRAM In 45nm

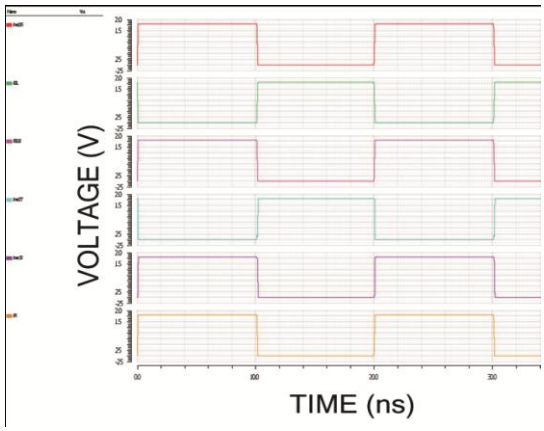

Figure 5(D): Transient Response Of 9T SRAM In 45nm

The Below Figure 6(A),6(B),6(C),6(D) Shows The Transient Response Of The Srams In 65nm Technology.

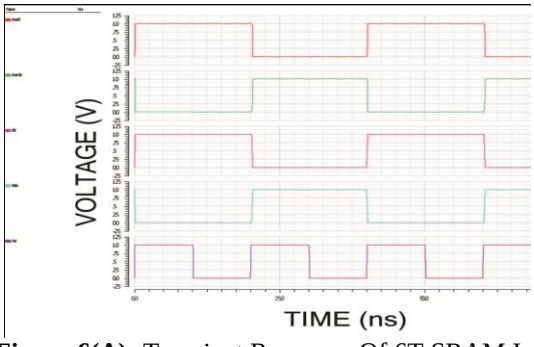

Figure 6(A): Transient Response Of 6T SRAM In 65nm

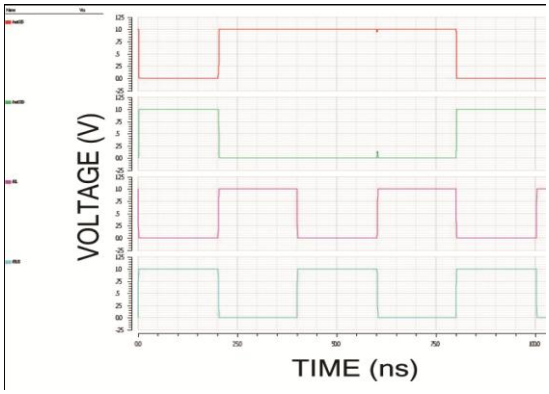

Figure 6(B): Transient Response Of 7T SRAM In 65nm

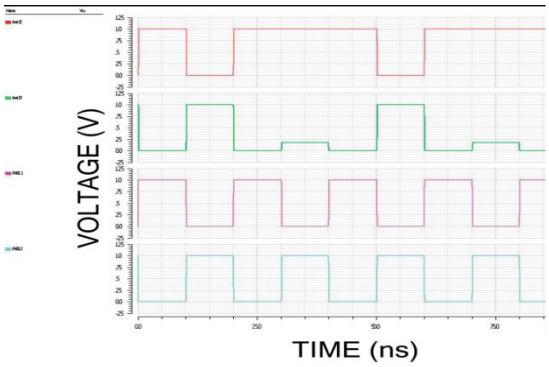

Figure 6(C): Transient Response Of 8T SRAM In 65nm

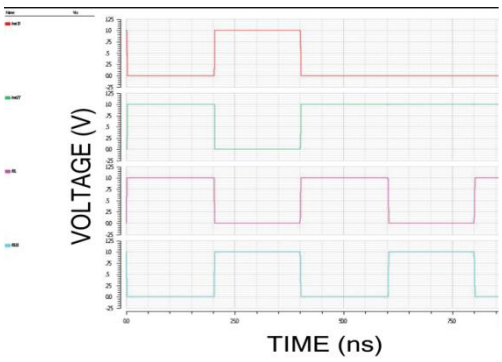

Figure 6(D): Transient Response Of 9T SRAM In 65nm

The Below Figure 7(A), 7(B) 7(C) ,7(D) Shows The Transient Response In 90nm.

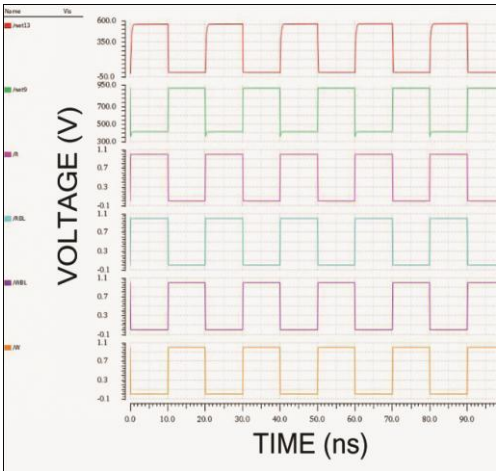

Figure 7(A): Transient Response Of 6T SRAM In 90nm

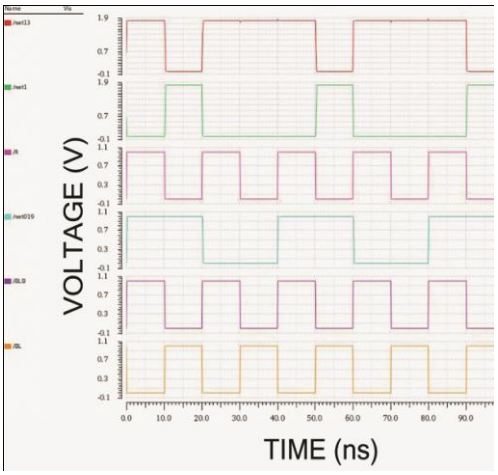

Figure 7(B): Transient Response Of 7T SRAM In 90nm

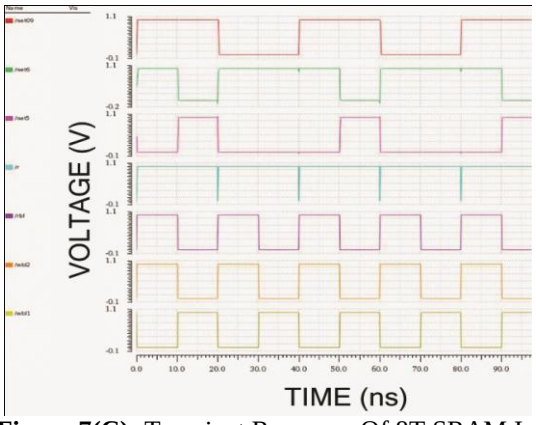

Figure 7(C): Transient Response Of 8T SRAM In 90nm

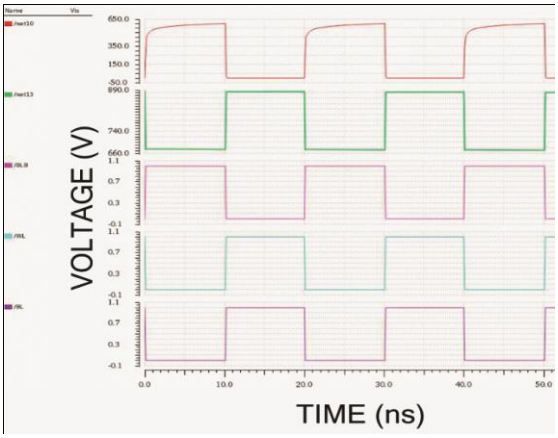

Figure 7(D): Transient Response Of 9T SRAM In 90nm

3.2 Static Power Dissipation

The Table Given Below Shows The Comparison Between The 6T, 7T, 8T And 9T SRAM In Different Technologies Of 4nm,65nm And 90nm. The Comparison Shows That 9T SRAM Has The Greatest Power Dissipation And The Lowest Being The 7T SRAM. The 6T SRAM Has More Power Dissipation In Comparison To 7T SRAM Due To Charging And Discharging Of The Bit Lines.

Table 5: Static Power Dissipation

Technology → / SRAM ↓	45nm	65nm	90nm
6T	1.093uw	1.54uw	2.240uw
7T	7.75nw	14.3nw	15.5nw
8T	1.45uw	1.875uw	2.66uw
9T	1.38uw	1.99uw	2.80uw

3.3 Static Noise Margin

The Stability Of Memory Cell Is Determined In Terms Of SNM Or Static Noise Margin. SNM Can Be Defined As The Maximum Noise Voltage That An SRAM Can Withstand Without Changing Its Node Data. SNM Is Determined By The Butterfly Curve Which Is The VTC Of One Inverter Superimposed On The VTC Of Another Inverter. From The Comparison It Can Be Said That Stability Is Highest In 9T And Lowest In 6T Due To Voltage Division Between Access And Driver Transistor.

Table 6: Read Static Noise Margin

Technology → / SRAM ↓	45nm (Mv)	65nm (Mv)	90nm (Mv)
6T	72.8	98.5	105
7T	79	107.87	185
8T	79.59	202.3	502
9T	497	531	540

Table 7: Write Static Noise Margin

Technology → / SRAM ↓	45nm	65nm	90nm
6T	274	300.6	396
7T	325	370.67	409
8T	485	509.6	532
9T	640.23	650	686

3.4 Delay

Write Delay Is Considered As The Time Difference Between The Applications Of The Word Line Signal And The Time At Which The Data Is Actually Written Into The Cell. As The Transistor Count Increases Delay Increases With An Exception That Delay Is Less In 7T SRAM Due To The Arrangement Of Transistors.

Table 8: Delay

Technology → / SRAM ↓	45nm(Ps)	65nm(Ps)	90nm(Ps)
6T	73.37	75.19	79.87
7T	62.8	65.7	71.32
8T	137.7	138.8	146.2
9T	147.3	150.2	157.2

3.5 Leakage Current

The Comparison Shows That Leakage Increases As The Technology Increases. Leakage Current Contributes To Major Part Of Power Consumption In SRAM In Sub Micron Regime. Leakage Current Is Highest In 9T SRAM.

Table 9: Leakage Current

Technology → / SRAM ↓	45nm	65nm	90nm
6T	1.093ua	1.54ua	2.240ua
7T	7.75na	14.3na	15.5na
8T	1.45na	1.875ua	2.66ua
9T	1.48ua	1.99ua	2.80ua

V. CONCLUSION

The Operation Of SRAM Is Studied In Details In Cell Level. This Has Provided A Thorough Understanding Of The Working Of SRAM. In This Paper Parameters Like Delay, Static Power Dissipation, Static Noise Margin And Leakage Current Of Various SRAM Cell Such As 6T, 7T, 8T,9T Are Compared In Different Technologies To Check Its Variation. All The Simulation And Calculations Are Done Using

CADENCE Tool. It Has Also Helped In Providing A Great Exposure To The Tool. It Is Observed That 7T SRAM Is Proved To Be The Best Among Other Cell In The Matter Of Leakage Current Or Delay Being The Least In Each Case. It Can Also Be Concluded That 9T SRAM Has Greater Stability Than Conventional 6T SRAM.

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