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RESEARCH ARTICLE OPEN

High Performance Weighted Random BIST

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ABSTRACT
A New Low-Transition (LT) Built-In Self-Test (BIST) Technique Is Proposed Based On Weighted Pseudo-Random Test Pattern Generation Tested In Circuit Under Test (CUT). A New BIST Method Has Been Proposed Using Weighted Random Test Pattern Generation. The New Method Consists Of Two Separate Phases: 1) Low Transition Pattern Generation And 2) Weighted Random Test Pattern Generation Using Weights Pattern. This Proposed Circuit Achieve High Speed And Low Area And Delay. The Experimental Shows Good Result Using XILINX XC3S100E-5TQ144 Spartan FPGA Device.
Keywords - Built-In-Self-Test, Model Sim, Weighted Pseudo-Random Testing, Xilinx Software

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I. INTRODUCTION

The important challenging field in VLSI is speed, cost, testing, area, reliability and power. The demand for viable computing devices and system of communication are increasing tremendously. These applications require low power dissipation. The main aim of these devices is to improve speed and performance with high fault coverage. Testing of integrated circuits is important to ensure high level of quantity products. The most popular testing method for embedded core is done using Built-In-Self-Test (BIST). Test pattern generation is vital in any BIST circuit. Off-chip communication between the Field Programmable Gate Array and a processor is bound to be slower than on chip communication and in order to reduce the time required for adjustment of the few parameters, the built in self-test approach is proposed for this method.

II. EXISTING SYSTEM

In the Existing system, Power is considered as one the parameter for improving the performance of the system. By making the phase shifter as common for all select chains, the size of the phase shifter is reduced. Thus by implementing the system, one of the parameter such as power is reduced

III. PROPOSED SYSTEM

In the Proposed system, the random input are obtained from the pseudo-Exhaustive Random Test Pattern Generator (RTPG), it is one of the test pattern It detects all detectable faults that do not cause sequential behaviour. By implementing this method the speed of the system is increased and the delay is reduced gradually. Where by using weighted BIST it detects faults and delay while testing

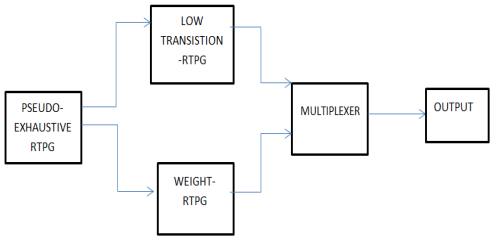

Fig.1.1 Block Diagram Of Proposed Module

Fig.1.1 represents the proposed module of the design. Here in this module it consists of four sections, namely Pseudo-Exhaustive Random Test Pattern Generator, Low Transition Random Test Pattern Generator, Weight Random Test Pattern Generator and Multiplexer. Pseudo-Exhaustive Random Test Pattern Generator is one of the types of test pattern generation. It is applied for all 2^n input vectors. It detects all detectable faults that do not cause sequential behavior. Exhaustive Testing use a counter or a LFSR for pattern generation. Low-Transition random TPG (LT-RTPG) is comprised of an Linear Feedback Shift Register, a N-input AND gate, and a Flip-flop. When used to generate test pattern for test-per-scan BIST, where it decreases the number of transition that produced during scan shifting and hence it increases the speed during testing. Test pattern generator (TPG) is one of the methods for scan-based built in self- test (BIST) that can decrease switching activity of the circuits under test (CUTs) during Built in Self-Test and also produce very high fault coverage with desire lengths

of test sequences. The Proposed BIST is comprised of two TPGs:

1) LT-RTPG

weight WRBIST. A Multiplexer is a device that selects one several digital input signals and forwards the selected input into single line. Multiplexer in proposed method is mainly used to increase the amount of data.

IV. TECHNOLOGIES USED

4.1. Xilinx ISE

For synthesis and analysis of HDL designs, a software tool named Xilinx ISE is produced by Xilinx is used. Xilinx enables the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

4.2.Model Sim

Model Sim is a multi-language HDL simulation environment, it increases the quality of design and debug. For simulating Hardware description language it is being used. In behavioral simulation, we can write models that will not necessarily synthesize. An example is a behavioral model for the ZBT RAMs used on the Xilinx Multimedia board. This code cannot be synthesized, but it is intended to give a true reflection of the behavior of the memory chip so that can test whether memory controller is functioning properly

4.3 Xilinx Spartan-3E Starter Kit

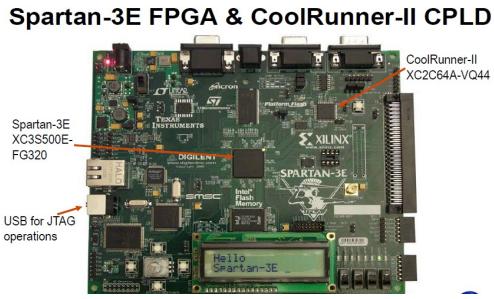

Fig.1.2 Spartan-3E FPGA Kit

Fig.1.2 Shows a full-featured Spartan-3E FPGA kit it includes,

1) Starter Kit Board

2) Power Supply

3) Evaluation Software & Resource CD

4) USB Cable (for programming)

Features of Spartan -3E FPGAs configure from commodity Flash memory which fully supports easy-to-handle Xilinx Platform Flash and consists of -Software Process Improvement serial Flash. Neither where Parallel NOR are flash supports primarily for Micro Blaze embedded applications configured. Improved

2) Weight-RTPG

Test patterns generated by the LT-RTPG detect easy

support for embedded systems applications includes Low-end support for 32-bit Micro Blaze RISC core and Efficient 8-bit Pico Blaze controller core. An advantage of Spartan-3E is Low-cost, space efficient FPGA power solution. Humidity sensor (or hygrometer) senses, measures and reports both moisture and air temperature. It senses the temperature of the mining area and alerts the user if the range exceeds.

V. SIMULATED RESULT

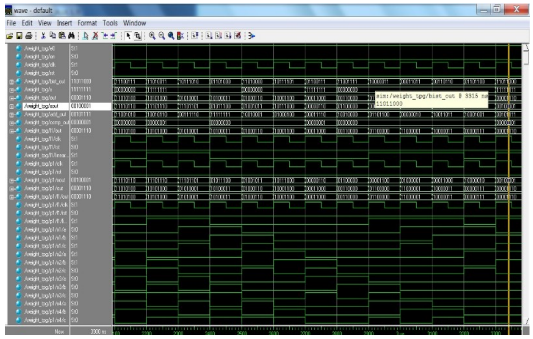

Fig.1.3 Shows The Output Of The Proposed Method.

Fig.1.3 Shows The Output Waveform Of The Proposed Method, And It Shows The Different Comparison Of Various Parameters Such As Area, Speed, And Delay.

VI. SYNTHESIZE RESULT

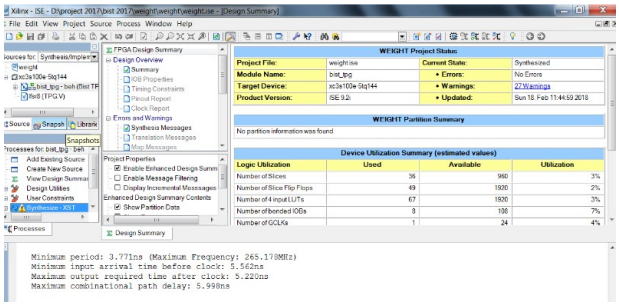

Fig.1.4 Synthesize Result

Fig.1.4 Shows The Utilization Of Maximum Frequency, Output Required Time After Clock, Combinational Path Delay And Minimum Input Arrival Time Before Clock

VII. RESULT ANALYSIS

METHODS	AREA (NO.OF FLIPFLOPS)	DELAY(NS)	SPEED(MHZ)
LOW POWER SCAN	123	3.804	262.916
WEIGHT_TPG	32	6.241	160.229
PROPOSED_WEIGHT_TPG	49	3.771	265.178

Fig.1.5 Result Analysis

Fig.1.5 represents the Area, Delay and Speed of the proposed method. In proposed method Number of Flip-flops and Delay are reduced, while the speed is increased.

VIII. COMPARISION OF EXISTING AND PROPOSED METHOD

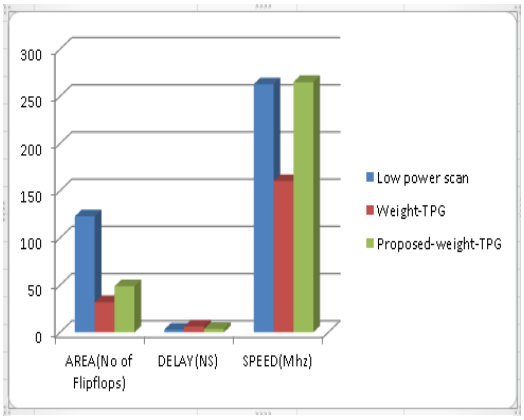

Fig.1.6 Comparisons Chart Of Existing And Proposed Method

As the result shows the comparisons of speed between the existing and proposed method. Fig.1.6 shows that the speed is increased in proposed method while compared to existing method.

IX. CONCLUSION

The new method consists of two separate phases: 1) Low Transition pattern generation and 2) weighted random test pattern generation using weights pattern. In first phase reduce the transitions among patterns. The proposed Circuit achieves high speed and low area and delay. High performance is achieved by increasing the clock frequency. Experimental results have illustrated the performance of the proposed method by comparing with LP BIST method. The experimental shows good result using XILINX XC3S100E-5TQ144 Spartan FPGA Device.

X. FUTURE WORKS

The proposed BIST-TPG can be further extended with suitable block encoding mechanism in which block encoding can be done based on the transitions associated with test patterns or by designing an architecture that can control the toggling levels associated with the BIST schemes. The reduction in hardware overhead can be achieved by employing quantum adders for performing the addition and designing the fixing logic with quantum gates

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