RESEARCH ARTICLE OPEN ACCESS

FPGA Based Decimal Matrix Code for Passive RFID Tag

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ABSTRACT
In this paper, Decimal Matrix Code is developed for RFID passive tag. The proposed DMC uses the decimal algorithm to obtain the maximum error detection and correction capability. The Encoder-Reuse Technique is used to minimize the area overhead of extra circuits without disturbing the complete encoding and decoding processes. ERT uses DMC encoder itself to be part of the decoder. The Simulation results reveals that the Decimal Matrix Code is effective than existing Matrix and Hamming odes in terms of Error Correction Capability. Xilinx ISE 14.7 Software is used for the simulation outputs. The complete design is verified and tested on Spartan-6 FPGA board. The performance of system is measured in terms of power, area and delay. The Synthesis result shows that, the power required for complete design of Decimal Matrix Code is 0.1mW with a delay of 3.109ns.
Keywords: RFID, base band processor, HDL, FPGA, DMC

I. INTRODUCTION

Radio Frequency Identification (RFID) is "An automatic identification technology that uses radio frequency signals to transmit the identity of objects in the form of a unique serial number". This technology does not use line of sight for communication between reader and tag. It is the best choice for automatic identification due to flexibility, easy to use, contactless, multiple tag identification, high data rate, long read range and the lowest cost. RFID application is growing in many fields such as smart table, access control, animal tracking, logistics, supermarkets, airport baggage handling, antifraud systems and medical treatment [1-5]. RFID system consists of reader, tag and antenna. The reader has antenna that send/receive radio frequency signals to/from tags. Tag shares the data with the reader through radio frequency signals. The main component of the tag is digital base band processor which controls the all the functions of the tag. Several Decimal Matrix Code have been presented before namely, Jing Guo,[8] presented a paper on a "Enhanced Memory Reliability Against Multiple Cell Upsets Using Decimal Matrix Code" with reduced power consumption and chip area with a power consumption of about 10.8mW and area 41572.6μm^2. The challenge in designing UHF passive RFID tag is to reduce power consumption because the energy of a passive tag comes from the signal sent by a reader and also it is a power limited device. The operation range of a RFID system depending on the maximum of the dynamic power of the tag. There are static power dissipation and dynamic power dissipation in the VLSI circuit. Dynamic power dissipation includes switching power due to charge and discharge of load capacitance of input signals. Static power dissipation result from the leakage current when the logic gate is static [6]. To reduce power consumption and area in RFID tag, a DMC coding technique is included and there by power dissipation, area and delay of the RFID tag are reduced. In this proposed paper, we have developed a DMC coding technique for UHF RFID tag which includes, encoding and decoding architecture compatible with ISO/IEC 1800-6 tag on Spartan 6 FPGA to observe its functionality. The DMC coding technique is developed by ModelSim is implemented and verified on Spartan-6 FPGA.

This paper is organized as follows: Section 2 defines DMC encoder. Section 3 describes DMC encoder. Section 4 simulation results. Finally section 5 presents the Conclusion.

II. DMC ENCODER

DMC Encoder, which uses decimal algorithm to increase the error detection and correction capability. In this algorithm power consumed will be less compared to other detection methods. This algorithm involves decimal integer subtraction and integer addition. In the decimal algorithm, the divide-symbol and arrange-matrix are performed. Here the N-bit word is divided into n symbols of m bits ($N = n \times m$), and these symbols are arranged in a n= $n1 \times n2$ 2-D matrix (n_1=number of columns and n_2 =number of rows). The horizontal redundant bits H are obtained by performing decimal integer addition on symbols per row. Finally, then vertical redundant bits V are obtained by binary operation on the bits per column. It is noted that both divide-symbol and arrange-matrix are presented in logical instead of in physical.

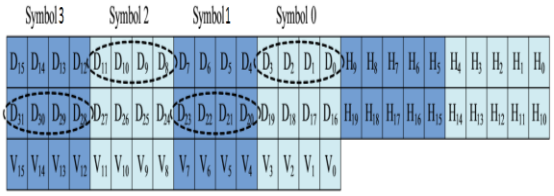

Figure.2.1.1 32-bits DMC logical Organization [8]

To explain the DMC scheme, take a 32-bit word is input, which is shown in Fig.2.1.1. The cells from D_0 to D_{31} are information bits. This 32-bit word has been divided into eight symbols of 4-bits. n_1=2 and n_2=4 have been chosen simultaneously. $H_0 - H_{19}$ are horizontal check bits;V_0 through V_{15} are vertical check bits.

The horizontal redundant bits H can be obtained by decimal integer addition as follows:

$H_4H_3H_2H_1H_0 = D_3D_2D_1D_0 + D_{11}D_{10}D_9D_8$	1
$H_7H_6H_5 = D_7D_6D_5D_4 + D_{15}D_{14}D_{13}D_{12}$	2

Similarly other remaining horizontal redundant bits are obtained where "+"represents decimal integer addition.

For the vertical redundant bits V, we have

$V_0 = D_0 \oplus D_{16}$	3
$V_1 = D_1 \oplus D_{17}$	4

In a similar manner remaining vertical redundant bits are obtained. The encoding can be done by decimal and binary addition operations from (1) to (4). The encoder that computes the redundant bits using multi-bit adders and XOR gates is shown in Fig.2.1.2 In this figure, H19−H0 are horizontal redundant bits, V_{15}−V_0 are vertical redundant bits, and the remaining bits U_{31}−U_0 are the information bits which are directly copied from D_{31} to D_0.

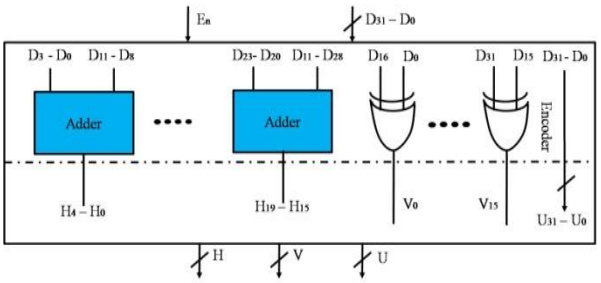

Fig. 2.1.2 32 bit DMC encoder structure using multi bit adders and XOR gate [8]

III. DMC Decoder

For the correction of word obtained, the decoding process is required. At the beginning, the received redundant $H_4H_3H_2H_1H_0'$ and $V_0' - V_3'$ are generated by the received information bits D'. Secondly, the horizontal syndrome bits $H_4H_3H_2H_1H_0$ and the vertical syndrome bits S3 −S0 can be calculated as follows:

$\Delta H_4H_3H_2H_1H_0' = H_4H_3H_2H_1H_0' - H_4H_3H_2H_1H_0$	5
$S3 - S_0 = V_0' \oplus V_0$	6

Similarly for the remaining vertical syndrome bits. Where "–" represents decimal integer subtraction. When $\Delta H_4H_3H_2H_1H_0'$ and $S_3 - S_0$ are equal to zero, the stored codeword has original information bits in symbol 0 are nonzero, then there is an error. Induced errors are detected and located in symbol 0 and these errors can be corrected by

$D_{0Correct} = D_0 \oplus S_0$	7

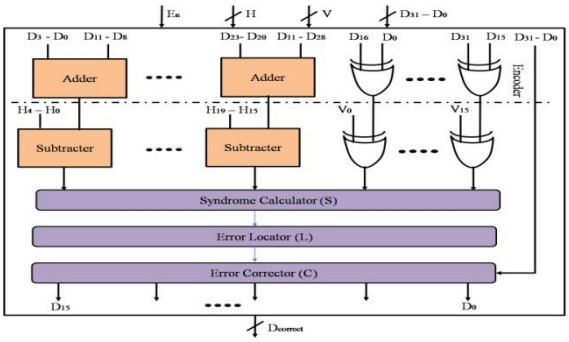

Figure.2.2.1 32-bit DMC decoder [8]

The DMC decoder is used in our design is shown in Fig.2.2.1, which consists of Syndrome calculator, Error locator, and Error corrector. Here, each module performs a particular function in the decoding process. It is noted from Fig. 2.2.1, that the redundant bits re obtained from the received information bits 'D' and compared with the original set of redundant bits in order to obtain the syndrome bits ΔH and S. Then, error locator uses ΔH and S to detect and locate error bits. Finally, the error corrector corrects the error bits by inverting the values of error bits. The 'En' signal is used to decide whether encoder is a part of the decoder.

IV. SIMULATION RESULTS

The proposed design has been done in Verilog HDL. Simulated using model Sim Simulator. For synthesis, we have used the EDA tool Xilinx and all sub module simulation results and top module results are shown in the following sections. Figure.4.1 shows the simulation result and of encoder module. Input is a 32-bit tag ID number and generates 20-bit horizontal and 16-bit vertical redundant numbers as output.

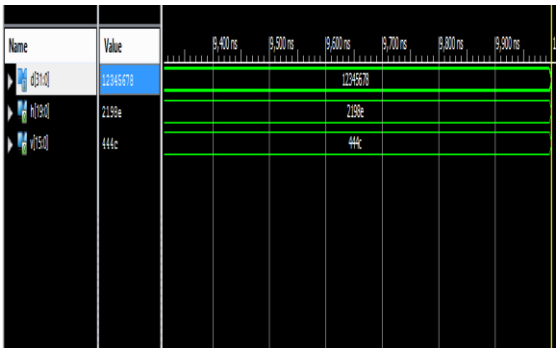

Figure.4.1.Simulation result of encoder

Figure.4.2 shows the simulation result of transmitter module. The 32-bit Tag ID number is input to this module. It generates a output frame of 68-bit length. The frame contains 16-bit vertical redundant number, 20-bit horizontal redundant number and 32-bit input.

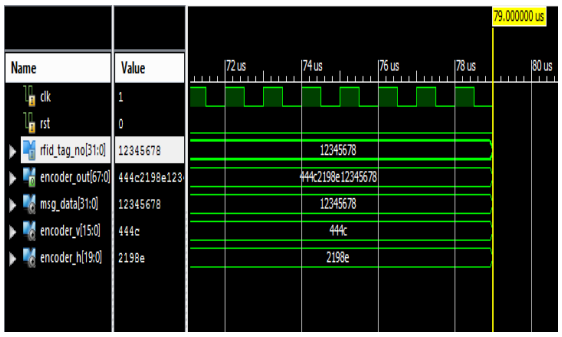

Figure.4.2 Simulation result of transmitter

The Figure.4.3 shows simulation result of encoder in receiver. The received data may be corrupted due to the transmission error. So, the error data is given to this module as an input, then it generates 20-bit horizontal redundant bits and 16-bit vertical redundant bits derived from error data as an output.

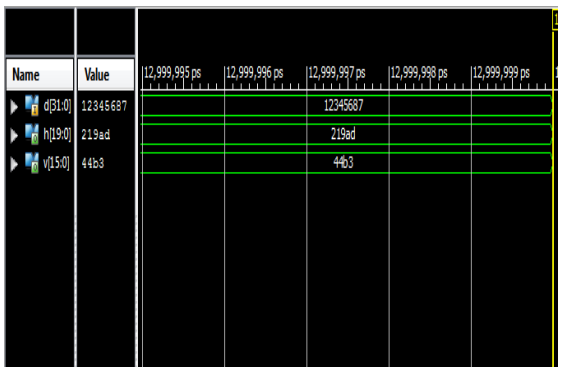

Figure.4.3 Simulation waveform of encoder in receiver

Figure. 4.4 shows the simulation result of CRC module, to check whether the received data bits are correct or not. It calculates the vertical syndrome bits by XORing the original vertical V [15-0] bits with the vertical bits being derived from received data V_d [15-0].

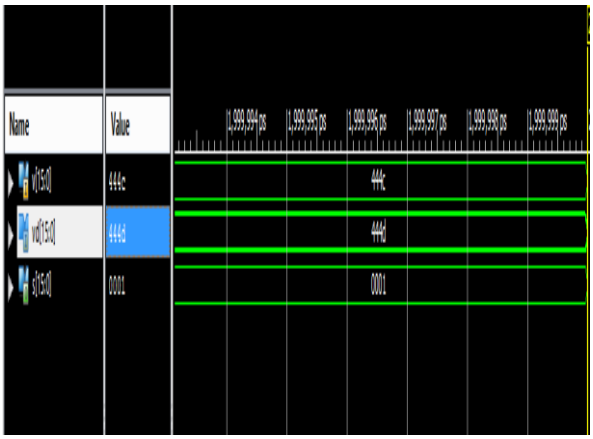

Figure.4.4 Simulation result of CRC for vertical syndrome bits

Figure.4.5 shows the simulation result of CRC module, to calculate horizontal syndrome and whether the received data bits are corrupted or not. It calculates the horizontal syndrome bits by subtracting the original horizontal H [19-0] bits with the horizontal bits which are derived from received data H_d [19-0]. If it is non-zero value the data is corrupted otherwise it is not corrupted.

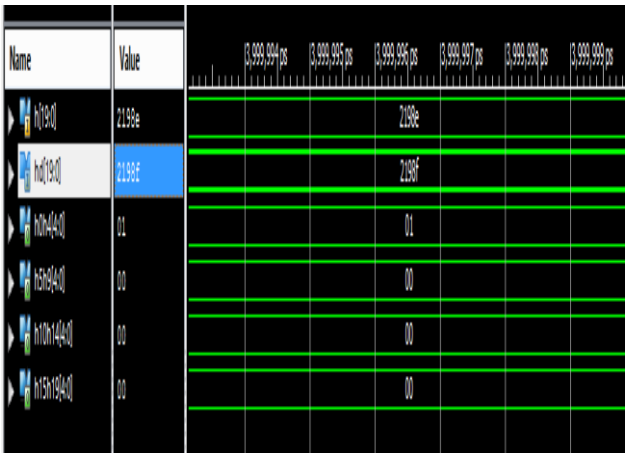

Figure.4.5 Simulation result of CRC for horizontal syndrome bits

The Figure 4.6 shows simulation result of corrector, the 32-bit error data, computed 20-bit horizontal syndrome bits and 16-bit vertical syndrome bits given as an input to the model. It generates a output of corrected 32-bit data.

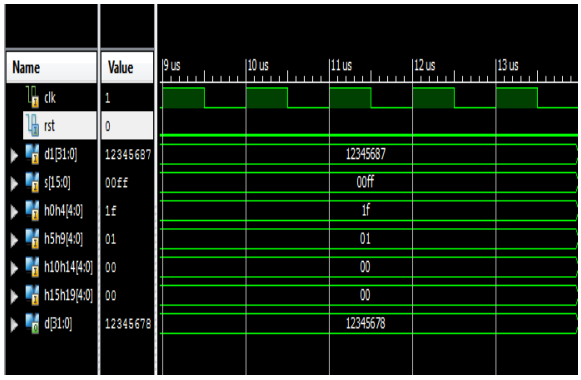

Figure 4.6 Simulation waveform of corrector

Figure.4.7 shows the simulation result of receiver module, the 68-bit frame is input and generates 32-bit decoded data as an output. It performs the data correction if it is required. This module is comprised of CRC and error corrector modules.

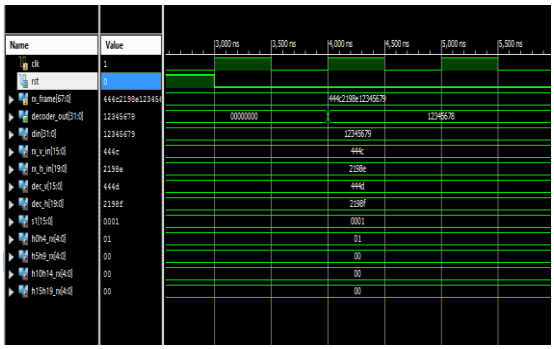

Figure.4.7 Simulation result of receiver

Figure.4.8 It consists of all sub modules such as encoder, decoder, CRC checker, error corrector, frame generator and buffer. It fetches the 32-bit tag ID number stored in ROM memory, performs encoding, frame generating, decoding, error corrections and generates fetched 32-bit tag ID as output.

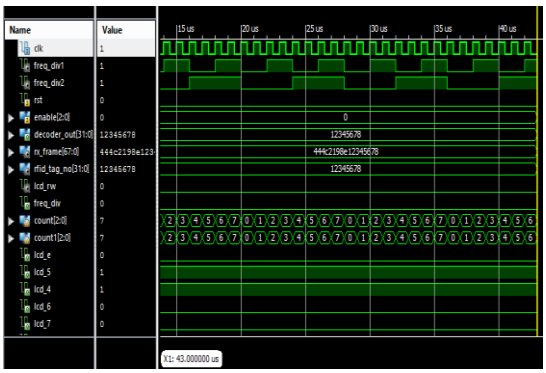

Figure 4.8 Simulation results of Top Module

The table 4.1 shows Area Comparison summary of the DMC Technique. It indicates that DMC Technique performance is better in terms of area when compared with other publications.

Table 4.1 Area Comparison summary of the DMC Technique.

Name	**Ref. No[13]**	**Ref. No[14]**	**This work**
No. of Slices	75	38	15
No. of flip-flops	100	50	15
No. of LUTs	132	68	14
No. of Logic	196	50	13
No .of IOS	72	56	44
No. of bounded IOB	72	40	44
No. of GCLK	1	1	1
Total	584	321	146

Various other parameters such as Delay and Power Summary for DMC Technique are shown in the table 4.2 for various ECC's. This Technique has better performance in terms of power and speed.

Table 4.2 Power and delay comparison summary of the DMC Technique

Type of ECC used	Slices	flip flops	LUTs	Bounded IO	Delay(ns)	Power
This work	174	30	96	44	3.10ns	0.5mW
DMC[40]	NA	NA	NA	NA	4.9ns	10.8mW
PDS* [41]	NA	NA	NA	NA	18.7ns	221.1mW
MC [15]	NA	NA	NA	NA	7.1ns	24.7mW
Matrix Code	164	32	291	96	14.548ns	0.121W
Hamming Code	1350	32	2682	84	17.133ns	0.163W
PIE/FM0 [21]	NA	NA	NA	NA	NA	1.58mW

V. CONCLUSION

In this paper, the Decimal Matrix Code for UHF passive RFID tag has been presented. Encoder re-use technique reduced the area overhead of extra circuits. Simulation and synthesis results reveal that our Decimal Matrix Code can complete its function successfully with power consumption of about 0.1 mW, delay is about 3.109 ns.

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