RESEARCH ARTICLE OPEN ACCESS

Design and Simulation of Low Noise Amplifiers at 180nm and 90nm Technologies

Fathima Janisha[1], Lekha Pankaj[2],
Associate Professor,AWH Engineering College Dr.Shahul Hameed,Professor At TKM College Of Engineering

ABSTRACT
With continued process scaling, CMOS has become a viable technology for the design of high-performance low noise amplifiers (LNAs) in the radio frequency (RF) regime. This thesis presents design and simulation of LNA at 180nm and 90nm technology. The LNA function is used to amplify signals without adding noise. The work is done on Cadence Virtuoso platform and the performance parameters like transient response and Noise figure are simulated and plotted. A supply voltage of just 5mV is used here. The noise figure at 180nm is found to be 259.722mdB at 1.04502GHz and The noise figure at 90nm is found to be 183.21mdB at 1.157GHz. 1.04502GHz and 1.157GHz are the peak frequency obtained from the frequency response of the Low noise amplifier. It is observed that the noise figure varies in each technology.
Index Terms: Low Noise Amplifiers, Noise Figure

I. INTRODUCTION

The growth of wireless services and other telecom applications has pushed the semiconductor industry towards complete system-on-chip solutions. Wireless systems comprise of a front-end and a back-end section. The front-end section processes analog signals in the high radio frequency (RF) range while the back-end section processes analog and digital signals in the baseband low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications. It lies typically from 100 KHz to 100 GHz. However in general, frequencies below 1 GHz are considered baseband frequencies while those greater are described as RF. The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver. Such an amplifier is referred to as a Low Noise Amplifier and forms an essential component of any RF integrated circuit receiver.

LNA is a special type of electronic that widely used in wireless communication system. Generally, the main goal of LNA design is to achieve simultaneous a low noise and high power gain for the given power dissipation and frequency condition . There are several fundamental low noise amplifier topologies for single ended narrow band low power low voltage design, such as resistive termination common source, common gate, shunt series feedback common source, inductive degeneration common source, cascode inductor source degeneration. The design is based on a cascode configuration including feedback to the common source amplifier for simultaneous noise and input impedance matching. This project describes the operation and the simulation of gain and minimum noise figure using 180nm and 90nm CMOS technology.

The objective of this project is to perform circuit level design, simulation and measurement, including circuit analysis and verification of a low noise amplifier circuit **.** This low noise amplifier will produce a gain more than 10dB and noise figure less than 3dB. Section II will discuss the design and the process of the low noise amplifier. Section III will discuss on the result of the simulation for the low noise amplifier and finally Section IV will discuss on the analysis of project. And finally the last section draws the conclusions obtained from the simulation results and the future scopes.

II. LNA TOPOLOGY

Low noise amplifier is the first stage in the receiver design. Because the operating frequency of LNA is in RF frequency band, the circuit should be as simplified as possible, especially for the RF path. Otherwise the circuit noise becomes too high. Moreover, if the circuit is complicated, the parasitic effects may distort the amplified signal. Hence, there are several fundamental low noise amplifier topologies for single ended narrow band low power low voltage design, such as resistive termination common source, common gate, shunt series feedback common source, inductive degeneration common source, cascode inductor source degeneration, which are shown in Fig.1.

All of these designs has a tradeoff between gain and performance. For example gain is very high in cascade amplifiers but the stability is less or even chip size is large.In the inductive source degeneration design,low noise and high gain is achieved but stability can be critical issue for non differential

topologies because of undesired feedbacks in ground[4][5]

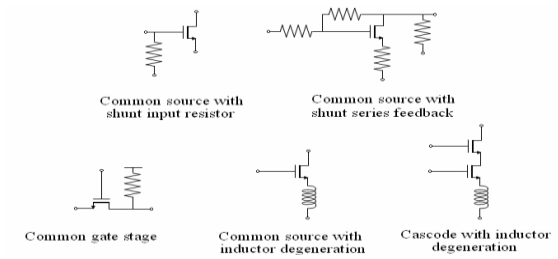

Fig.1. Low Noise Amplifier Topologies

III. LNA Design

The final and complete schematic of the LNA is shown in Figure 2. Here all the inductors (L1,L2,L3) are implemented as on chip spiral inductors. Amongst all the input matching methods namely resistive termination, series shunt feedback, common gate and inductive degeneration, the last one is selected simply because it offers the lowest noise figure. The minimum noise figure in resistive termination is 3 dB because of the thermal noise offered by the resistor at the gate of the transistor. The minimum noise figure offered by common gate configuration is 2.2 dB even though no resistors are present here. Inductive degeneration topology offers the lowest noise figure and no resistors are required here. It is called inductive degeneration because the L3 inductor is connected in such a way that the current through it opposes the current through the gate of the transistor M1 (negative feedback). This negative feedback connection is vital because it provides the necessary stability the circuit needs as well as improves a wide array of parameters.[1]

The transistor M2 is connected in common gate connection and the transistor M1 is connected in common source connection. Together they form a cascode, this cascode connection is necessary to provide the required isolation between the input and the output, reduce the effect of miller effect caused by gate-drain capacitance Cgd of the M1 transistor. The inductors L1 and L3 are chosen in such a way as to provide matching to the output resistance of the antenna . Their combination forms the input resistance (Rs) where is matched to the output of the antenna for favorable results.

The transistor M3, R1 and R2 forms the biasing circuit. They are used to set the prerequisite DC voltage so that the transistor can operate in the correct region (Region 2 in this case). Transistor M1 forms a current mirror with the transistor M3, whose width is just a fraction of the width of M1 to minimize the current through it and hence save power. The current through the transistor M3 is set by the supply voltage as well the resistor R1 which is chosen to be around 500Ω. The resistor R2 has to be large enough so that the equivalent noise current is small enough to be ignored. Here it is chosen to be around 5KΩ (optimized). The capacitor C3 forms the final piece of the DC biasing circuit. It acts a DC blocking capacitor and should be large enough to provide a negligible reactance at the frequency of 1.57542 Ghz. Here it is chosen as 1.2Pf.[1]

The inductor L2, Capacitor C2 and the resistor R3 form the output matching circuit. Output matching is once again crucial so as to provide maximum power to the subsequent stage of the LNA which is usually a mixer or in some cases a band pass filter for image rejection. Together they form a parallel tank circuit as opposed to a series tank circuit at the input of the transistor M1.

Supply voltage used here is just 0.5V. At the input of the LNA an AC source with a sweep of -10dbm and an amplitude of 1V is modeled. The resistor R3 is known as the output loading resistor which provides stability but reduces the gain as well as the compression point.

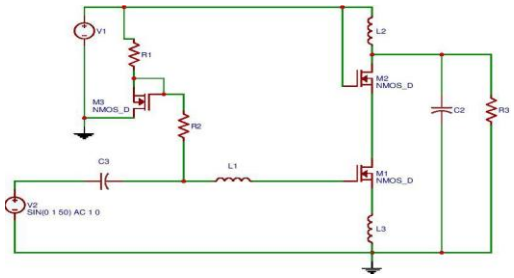

Fig.2. Schematic of LNA

A. *Component Design*
Design of LNA at 180nm

STEP 1: *Calculation of gate-oxide Capacitance (Cox)*

$$Cox=\varepsilon_{ox}/t_{ox}$$

$$\varepsilon_{ox}=\varepsilon_o * \varepsilon_r$$

Where ε_{ox}=Permitivity of gate oxide
t_{ox}=Thickness of gate oxide
$\varepsilon_{o=}$Free space permittivity
$\varepsilon_o=8.854*10^{-12}$ F/m
$\varepsilon_r=3.9$

Hence we get

$\varepsilon_{ox}=3.45*10^{-11}$ F/m

so

$$Cox=3.45*10^{-11}/4.1*10^{-9} \quad (1)$$
$$=8.42*10^{-3}\ F/m^2$$

STEP2: *Calculation of optimum width of the transistor M1*

$$W_{opt}=1/(3.Cox.\omega.L.R_s) \quad (2)$$

Where Cox=Capacitance of the gate oxide
ω=Angular Frequency
L=Lengthof the device
R_s=Source Resistance

Hence we obtain

$W_{opt}=\frac{1}{3(8.42*10^{-3})*(2\pi*1.57542*10^{9})*(180*10^{-9})*50}$=444µm

Step 3: Calculation Of Gate-Source Capacitance (Cgs)

$$Cgs=\frac{2*Wopt*Cox*L}{3} \quad (3)$$

Substituting the values Wox=444 µm, Cox=8.42*10^{-3} F/m^2 and L=180nm,
we get Cgs=449 fF

Step 5: Calculation of Source inductor L3

Input impedance looking into the LNA,

$$Z=j\omega L_s+\frac{gm.Ls}{Cgs}+\frac{1}{j\omega Cgs} \quad (4)$$

The individual inductance and capacitance part would be resonated out and the remaining part should be effectively equal to 50Ω, so we get

$$\frac{gm.Ls}{Cgs}=50$$

Substituting the values of g_m and c_{gs} in the above,we get L_s=400pH

STEP 6*: Calculation of Gate inductor L1*

We are employing a series resonant circuit at the input, to set the resonant frequency. The resonant frequency of a series resonant circuit is as follows:

$$F=\frac{1}{2\pi\sqrt{(L_s+L_g)Cgs}} \quad (5)$$

Substituting the obtained values of $L_s$and Cgs, we get L_g=22nH

Step 7: Calculation of output inductor

The equation that governs the output matching is as follows:

$$Z = g_m r_{ds} Z_s + Z_s + r_{ds} \quad (6)$$

Where g_m is the transconductance,
r_{ds} is the drain to source resistance,
Z_s is the source impedance.

The formula for the resonant frequency of a parallel resonant circuit is as follows:

$$F=1/2\pi\sqrt{\frac{1}{LC}-\frac{R^2}{L^2}} \quad (7)$$

We need to work on the formula of Z twice as we have two cascaded amplifiers, by substituting the values of g_m,r_{ds} ,Z_s , R and C values of the parallel resonant circuit we obtain the value of L as approximately 17.7 nH.

Design of LNA at 90nm

Step 1: *Calculation Of Gate-Oxide Capacitance (Cox)*

$$Cox=\varepsilon_{ox}/t_{ox}$$
$$\varepsilon_{ox}=\varepsilon_o * \varepsilon_r$$

Where ε_{ox}=Permitivity of gate oxide
t_{ox}=Thickness of gate oxide
ε_o=Free space permittivity
ε_o=8.854*10^{-12} F/m
ε_r=3.9

Hence we get

ε_{ox}=3.45*10^{-11} F/m

so

Cox=3.45*10^{-11}/4.1*10^{-9}
=8.42*10^{-3} F/m^2

Step2: Calculation of optimum width of the transistor M1

$$W_{opt}=1/(3.Cox.\omega.L.R_s)$$

Where Cox=Capacitance of the gate oxide
ω=Angular Frequency
L=Length of the device
R_s=Source Resistance

Hence we obtain

$W_{opt}=\frac{1}{3(8.42*10^{-3})*(2\pi*1.57542*10^{9})*(90*10^{-9})*50}$=888µm

Step 3: Calculation of gate-source capacitance (Cgs)

$$Cgs=\frac{2*Wopt*Cox*L}{3}$$

Substituting the values W_{opt}=888 µm, Cox=8.42*10^{-3} F/m^2 and L=180nm, we get Cgs=448.61 Ff

Step 4: calculation of source inductor l3 input impedance looking into the lna,

$$Z=j\omega L_s+\frac{gm.Ls}{Cgs}+\frac{1}{j\omega Cgs}$$

The individual inductance and capacitance part ould be resonated out and the remaining part should be ffectively equal to 50Ω, so we get

$$\frac{gm.Ls}{Cgs}=399pF$$

Substituting the values of $g_m$andc_{gs} in the above, we get L_s=400pH

III. SIMULATION

The schematic of fully inductive degeneration LNA designed is shown in Fig. 3.The simulation is done using Cadence EDA tools-Virtuoso Schematic Editing and it is Simulator Spectre.

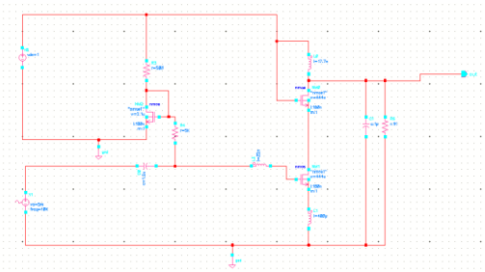

Fig.3 Schematic of inductive degenerated LNA

A. Simulation Results

Frequency response:

Frequency responses of the LNA at different technologies were found from dc analysis. The Frequency Response for the LNA obtained at 180nm technology is shown in the figure 4 and the peak frequency is found to be 1.047GHz.The Frequency Response for the Low Noise Amplifier obtained at 90nm technology is shown in the figure 5 and the peak frequency was found to be 1.157GHz.

Noise Figure:

The noise figure in dB(Noise Factor) of the LNA at different technologies were found from the S-Parameter analysis.The Noise Figure for the Low Noise Amplifier at 180nm technology for the peak frequency 1.047GHz is shown in figure 6, and it is found to be 259.175 mdB.Also, the Noise Figure for the LNA at 90nm technology for the peak frequency 1.157GHz is shown in figure 7, and it is found to be 145.84mdB.From both these analysis, it is found that the 90nm technology has lesser Noise Factor compared to the 180nm technology. Table1 shows the performance comparison of the Low Noise Amplifiers at both 180nm and 90nm technologies.

Table 1 Performance Comparison

Parameter	1	2
Technology	180nm	90nm
Transistor Length	180nm	90nm
Supply Voltage	0.5V	0.5V
Peak Frequency	1.047GHz	1.157GHz
Gain	46.020dB	46.020dB
NF(dB)	259.175 mdB	145.84mdB

B. Simulation figures

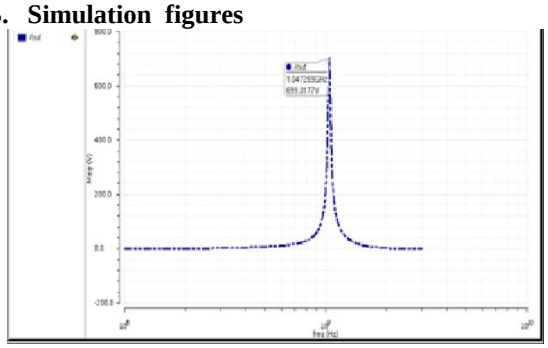

Fig.4. Plot for frequency response of LNA at 180nm Technology

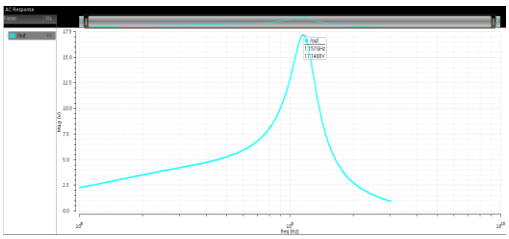

Fig.5 Plot for frequency response of LNA at 90nm Technology

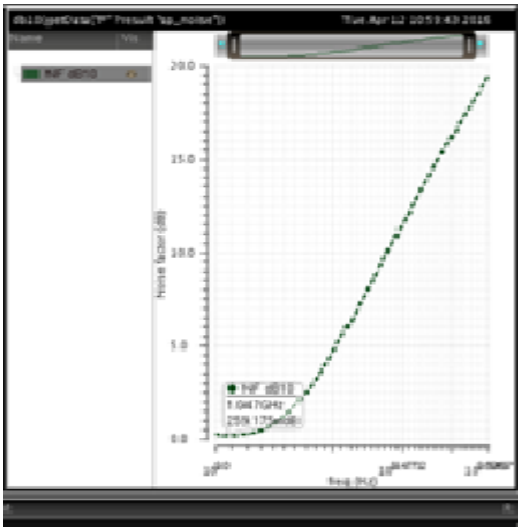

Fig.6 Plot for Noise Figure of LNA at 180nm Technology

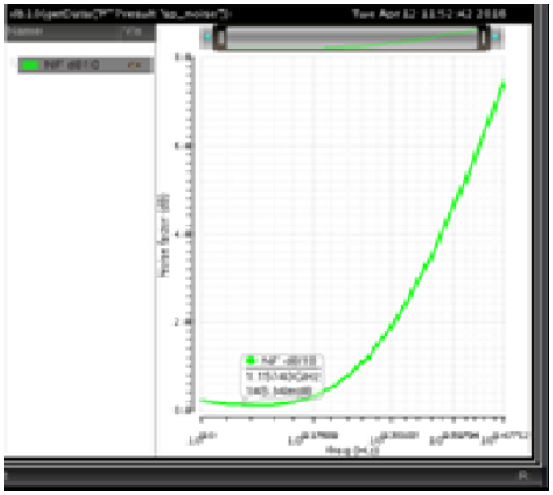

Fig.7. Plot for Noise Figure of LNA at 90nm Technology

IV. CONCLUSION

A Low voltage CMOS Low noise amplifier was designed at 180nm and 90nm technology in cadence virtuoso platform at gpdk180 and gpdk 90 libraries respectively.The Noise figure for both the technologies were compared at the peak frequency obtained from the frequency responses of both the LNA. From the analysis it is seen that the Noise figure at 90nm (145.84mdB) is less than the noise figure at 180nm(259.175 mdB).

Though the responses are satisfactory, but still there are scopes to improve the performances. Some of the circuits can be improved in design and with more proper optimization to have better responses. Many other parameters of the device can be studied and analysed. The layout can also be designed with

zero errors in both DRC and LVS so that the design can be fabricated without any off-chip components.

REFERENCES

[1]. Ke-Hou Chen, Jian-Hao Lu, Bo-Jiun Chen, and Shen-Iuan Liu, "An ultra-wide-Band 0.4–10-GHz LNA in 0.18um CMOS," IEEE Transaction on Circuits and Systems II: Express Briefs, vol. 54, no. 3, pp. 217- 221, March 2007

[2]. Shaeffer, D.k; Lee T.H. ; Center for integrated systems, stanford university, " A 1.5V, 1.5Ghz CMOS low noise amplifier," IEEE journal on solid-state circuits, Volume: 32, Issue: 5, May 1997

[3]. Jenn-Tzer Yang; Yuan-Hao Lee; Yi- Yuan Huang; Yu-Min Mu, "A 0.18μm CMOS using High- Q Active inductors for Multi-band Low noise amplifier," IEEE conference on Electron device and Solid-state circuits, 2007

[4]. Shervin Ehrampoosh, Ahmad Hakimi, "High gain CMOS Low Noise Amplifier with 2.6 GHz Bandwidth", International Conference on Communication Engineering, Dec.2010

[5]. F.Ellinger , "Radio Frequency Integrated Circuits and Technologies," Springer:New York 2007

[6]. Bhasin, H; Handa, M; Kumar, S; Kanaujia, B.K., " Optimization of noise figure and gain of a CMOS RF low noise amplifier", International conference on Industrial and Information systems, 2014.

[7]. The text " High Frequency and Microwave engineering" by E. da Silva, Butterworth Heinemann.

[8]. Wang Peng, Hao Qing, Wang Jian, Chen Yaqin, "Design of C-band low noise amplifier with switch," In Proceedings of the IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT '07). pp. 1-3, April 2007.