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High- Throughput CAM Based On Search and Shift Mechanism

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ABSTRACT
This paper introduces a search and shift mechanism for high throughput content-addressable memory(CAM). A CAM is a memory unit that process single clock cycle content matching instead of addresses using well dedicated comparison circuitry. Most mismatches can be found by searching a few bits of a search word. The most critical design challenge in CAM is to reduce power consumption associated with reduced area and increased speed. To lower power dissipation, a word circuit is often divided into two sections that are sequentially searched or even pipelined. Because of this process, most of match lines in the second section are unused. Since searching the last few bits is very fast compared to searching the rest of the bits, throughput can be increased by asynchronously initiating second-stage searches on the unused match lines as soon as a first-stage search is complete. A reordered overlapped search mechanism for high throughput low energy content addressable memories (CAMs) is the existing method. By this method the latency and throughput does not shows a better improvement.
Here a method of search and shift mechanism for cam is proposed to improve the latency and throughput. This method also reduces power consumption. Here a cache memory is using to store the compared result. This will reduce the number of registers used for output bits. A 32x16 bit CAM is implemented and evaluated using Xilinx simulation. Thus the proposed method improves the latency by k+1 cycles and throughput by K cycles and reduces the power consumption also.
Index Terms: Asynchronous, CAM, Latency, Throughput

I. INTRODUCTION

Content-addressable memory (CAM) is a special type of computer memory used in certain very-high-speed searching applications. It is also known as associative memory and execute a look up-table function in parallel. CAM compares input search data against a table of stored data, and returns the address of the matching data. CAMs have a single clock cycle throughput making them faster than other hardware- and software-based search systems. An input search word is compared with a table of stored words and the matching word is obtained at high speed through a parallel equality search. CAMs can be used in a wide variety of applications requiring high search speeds. CAMs are used for many applications, such as parametric curve extraction, Hough transformation, Lempel-Ziv compression, a human body communication controller, a periodic event generator, cache memory, a virus-detection processor, and packet forwarding and packet classification in network routers. The primary commercial application of CAMs today is to classify and forward Internet protocol (IP) packets in network routers. In networks like the Internet, a message such an as e-mail or a Web page is transferred by first breaking up the message into small data packets of a few hundred bytes, and, then, sending each data packet individually through the network. These packets are routed from the source, through the intermediate nodes of the network (called routers), and reassembled at the destination to reproduce the original message. The function of a router is to compare the destination address of a packet to all possible routes, in order to choose the appropriate one.

A CAM is a good choice for implementing this lookup operation due to its fast search capability. However, the speed of a CAM comes at the cost of increased silicon area and power consumption, two design parameters that designers strive to reduce. As CAM applications grow, demanding larger CAM sizes, the power problem is further exacerbated. Reducing power consumption, without sacrificing speed or area, is the main thread of recent research in large-capacity CAMs. CAMs often contain a few hundred to 32 K entries for network routers, where each entry or word circuit contains several dozens of CAM cells. Each input-search bit is compared with its CAM-cell bit and the comparison result determines whether a pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on or off states.

In CAM each word circuit contains several dozens of CAM cells. Each input-search bit is compared with its CAM-cell bit and if the comparison matches then the pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on state, else it will be in off state. CAM cells are classified into two types: NOR and

NAND NOR and NAND. A NOR-type word circuit operates at high speed because pass transistors are connected between a ML to a ground line in parallel; however it consumes large power dissipation.

It is because mismatched word circuits discharge their ML capacitances to the ground line, where most of the word circuits tend to be mismatched in a CAM. In contrast, a NAND-type word circuit operates at medium speed because pass transistors are connected serially between a ML to a ground line. Because very few matched word circuits discharge their ML capacitances, a NAND-type word circuit reduces the power dissipation of MLs compared to the NOR-type word circuit. A pipelined approach is a general solution to improve the throughput. In pipelined approach the match-lines are divided into two pipeline segments, each segment with its own MLSA to decide if there is a match and its own pipeline flip-flop to store the outcome of the match operation for the segment. Segmenting the match-lines saves power because most words will miss in the first segment, eliminating the need to activate the subsequent segments. To save search-line power, one would ideally use low-swing signalling on the SLs. In the existing system we have a reordered overlapped search mechanism for a high-throughput low-energy CAM. It includes two new approaches: a reordered word-overlapped search (RWOS) at the scheduling level and phase-overlapped processing (POP) at the circuit level.

In a CAM, most mismatches can be found by searching a few bits of a search word. In the proposed CAM, a NAND-type word circuit is partitioned into two segments of different sizes that sequentially operate. Only when an input sub-word matches a stored sub-word that is the last few bits of a stored word in the smaller first segment, does the larger subsequent segment operate using its subsequent sub-word. Because of this process, most of the subsequent segments are unused. An input word is assigned to word circuits at a rate based on the short delay of the first segment instead of the long delay of the whole word circuit.

In the proposed method a new architecture is used to improve the efficiency of the CAM block by adding cache memory. As long as consecutive input words match in unused different word circuits, the CAM properly operates at a rate based on the short delay. A pre-computation block checks the last few bits of consecutive input words. If they are found to be the same, then the next search is only initiated once the current search has completed in both segments. For applications that would store random patterns in the last few bits of stored words, such as caches, the probability of the usage of the same first segment is very small. Moreover, input words are reordered to reduce the probability when the last few bits of consecutive input words are the same. Hence, CAM can operate at high speed based on the short delay because the long delay rarely affects the throughput. At the circuit level, the POP scheme can take full advantage of the RWOS scheme for further through put.

In a traditional synchronous CAM, all word circuits are controlled by a global clock signal and hence they periodically operate using two phases. In contrast, in the proposed POP scheme, each word circuit is designed using asynchronous circuits. As each word circuit is independently controlled using its local control signal, unused word circuits are on the evaluate phase, while the others are on the precharge phase. In combination with the RWOS scheme, input search words match in unused different word circuits whose MLs have already been pre-charged. Therefore, new search words are immediately processed without wasting the precharge time. Along with these existing techniques the proposed method adds the cache memory which further improves the throughput. Hence the proposed method we can increase the efficiency of searching mechanism using cache memory by little increase in latency during worst path.

The rest of this paper is organized as follows.Section II describes about the existing method.Section III describes about the proposed methodand section IV describes about the evaluation and performance comparison

II. REORDERED WORD OVERLAPPED SEARCH

This existing method is an extension of word overlapped search method. In the word overlapped search the input bits are divided into k bits and n-k bits.This scheme reduces the probability of slow mode to improve the throughput. Here the last bits of a current search word are compared with the last bits of m consecutive search words and an extra search word followed by the current search word. If the m consecutive sub-search words are different from the current sub-search word, the CAM operates at the fast mode. Otherwise, one of the m sub-search words that is the same as the current sub-search word is replaced by the extra sub-search word. In this case, the extra sub-search word has to be different from the current sub-search word.

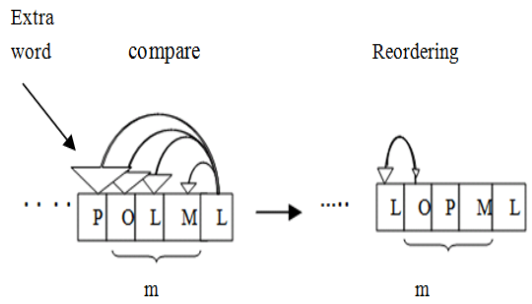

Fig1. Reorderd word overlapped search mechanism

In the example shown in Figure.1 the current sub-search word is "L," while the input buffer has "M," "L," and "O." In this case, as the second sub-search word "L" is replaced by the extra sub-search word "P," the current sub-search word "L" is different from all m consecutive sub-search words in the input buffer. Therefore, the CAM keeps operating at the fast mode. This method of reordering with a dummy word will take a longer time for the operation. This method doesnot show a better throughput and latency. Here throughput is equal to n cycles. The number of registers using is high. Power consumption is also high.

III. SEARCH AND SHIFT MECHANISM

In this section we propose a search and shift mechanism to improve the throughput and latency. In the proposed method, the total number of available bits are divided into k bits and n-k bits. Considering a 32 bit word we can divide them by setting k as 10 bits and n-k bits as remaining 22 bits. Proposed method is based on a search and shift mechanism and it uses a cache memory for storing the matched data.

The working of the system starts only when the cam enable signal goes high. Then only the input value is taken and then hold it throughout the operation. Firstly the k bits are searched by search and shift mechanism. Comparing each bit of input and memory by shifting the bits .Here only one register is using for this purpose. Each bits are shifted to one register and compared. Thus the name shift and search.

On comparing the data input and memory value using an xnor operation an enable signal will be generated if bits match. This signal is fed back to the shifters for shifting the next bit. This will depend upon the value of enable signal At the time when k bit search is initiated then a down counter is enabled. The n-k bit parallel search is delayed using this counter so that timing issue is removed. It will wait for the k bit search to complete. When the counter value reaches a 1 an internal enable signal is generating. This is for solving the timing issues of the system. This signal will inform the system about when we need to capture the values, outputs e.t.c. The comparison of n-k bits takes place parallely. Each input value is compared against the memory value by exor operation. This will generate another enable signal. These three enable signals are fed to an and gate which will produce a high enable signal. This in turn fed to a cache memory. From there the output address of the matched word is obtained.

The address is represented as one hot address. This will reduce the dynamic power. One hot address representation has got many advantages. High speed, lesser dynamic power, decoding complexity is less e.t.c. Priority encoder is used here in order to solve the problem of multiple match location. Overall design of the system will improve the throughput, latency, power consumption and area used. Here the method is based on a shift and search mechanism. If any one of the enable signal is 0 then whole operation will stop.

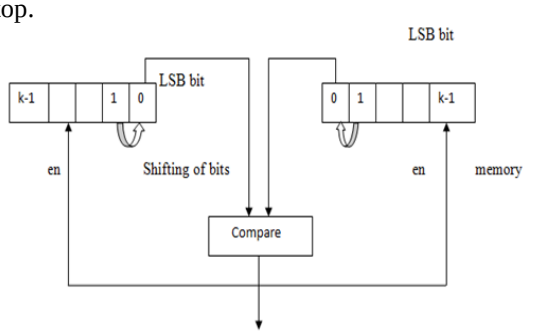

Figure 2. Diagram showing k bit search

In this mechanism K bit searching requires only one register for comparing the values.. First the LSB bit of input is compared against the LSB bit of memory. This is done using xor operation. If the comparison result is a true value then the enable signal is fed back to the shifter, then next bit is shifted and compared. The same shifting is occurring in memory also. These k bit and stored bits in the memory are searched for a match. If a match is found then enable signal will be active.

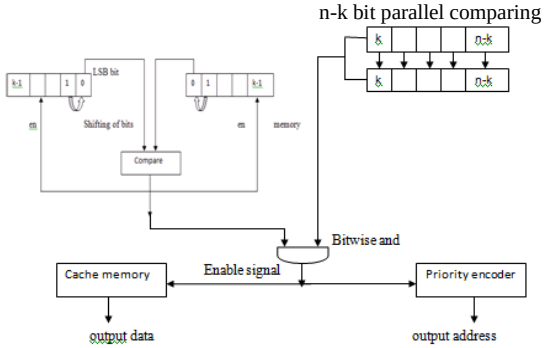

Fig3. Working diagram of the proposed architecture

The enable signals (en) generate depending on the comparison results. Three enable signals are generating. One from k bit search, one from n-k bit search and the other one is an internal enable signal. This signal is for capturing outputs at the correct time.

These three enable signals are fed to a bitwise and operation to produce a single enable signal. If these three enable signals are high then only the and operation gives a true value. If this signal is high then cache memory is activated for storing the data. This will avoid the frequent updation of cache memory. Thereby reducing the power consumption. Data stored in cache memory can be used for further needs. The output address of matching location is obtained as one hot address. This will also reduces power consumption because of the avoidance of toggling bits. The usage of priority encoder will resolve the issue of matching of multiple location. Each location will be assigned with a priority value. Throughput and latency shows a better improvement in this method. Latency is the time interval between the arrival of input and output whereas throughput is the time interval between the arrival of consecutive inputs. Here throughput is K cycle and latency is K+1 cycles

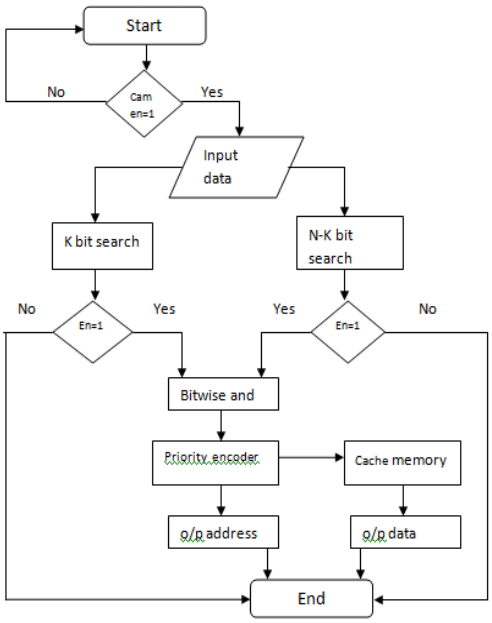

Fig 4. Flow chart showing the working of CAM using search and shift mechanism

Here in this proposed method, the throughput depends on K value whereas in overlapping mechanism it depends on the nbit value. Here Latency is K+1.This is a better improvement than the existing method. Cache memory is using for storing the data value. It is just like storing in an internal memory. We can take the data values for further requirements.

IV. EVALUATION

A 32X16 bit CAM is implemented for high throughput applications. Here the K value for proposed system is chosen as 10. Therefore th first segment is a 10 bit word and the remaining bits will form the second segment. These CAMs are implemented and evaluated by Xilinx simulation. This proposed CAM is implemented using Virtex 5 FPGA kit.

A. Performance Comparison

The proposed method when compared with the result of existing method shows that there is a better improvement in throughput and latency. Throughput of the proposed method is equal to the k cycles .Here K is set to 10. So throughput is 10 clock cycles. This result is far better than the existing system. Latency of proposed system shows a better improvement than the existing system. The existing method has a higher latency which is equal to the n cycles ie 64 clock cycles. In search and shift mechanism it is equal to the k+1 cycles.

Here latency is equal to K+1.ie 11. In the existing system xor operation is using always. But in the proposed method bit by bit analysis make an xor operation only if the comparison of previous bits are true. Here in this method the LSB of k bit is compared against the LSB of value stored in memory. If that comparisons yields to a true value then next bit is shifted and comparison takes place. In reordered overlapped search if a bit is compared truly then it is replaced .Then a dummy value is placed to that position and compared. This will take a longer time than the existing method. Proposed method has a special flop with multicycle path. It is a type of hold+latch. This means the input value is holding throughout the process. A cache memory is added in the proposed method. Here the compared value is stored when it shows a match. This is working on the basis of 3 enable signals coming from the comparison operations. By using this cache memory 32 bit data value can be stored and can be used whenever needed.

Existing method uses registers for storing each of these bits in the output. But here by using this cache memory we are reducing the number of registers.

B. Analysis Of Power

In the proposed method power is reducing considerably. Here there is a cache memory for storing the matched result. Here the complete value is storing only when the comparison of entire data shows a match. So there is no need of updating the cache frequently. This will reduce the dynamic power which is a major source of power consumption. In the existing method each and every time the comparison result is registering. So this will lead to power consumption.

In search and shift mechanism address of matched location is represented using one hot address. So this has got many advantages. High speed, lesser dynamic power, decoding complexity is less e.t.c. Here in this representation bit toggling is not taking place. This will also result in lesser power consumption.

Analysis Of Latency And Throughput

Latency is the time interval between the arrival of input and output whereas throughput is the time interval between the arrival of consecutive inputs.

Latency of proposed system shows a better improvement than the existing system. The existing method has a higher latency which is equal to the number of bits n ie 64 clock cycles. In search and shift mechanism it is equal to the k+1. Here latency is equal to K+1.ie 11. Throughput of the proposed method is equal to the k bits whereas in existing method it is equal to n cycles.Here K is set to 10.So throughput is 10 cycles. This result is far better than the existing system.

Table I Performance Comparison

parameter	Existing method	Proposed method
Throughput	64 cycles	10 cycles
Latency	64 cycles	11cycles

V. CONCLUSION

This paper focuses on the design of a cam memory based on search and shift mechanism for improving the throughput and latency of the system. In this method the total number of input bits are divided into two sections as k bits and n-k bits. K bits are searched using shift and search mechanism and the remaining bits are compared parallely. The timing issue between these two comparison methods is solved using a counter. The counter value is set to k bits .The comparison results either shows a matching condition or mismatching condition. The comparison result yields to enable signals.

During the time of a matching condition the address of matched location is obtained and also the matched data is being stored in a cache memory. Cache memory is enabled using 3 enable signals coming from the comparison results. Therefore frequent updation of cache memory is not required thereby reducing the power consumption. The flops used here are of a particular type. Here we use a hold+latch method for the flop. This will hold the input value throughout the operation.

Here this shifting and searching operation takes places faster and thereby improving the throughput and latency. Throughput and latency shows a better improvement than previous designs. Usage of cache memory and onehot address representation reduces the power consumption also. The throughput of this method is K cycles and latency is equal to K+1 cycles.

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