

Implementing Neural Networks Using VLSI for Image Processing (compression)

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Abstract

Biological systems process the analog signals such as image and sound efficiently. To process the information the way biological systems do we make use of ANN. (Artificial Neural Networks)

The focus of this paper is to review the implementation of the neural network architecture using analog components like Gilbert cell multiplier, differential amplifier for neuron activation function and tan sigmoid function circuit using MOS transistor.

The neural architecture is trained using Back propagation algorithm for compressing the image. This paper surveys the methods of implementing the neural network using VLSI .Different CMOS technologies are used for implementing the circuits for arithmetic operations (i.e. 180nm, 45nm, 32nm).And the MOS transistors are working in sub threshold region. In this paper a review is made on how the VLSI architecture is used to implement neural networks and trained for compressing the image.

Key words: Artificial Neural Networks Back propagation algorithm

I. Introduction

The study of the human brain is thousands of years old. With the advent of modern electronics, it was only natural to try to harness this thinking process, and then the concept of neural network was developed by observing the processing capabilities of human brain. Computing is an information processing paradigm inspired by biological system composed of large number of highly interconnected processing elements(neurons) working in parallel to solve specific problems.

1.1 Neural Network

Intelligence is actually acquired and learned from the past experiences This intelligence though a biological word is realized based on mathematical

equations giving rise to development of artificial neural networks. These networks are realized by analog components like multipliers differential amplifiers.

An ANN is configured for specific application such as pattern recognition function or classification through a learning process.

Each biological neuron is connected to several thousands of other neurons, similar to powerful parallel computers and there are approximately 10 billion neurons in the human cortex. But the operating speed is measured in milli seconds while a silicon chip can operate in nano seconds.The human brain is extremely energy efficient compared to the best computers.

Artificial neuron model in biological terms

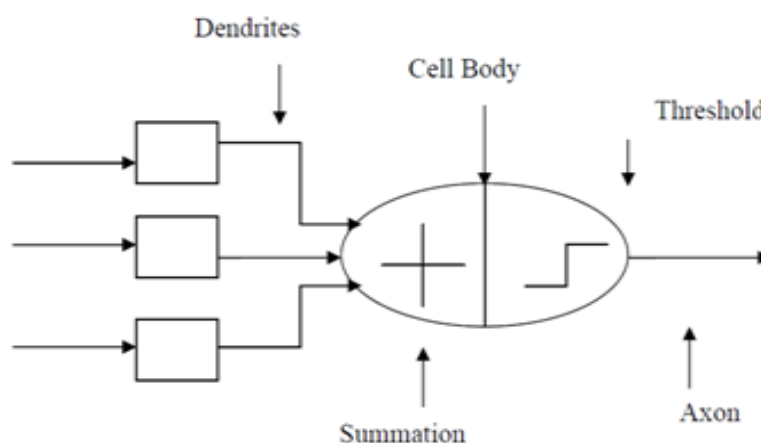


Figure 1: Artificial neuron model

1.2 Image Compression

Image compression is one of the key image processing techniques in signal processing and communication systems. Compression of images leads to reduction of storage space and reduces transmission band width and therefore the cost. Advances in VLSI technology are changing the definition of technological needs for common man. Image compression is one of the need.

Today's technological growth has led to scaling of transistors and hence complex and massively parallel architecture are possible to realize on dedicated hardware consuming low power and less area. This paper reviews the neural network architecture for image compression. The transport of images across communication paths is an expensive process. Image compression provides an option for reducing the number of bits in transmission, which in turn helps to increase the volume of data transferred in a space time, along with reducing the cost required. Compression has become more important in computer networks as the volume of data traffic has begun to exceed their capacity for transmission.

1.3 CMOS technology

The evolution of important parameters in CMOS technology like gate length switching performance and the required supply voltage has revolutionized the VLSI. The trend of CMOS technology

improvement continues to drive by the need to integrate more function within a silicon area. Different technologies used have the following features:

- ❖ Reduce the fabrication cost.
- ❖ Increase the operating speed.
- ❖ Dissipate less power.

The electronic industry has made phenomenal growth due to rapid advances in VLSI. The applications of VLSI in high performance computing, telecommunications is increasing at a very fast rate.

II. Design Architecture of Basic Components

2.1 Multiplier block

The Gilbert cell is used as the multiplier block. The output of the Gilbert cell is in the form of current. The schematic of the Gilbert cell is as shown in the figure

The Gilbert cell works in the subthreshold region. The current for the NMOS transistor to work in the subthreshold region is given by the following equation

$$I_{ds} = I_0 e^{q[V_g - nV_s]/nKT} (1 - e^{-qV_{ds}/nKT})$$

Where all the voltages V_g , V_s , V_d are taken with respect to the bulk voltage V_b .

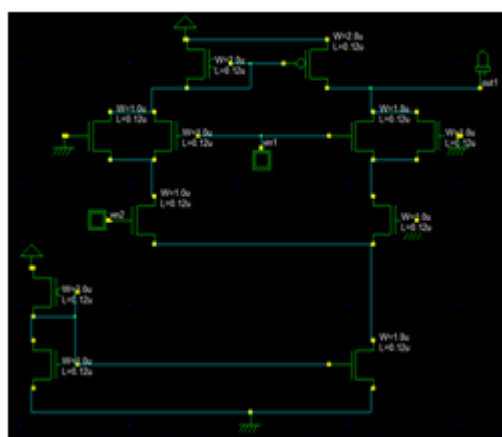
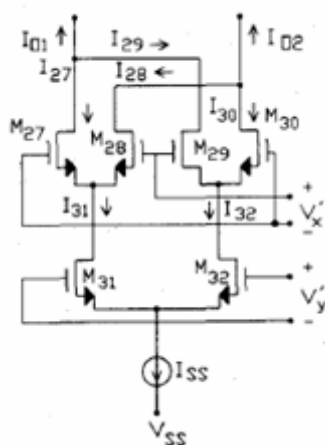


Figure 2: Gilbert cell circuit diagram and schematic diagram

2.2 Neuron activation function

Neuron activation function designed is tan sigmoid. The proposed design is actually a differential amplifier modified for differential output. Same circuit is capable of producing output of the activation function. Differential amplifier when design to work in the subthreshold region acts as neuron activation function.

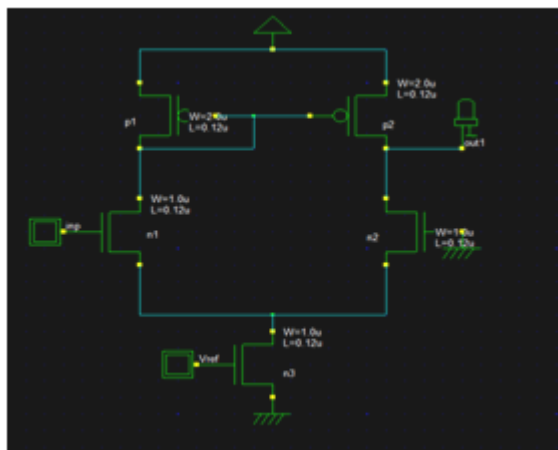
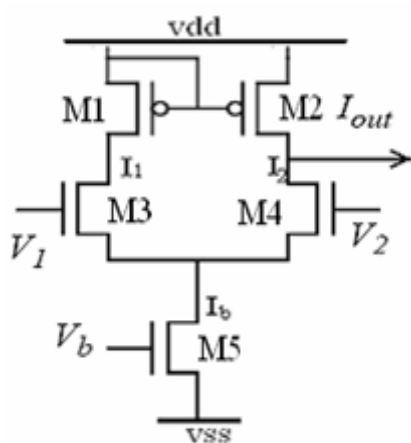


Figure 3: Differential amplifier circuit diagram and schematic diagram

III. Realization of Neural Architecture using Analog Components

The components designed are used to implement the neural architecture. The gilbert cell and differential amplifier used as activation function performs the multiplication function.

IV. Back Propagation Algorithm

The training is important part in neural architecture. It is the most common method used to train the artificial neural network to minimize objective function. It is the generalization of delta rule and mainly used for feed forward network. The Back propagation is divided into two phases.

The first phase is for propagation and the second is for weight update. In the first phase the training pattern is propagated forward to the neural network in order to generate the propagation output activation.

Then the output activations are propagated backward through the network in order to generate the deltas.

The weights of the network are chosen randomly and then the algorithm is used to do necessary corrections. The algorithm is stopped when the value of the error function has become sufficiently small.

V. Neuron Application- Image Compression

The network architecture proposed and designed in the previous section is used to compress image. Image consisting of pixel intensities are fed to the network shown in Figure 4 for compression and decompression. The 2:3:1 neuron proposed has an inherent capability of compressing the inputs, as there are two inputs and one output. The compression achieved is 50%. Since the inputs are fed in the analog form to the network there is no need for analog to digital converters. This is one of the major advantages of this work. A 1:3:2 neural networks is designed for the decompression purpose. The neural network has 3 neurons in the hidden layer and two in the output layer.

Figure shows the compression and decompression scheme. The training algorithm used in this network is Back Propagation algorithm. The error propagates from decompression block to the compression block. Once the network is trained for different inputs the two architectures are separated and can be used as compression block and decompression block independently.

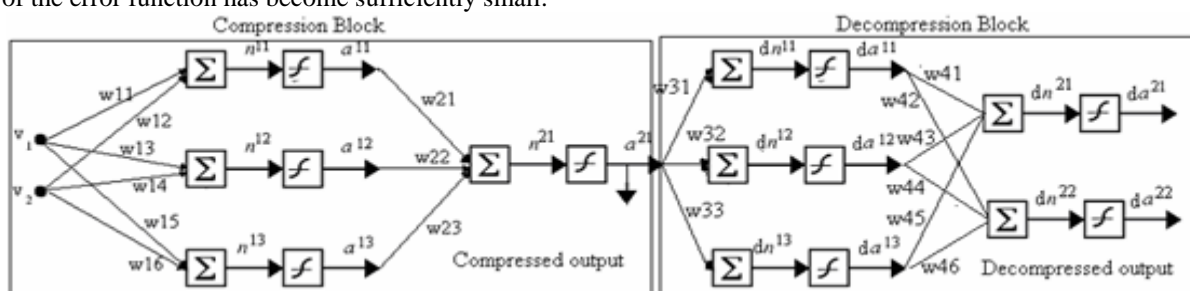


Figure 4: Image Compression and Decompression using proposed Neural architecture

VI. Conclusions

In this review paper we have discussed three concepts neural network architecture using VLSI and applying the concepts for image compression. Neural

network has remarkable ability to derive meaning from complicated or imprecise data can be used to extract patterns and to detect trends that are too complex to be noticed by either humans or other

computer techniques Gilbert cell multiplier, Neuron Activation function are used to design neural network.

Back Propagation algorithm is used to train the network.

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