

## A Novel Technique for Enhancing Speed of Successive Approximation Analog to Digital Converter

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### ABSTRACT

High resolution analog to digital converters (ADC's) have been based on self-calibrated successive approximation technique, because it uses a single comparator and consumes less power. Unfortunately successive approximation technique requires N comparisons to convert N bit digital code from an analog sample. This makes successive approximation ADC's unsuitable for high speed applications. This paper demonstrates a simple technique to enhance speed of successive approximation ADC's that require as few as N-3 comparisons for N bit conversion. This technique optimizes the number of comparator requirements while increasing conversion speed by 37.5% for 8-bit resolution. In our approach, the analog input range is partitioned into 8 quantization cells, separated by 7 boundary points. A 3-bit binary code 000 to 111 is assigned to each cell. A normal successive approximation converter requires 8 comparisons for 8-bit quantization, while our proposed technique reduces number of comparison requirements to 5 comparisons for 8 bit conversion. The results show that the ADC exhibits a maximum DNL of 0.47LSB and a maximum INL of 0.5LSB.

**Keywords** - ADC, Microcontroller, DAC, Sample and Hold. Successive approximation.

### I. INTRODUCTION

Analog-to-digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses  $2^{N-1}$  comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions [2]. All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flush architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially, consequently and this architecture requires very large IC's. It has high power dissipation.

The conventional pipelined architecture has been widely employed to meet the required performance in this arena due to properly managed trade-offs between speed, power consumption and die area [3]-[5]. Among a variety of pipelined ADCs, the multi bit-per-stage architecture is more suitable for high resolution, as the single bit- per stage structure requires more stages, high power consumption and larger chip area [6]. However the multi bit-per-stage architecture has a relatively low signal processing speed due to reduced feedback factor in the closed – loop configuration of the amplifiers. In switched capacitor type multiplying digital-to-analog converters (MDACS) used in conventional pipelined ADCs, the

mismatch between capacitors limits the differential non linearly (DNL) of ADCs. This is because each DNL step is defined by the random process variation of each unit capacitor value. A common centroid geometry layout technique can improve this capacitor matching for DNL, but it cannot have an effect on random mismatch [7]. Naturally increasing the capacitor size can directly improve the capacitor matching accuracy, but at the added cost of increased load capacitance. This means the amplifiers would dissipate more power or the ADC sampling speed would have to be reduced.

In this paper, a novel architecture is proposed to improve the sampling rate and the resolution of an ADC. The prototype ADC based on this technique needs only five comparisons instead of eight comparisons normally required in the conventional successive approximation techniques for 8-bit resolution. This can increase the speed of conversion. This paper organized as follows. The ADC architecture with the proposed technique is discussed in Section II. Circuit implementation is described in Section III and measured results of the prototype are summarized in Section IV. Finally, the conclusions are given in Section-V.

### II. ADC ARCHITECTURE

The block diagram of the proposed 8-bit ADC is illustrated in Fig. 1. It is based on a conventional successive approximation technique. The ADC consists of an input sample and hold amplifier (SHA), 8-comparators, one 8-bit DAC, 8-bit Microprocessor 8085 and some extra supporting circuit blocks. Seven comparators, partitions input

range into 8-quantization cells. The Microprocessor decides within which cell the input sample lies. This gives 3 MSB bits 000 to 111 according to the cell value. Remaining 5 bits are obtained by successive approximation technique.

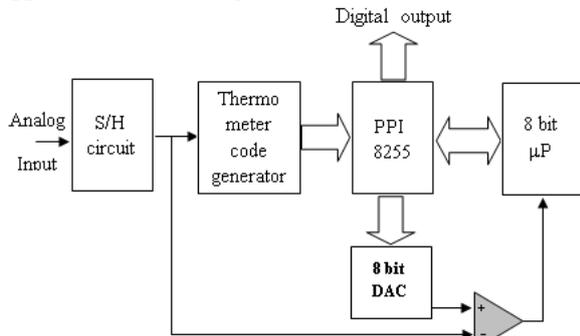


Figure 1: Block diagram of 8 bit ADC

A Circuit which partitions Analog input signal into 8-quantization cells as shown in Fig. 2, has 7 comparators and a potential divider network. During sampling all comparators samples the analog input voltage  $V_{in}$  simultaneously and generates thermometer Code. A binary count is loaded into the accumulator depending on the thermometer code, the detailed binary count loaded into accumulator for different thermometer code is summarized in table 1.

Table 1: Binary count corresponding to thermometer code

Thermometer Code	Binary count
00000000	00010000
00000001	00110000
00000011	01010000
00000111	01110000
00001111	10010000
00011111	10110000
00111111	11010000
01111111	11110000

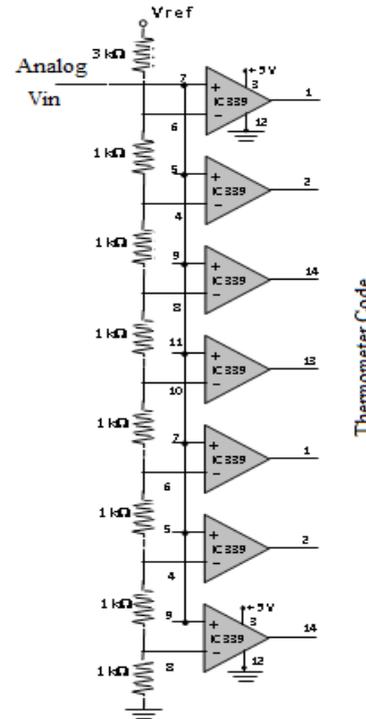


Figure 2 : Thermometer code generator

### III. CIRCUIT IMPLEMENTATION.

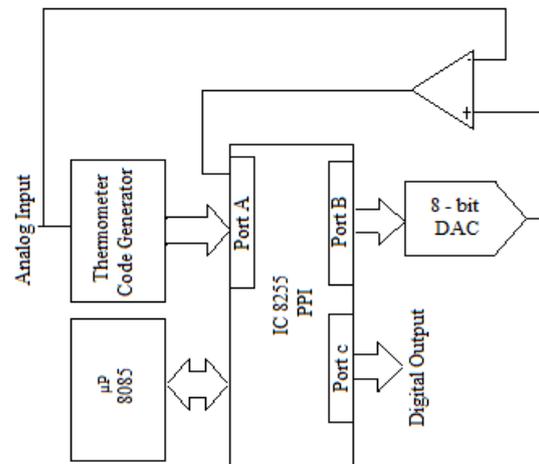


Figure 3 : Schematic diagram of 8 bit ADC

The Schematic diagram of the 8-bit ADC is as shown in Fig. 3. The PPI 8255 port A is used as input port which gets the thermometer code from comparator network and DAC comparator output. Port B is used as output port connected to 8-bit DAC to obtain analog signal equivalent to digital count in an accumulator, which is compared with an analog input voltage  $V_{IN}$ . After completion of five comparisons, count in the accumulator is digital equivalent of Analog input voltage  $V_{IN}$ , it is outputted to Port C. The software for successive approximation Analog to digital conversion is written in assembler codes and converted to hexadecimal code by the assembler software. Hex codes are transferred to the Microprocessor by a programmer. State diagram of the ADC is shown in fig. 4.

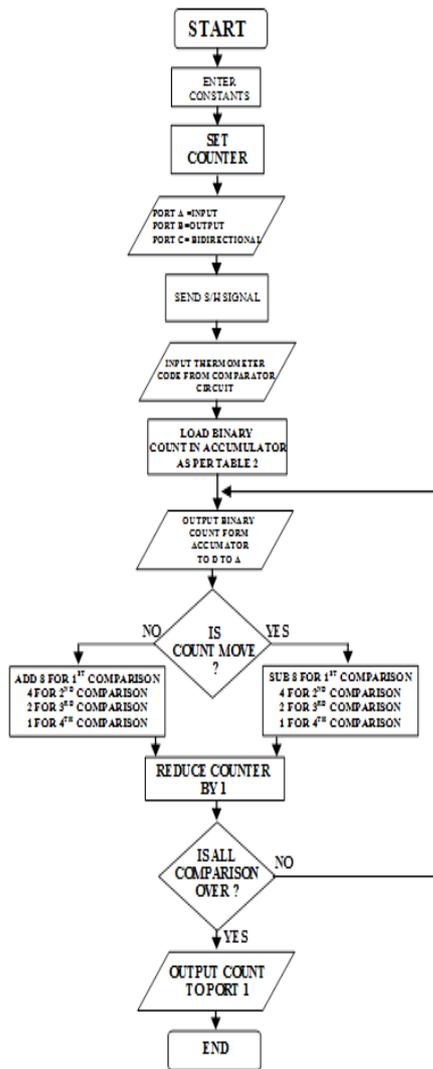


Figure 4 : State diagram

**IV. EXPERIMENTAL RESULTS**

Figure 5 shows the dc linearity of the ADC. In figure 5(a) differential nonlinearity (DNL) is plotted versus code, and in Figure 5(b) integral nonlinearity (INL) versus code is plotted. The magnitudes of the maximum DNL and INL are less than 0.45 and 0.5 LSB, respectively.

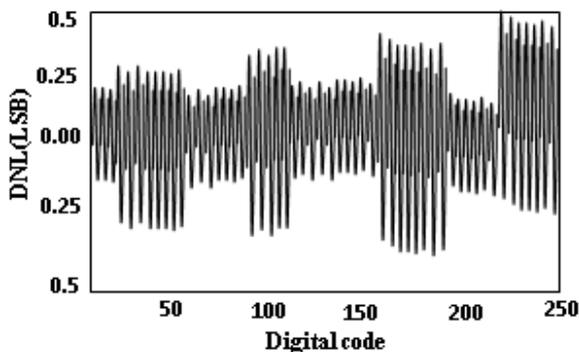


Figure 5(a) : Differential Non linearity(DNL) versus Code

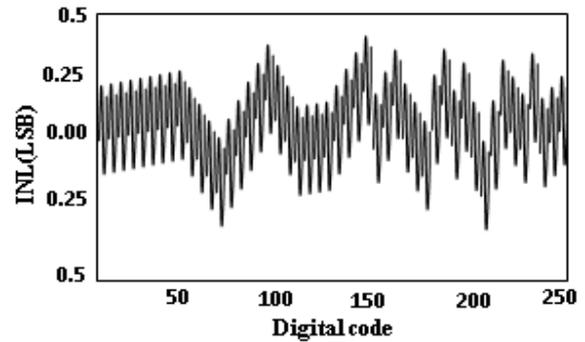


Figure 5(b) : Integral Non linearity (INL) versus Code

**V. CONCLUSION**

In this paper, a new architecture for Successive Approximation Analog to digital conversion is introduced. The proposed scheme reduces number of comparisons required to obtain digital data, which makes the quantization feasible with much higher speed, demonstrating the proposed Architecture is effective. An hardwired 8 bit prototype ADC is fabricated and tested.

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