RESEARCH ARTICLE OPEN ACCESS

Design of Aware Flip-Flop with Low Power Variations by P-Spice

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ABSTRACT
Excessive power dissipation causes overheating, which can lead multiple impacts like, packaging cost, reliability & functionality of IC and other soft errors. This naturally limits battery life of hand held equipments and need urgent solution to enable the proliferation of technology at large. Parameter variations in nanometer process technology are one of the major design challenges. They cause to be increased delay on the critical path and to change the logic level of internal nodes. The basic concept to solve these problems at the circuit level, design-for-variability (DFV), is to add error handling circuits at the conventional circuits so that they are robust to nanometer related variations. The state-of-the-art variation-aware flip flops are mainly evolved from aggressive DVFS (dynamic voltage and frequency scaling) -based low power application systems which handle errors caused from the scaled supply voltage. They only detect the timing errors and cannot correct the errors. We propose a variation–aware flip flop which can detect and correct the timing error efficiently. The experimental results show that the proposed variation aware flip flop is more robust and lower power than the existing approaches.

I. *Introduction*

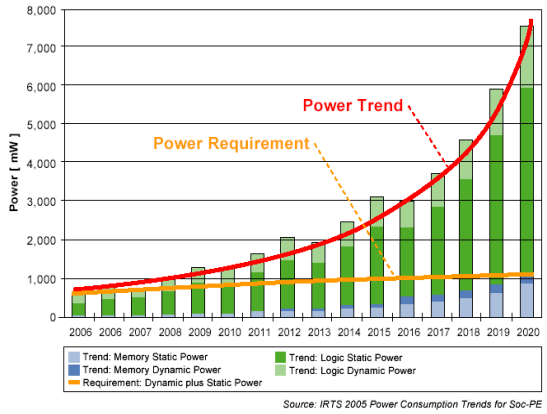
In order to increase the performance of digital integrated circuits, very aggressive scaling technology has been developed. According to ITRS roadmap , MPU physical gate length is expected to be 22*nm* in 2012. Due to the parameter variations and increased sensitivity to radioactive particles, it is very difficult to keep increasing the performance of nanometer process technology ruled by Moore's law. Compared to the micrometer ICs, nanometer ICs require smaller charge to maintain a logic level at the internal nodes. Thus, they are more susceptible to variations and external radioactive particles even at sea level. The sources of the variations are PVT (process (threshold, distortion of layout patterns during lithography), voltage (IR drop), and temperature). They also suffer from unreliability and aging problems (time-dependent variations) such as NBTI.

It's no secret that power is emerging as the most critical issue in system-on-chip (SoC) design today. Power management is becoming an increasingly urgent problem for almost every category of design, as power density—measured in watts per square millimeter—rises at an alarming rate.

In the last few years, design for low power has started to change again how designers approach complex SoC designs. Each of these revolutions has been a response to the challenges posed by evolving semiconductor technology. The exponential increase in chip density drove the adoption of language-based design and synthesis, providing a dramatic increase in designer productivity. This approach held Moore's law at bay for a decade or so, but in the era of million gate designs, engineers discovered that there was a limit to how much new RTL could be written for a new chip

project. The result was that IP and design reuse became accepted as the only practical way to design large chips with relatively small design teams. Today every SoC design employs substantial IP in order to take advantage of the ever increasing density offered by sub-micron technology.

Deep submicron technology, from 130nm on, poses a new set of design problems. We can now implement tens of millions of gates on a reasonably small die, leading to a power density and total power dissipation that is at the limits of what packaging, cooling, and other infrastructure can support. As technology has shrunk to 90nm and below, the leakage current is increasing dramatically, to the point where, in some 65nm designs, leakage current is nearly as large as dynamic current. These changes are having a significant effect on how chips are designed. The power density of the highest performance chips has grown to the point where it is no longer possible to increase clock speed as technology shrinks. The voltage variation, threshold variation and performance variation of ICs are expected to be 10%, 40%, and 60% in 2012, respectively.



II. *Existing system*

2.1 Clock tree optimization and clock gating

In normal operation, the clock signal continues to toggle at every clock cycle, whether or not its registers are changing. Clock trees are a large source of dynamic power because they switch at the maximum rate and typically have larger capacitive loads. If data is loaded into registers only infrequently, a significant amount of power is wasted. By shutting off blocks that are not required to be active, clock gating ensures power is not dissipated during the idle time. Clock gating can occur at the leaf level (at the register) or higher up in the clock tree. When clock gating is done at the block level, the entire clock tree for the block can be disabled. The resulting reduction in clock network switching becomes extremely valuable in reducing dynamic power.

2.2- Operand Isolation

Often, data path computation elements are sampled only periodically. This sampling is controlled by an enable signal. When the enable is inactive, the data path inputs can be forced to a constant value. The result is that the data path will not switch, saving dynamic power.

2.3 Multi-Vth

Multi-Vth optimization utilizes gates with different thresholds to optimize for power, timing, and area constraints. Most library vendors provide libraries that have cells with different switching thresholds. A good synthesis tool for low-power applications is able to mix available multi-threshold library cells to meet speed and area constraints with the lowest power dissipation. This complex task optimizes for multiple variables and so is automated in today's synthesis tools.

2.4 MSV

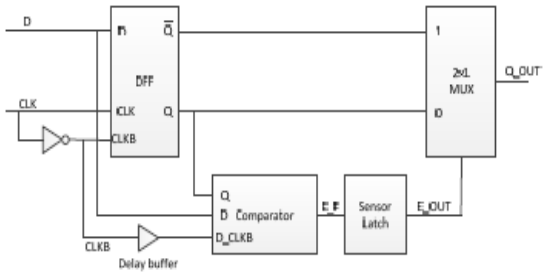
Multi-supply voltage techniques operate different blocks at different voltages. Running at a lower voltage reduces power consumption, but at the expense of speed. Designers use different supply voltages for different parts of the chip based on their performance requirements. MSV implementation is key to reducing power since lowering the voltage has a squared effect on active power consumption.MSV techniques require level shifters on signals that go from one voltage level to another. Without level shifters, signals that cross voltage levels will not be sampled correctly.

2.5 DVS/DVFS/AVFS

Dynamic voltage and frequency scaling (DVFS) techniques—along with associated techniques such as dynamic voltage scaling (DVS) and adaptive voltage and frequency scaling (AVFS)—are very effective in reducing power, since lowering the voltage has a squared effect on active power consumption. DVFS techniques provide ways to reduce power consumption of chips on the fly by scaling down the voltage (and frequency) based on the targeted performance requirements of the application.

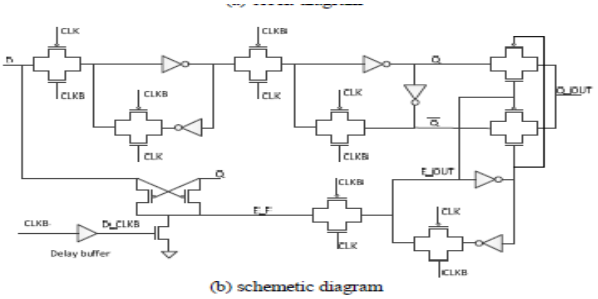
III. *Proposed system*

In this project, we propose a low-power variation-aware FF.Compared to the existing pproaches, the proposed FF does not require longer delayed clock and additional errorcorrection hardware. Also, the error detection and correction window is extended to the half of the clock period.
The block diagram and the schematic of the proposed FF are shown in Fig. 1 (a) and Fig. 1 (b), respectively. The proposed FF consists of the conventional DFF, a sensor latch, a comparator, and a 2x1 multiplexer. The sensor latch is transparent at the positive phase of the clock. As shown in Fig. 2, in the case of timing error of the delayed input signal D, the proposed FF can detect and correct it.



(a) block diagram

The design concept for the proposed FF is to sample the input and the output data of the DFF simultaneously at the positive phase of the clock. The proposed sensor FF eliminates the effect on the intra-die variation on the critical parts of the circuit using timing redundancy concept. Due to the fact that it borrows the timing margin from the hold time of the sequential element, the application system using the proposed FF can use higher target clock frequency with more robustness to PVT variations.



(b) schemetic diagram

Figure 1. Proposed Variation-Aware FF

Due to the fact that it borrows the timing margin from the hold time of the sequential element, the application system using the proposed FF can use higher target clock frequency with more robustness to PVT variations. The comparator detects timing error of the input data by comparing the output data of the FF, which has already been sampled before the setup time of the FF only when the positive phase of the clock is activated.

E_F signal is logical high ('1') in case of an error. By connecting the CLKB signal to the comparator module, the node E_F is deactivated and the pre-charged to logical low ('0') when CLKB is positive phase. It is possible to compare the value of the D with the value of the Q before the hold time of the DFF. In this case, the correct input value can be recognized as an error by the comparator module. In order to solve this problem, the additional small sized delay buffer is inserted between CLKB and D_CLKB to meet the hold time constraint. Compared to the existing FF , the proposed FF requires the small sized buffer, since the intrinsic hold time of the DFF is nearly equal to the propagation delay of a unit sized inverter.

3.1 Braun Multiplier

Braun's multiplier is an n × m bit parallel multiplier and generally known as carry save multiplier and is constructed with m × (n-1) addres and m × n AND gates. The Braun's multiplier has a glitching problem which is due to the ripple carry adder in the last stage of the multiplier.

Mathematical Basis

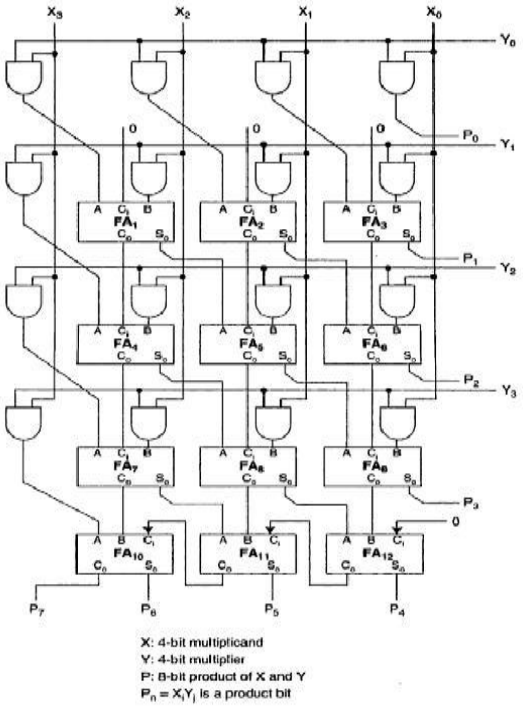
Consider a generic m by n multiplication of two unsigned n – bit number y= $y_{m-1}\ldots y_0$ and x= $x_{n-1}\ldots x_0$

$$Y = \sum_{i=0}^{m-1} Y_i 2^i \quad (1)$$

$$X = \sum_{i=0}^{n-1} X_i 2^i \quad (2)$$

The product P = $P_{2n-1} \ldots P_1 P_0$, which results from multiplying the multiplicand Y by the multiplier X, can be written as follows:

$$P = XY = \sum_{i=0}^{m-1}\sum_{j=0}^{n-1} (X_i Y_j) 2^{i+j} \quad (3)$$



3.2 Propsed Circuit

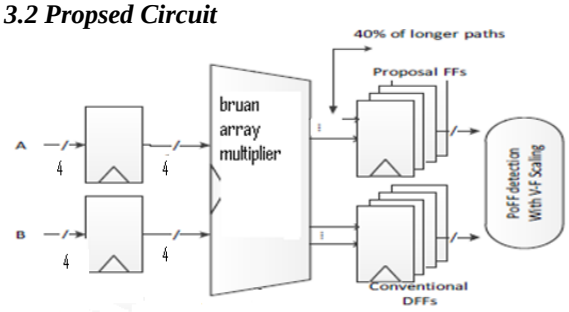
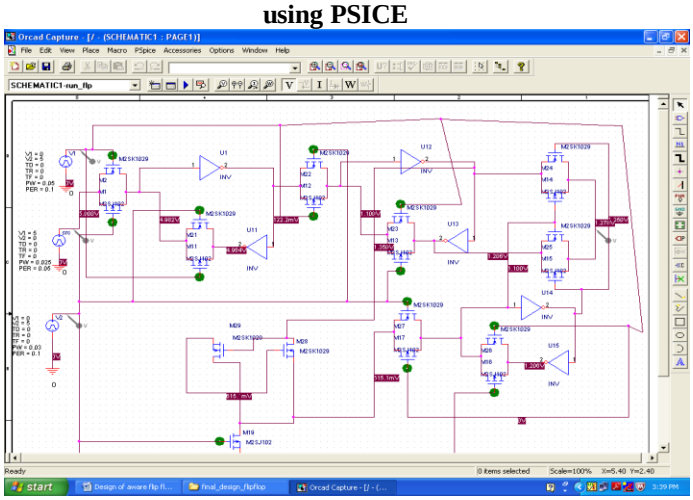


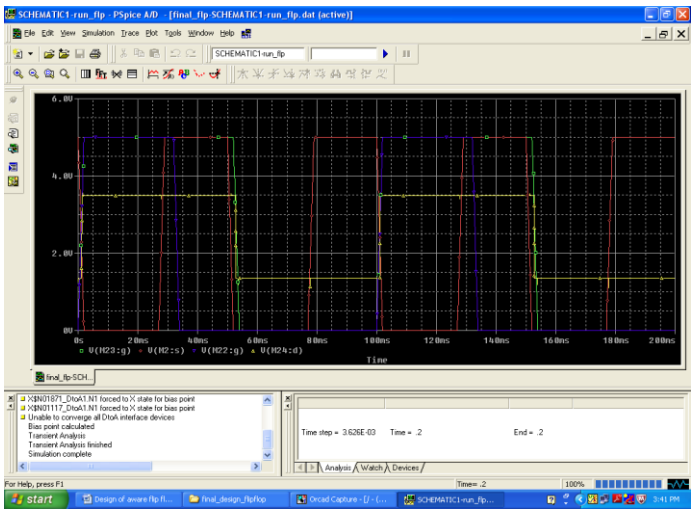
Figure 4. Circuit-under-test

IV. *Simulation Results*

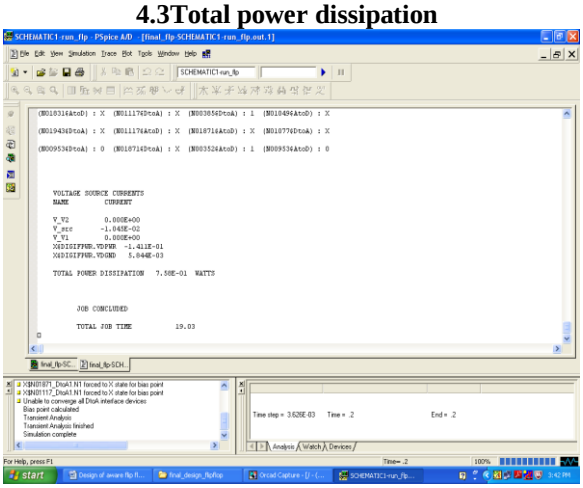
4.1 Implementation of the proposed aware flipflop by using PSICE



4.2 Expected simulation results



4.3Total power dissipation



4.4 PoFF Comparision Results

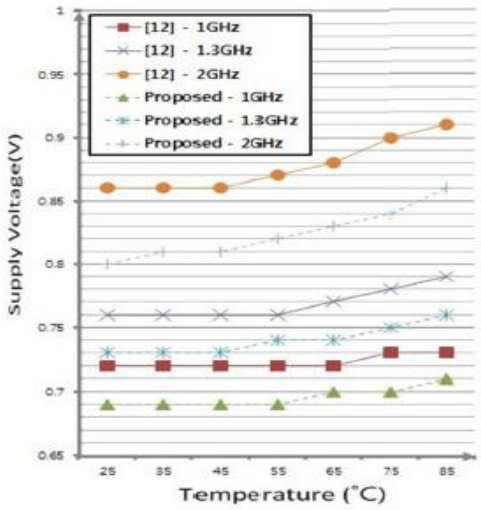


Figure 5. PoFF comparison results

4.5 Average Power Disapption at PoFF Volt

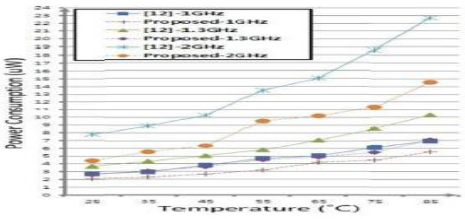
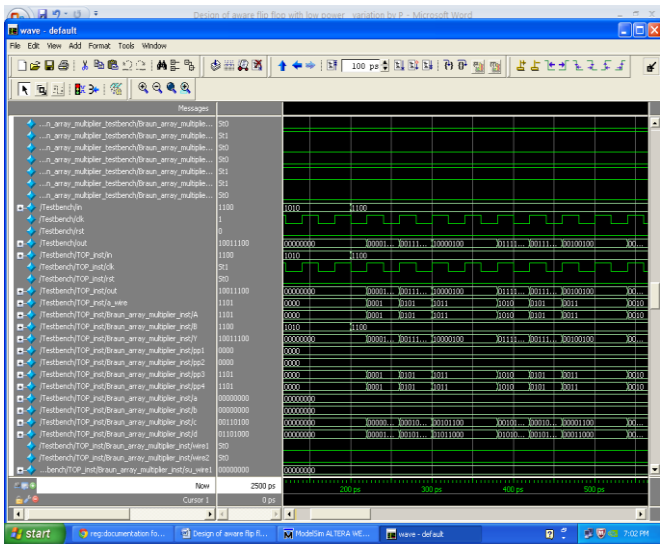


Figure 6. Average power dissipation at PoFF voltages

4.6 Simulation in modelsim as below



V. *Conclusion*

In this paper, we propose an efficient variation-aw are FF for low power circuit designs. Compared to the existing approach, the proposed FF has longer detection window and does not require large hardware over head for generating the delayed clock. PoFFs of the digital circuit s using the proposed FF are lower than those of the digital

circuits using the existing FF, since the proposed FF has longer error detection window. Also, the proposed system consumes less power dissipation with smaller number of transistors. Therefore, the proposed FF can be efficiently applied to low-power digital system technique. Also, the proposed FF design using DVFS be used for DFFV-aware circuit designs.

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