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FPGA Implementation of Motion Human Detection Based On Background Subtraction

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ABSTRACT
In this paper, a video surveillance-based image processing system is developed on Xilinx Spartan3 Field Programmable Gate Array (FPGA) device using embedded development kit (EDK) tools from Xilinx. Two different hardware architectures of two dimensional (2-D) video surveillance have been implemented as a coprocessor in an embedded system. It is direct implementation of video surveillance by Motion human detection algorithm. In addition, the hardware cost of these two architectures is compared for benchmark images.
Keywords– video surveillance, FPGA, EDK, Micro Blaze, FSL Introduction

I. Introduction

Many embedded DSP systems make use of a DSP chip utilizing a single processing core with high-bandwidth memory connections to implement DSP algorithms.In this investigation, we developed an alternative approach based on an embedded FPGA system for image processing. Field Programmable Gate Array (FPGA) is widely used in embedded applications such as automotive, communications, industrial automation, motor control, medical imaging etc. FPGA is chosen due to its reconfigurable ability. Without requiring hardware change-out, the use of FPGA type devices expands the product life by updating data stream files. FPGAs have grown to have the capability to hold an entire system on a single chip meanwhile, it allows in-platform testing and debugging of the system. Furthermore, it offers the opportunity of utilizing hardware/software co-design to develop a high performance system for different applications by incorporating processors (hardware core processor or software core processor), on-chip busses, memory, and hardware accelerators for specific software functions.

In this paper, video surveillance a -based image processing system is developed on a Xilinx Spartan3 Field Programmable Gate Array (FPGA) device using an embedded development kit (EDK) from Xilinx. Video surveillance is one of the most popular transform coding techniques for image and video Segmentation. The video processing and image compression standards such as JPEG, MPEG, and H.26x have adopted as video surveillance the transform coder [1-3]. Consequently, video surveillance is chosen as the application algorithm for the embedded system. This paper is organized as follows: Section II briefly reviews Back Ground Subtraction method. Section III discusses the design flow. Section IV covers different architecture for video surveillance co-processor and compares their performance. Section V is the conclusion part.

II. Moving Object Detection

A. Moving Object Extraction

Mter the background image B(x, y) is obtained, subtract the background image B(x,y) from the current frame Fk (x, y). If the pixel difference is greater than the set threshold T , then determines that the pixels appear in the moving object, otherwise, as the background pixels. The moving object can be detected after threshold operation. Its expression is as follows:

$$D_k(x,y)=\begin{cases}1 & |F_k(x,y)-B_{k-1}(x,y)|>T \\ 0 & others\end{cases} \quad (3)$$

Where Dk (x, y) is the binary image of differential results. T is gray-scale threshold, its size determines the accuracy of object identification. As in the algorithm T is a fixed value, only for an ideal situation, is not suitable for complex environment with lighting changes. Therefore, this paper proposes the dynamic threshold method, we dynamically changes the threshold value according to the lighting changes of the two images obtained. On this basis, add a dynamic threshold !'1T to the above algorithm. Its mathematical expression is as follows:

$$\Delta T=\lambda \bullet \frac{1}{M\times N}\sum_{i=0}^{N-1}\sum_{j=0}^{M-1}|F(i,j)-B(i,j)| \quad (4)$$

Then

$$D_k(x,y)=\begin{cases}1 & |F_k(x,y)-B_{k-1}(x,y)|>T+\Delta T \\ 0 & others\end{cases} \quad (5)$$

Where A is the inhibitory coefficient, set it to a value according to the requirements of practical applications, and the reference values is 2. M x N is the size of each image to deal with. M x N numerical results indicate the number of pixels in detection region. !'1T reflects the overall changes in the environment. If small changes in image illumination, dynamic threshold !'1T takes a very small value. Under the premise of enough pixels in the detection region, !'1T will tend to O. If the image illumination changes significantly, then the dynamic threshold !'1T will increase significantly. This method can effectively suppress the impact of light changes.

B. Reprocessing

As the complexity of the background, the difference image obtained contains the motion region, in addition, also a large number of noise. Therefore, noise needs to be removed. This paper adopts median filter with the 3 X 3 window and filters out some noise.

After the median filter, in addition the motion region, includes not only body parts, but also may include moving cars, flying birds, flowing clouds and swaying trees and other nonbody parts. Morphological methods are used for further processing. Firstly, corrosion operation is taken to effectively filter out non-human activity areas. Secondly, using the expansion operation to filter out most of the non-body motion regions while preserving the shape of human motion without injury. Mter expansion and corrosion operations, some isolated spots of the image and some interference of small pieces are eliminated, and we get more accurate human motion region.

C. Extraction of Moving Human Body

After median filtering and morphological operations, some accurate edge regions will be got, but the region belongs to the moving human body could not be determined. Through observation, we can find out that when moving object appears,shadow will appear in some regions of the scene. The presence of shadow will affect the accurate extraction of the moving object. By analyzing the characteristics of motion detection, we combine the projection operator with the previous methods.

Based on the results of the methods above, adopting the method of combining vertical with horizontal projection to detect the height of the motion region. This can eliminate the impact of the shadow to a certain degree. Then we analyze the vertical projection value and set the threshold value (determined by experience) to remove the pseudo-local maximum value and the pseudo-local minimum value of the vertical projection to determine the number and width of the body in the motion region, we will get the moving human body with precise edge. This article assumes that people in the scene are all in upright-walking state.

The flow chart of moving human body extraction is shown in Fig.1:

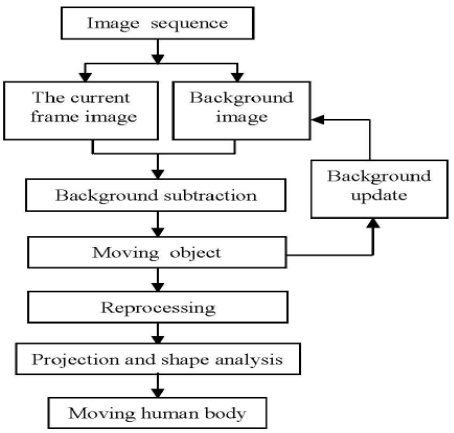

Figure 1. The flow chart of moving human body extraction

Human body detection is to identify the corresponding part of human from the moving region. But the extracted moving region may correspond to different moving objects, such as pedestrians, vehicles and other such birds, floating clouds, the swaying tree and other moving objects. Hence we use the shape features of motion regions to further determine whether the moving object is a human being. Judging criteria are as follows the object area is larger than the set threshold the aspect ratio of the object region should conform to the set ratio. If these two conditions are met, the moving object is the moving human body, or is not a human body.

III. Design Flow

To build an embedded system on Xilinx FPGAs, the embedded development kit (EDK) is used to complete the reconfigurable design. Figure 1 shows the design flow.

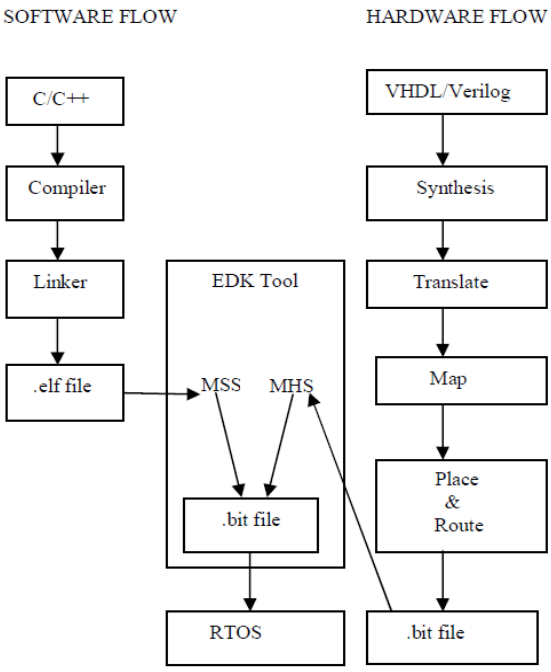

Fig 2 Design flow

Unlike the design flow in the traditional software design using C/C++ language or hardware design using hardware description languages, the EDK enables the integration of both hardware and software components of an embedded system. For the hardware side, the design entry from VHDL/Verilog is first synthesized into a gate-level netlist, and then translated into the primitives, mapped on the specific device resources such as Look-up tables, flip-flops, and block memories. The location and interconnections of these device resources are then placed and routed to meet with the timing Constraints. A downloadable .bit file is created for the whole hardware platform. The software side follows the standard embedded software flow to compile the source codes into an executable and linkable file (ELF) format. Meanwhile, a microprocessor software specification (MSS) file and a microprocessor hardware specification (MHS) file are used to define software structure and hardware connection of the system. The EDK uses these files to control the design flow and eventually merge the system into a single downloadable file. The whole design runs on a real-time operating system (RTOS).

IV. Videosurvelliance Co−Procesor

There are different ways to include processors inside Xilinx FPGA for System-on-a-Chip (SoC): PowerPC hard processor core, or Xilinx MicroBlaze soft processor core, or user-defined soft processor core in VHDL/Verilog. In this work, The 32-bit MicroBlaze processor is chosen because of the flexibility. The user can tailor the processor with or without advance features, based on the budget of hardware. The advance features include memory management unit, floating processing unit, hardware multiplier, hardware divider, instruction and data cache links etc. The architecture overview of the system is shown in Figure 2. It can be seen that there are two different buses (i.e., processor local bus (PLB) and fast simplex link (FSLbus) used in the system [5-6]. PLB follows IBM core connect bus architecture, which supports high bandwidth master and slave devices, provides up to 128- bit data bus, up to 64-bit address bus and centralized bus Arbitration. It is a type of shared bus. Besides the access overhead, PLB potentially has the risk of hardware/software incoherent due to bus arbitration. On the other hand, FSL supports point-to-point unidirectional communication. A pair of FSL buses (from processor to peripheral and from peripheral to processor) can form a dedicated high speed bus without arbitration mechanism. Xilinx provides C and assembly language support for easy access. Therefore, most of peripherals are connected to the processor through PLB; the DWT coprocessor is connected through FSL instead.

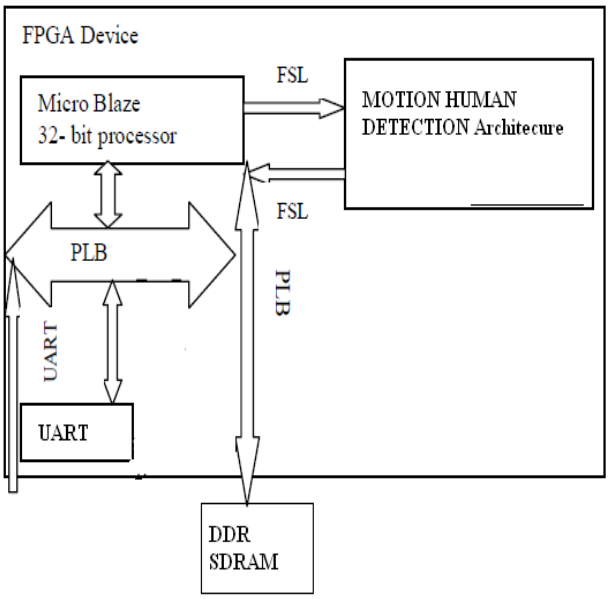

Fig 3 System Overview

The current system offers several methods for distributing the data. These methods are a UART, and VGA, and Ethernet controllers. The UART is used for providing an interface to a host computer, allowing user interaction with the system and facilitating data transfer. The VGA core produces a standalone real-time display. The Ethernet connection allows a convenient way to export the data for use and analysis on other systems. In our work, to validate the DWT coprocessor, an image data stream is formed using VISUAL BASIC, then transmitted from the host computer to FPGA board through UART port.

V. Experimental Results

Experiments are performed on gray level images to verify the proposed method. These images are represented by 8 bits/pixel and size is 128 x 128. Image used for experiments are shown in below figure.

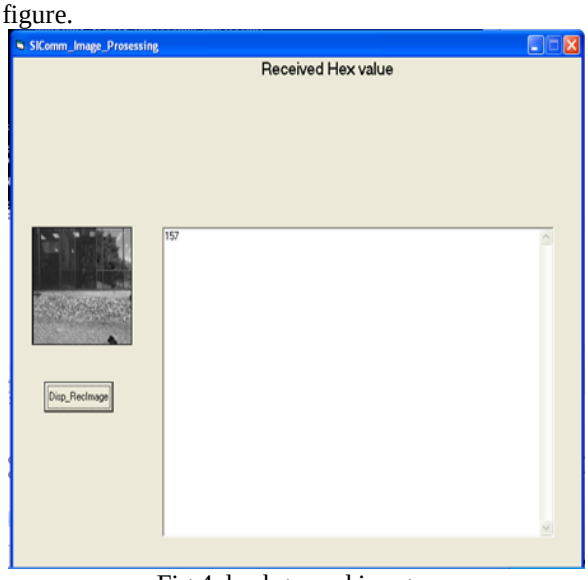

Fig 4 background images

The measurands used for proposed method are as follows:

The entropy (E) is defined as Where s is the set of processed coefficients and p (e) is the probability of processed coefficients. By using entropy, number of bits required for compressed image is calculated. An often used global objective quality measure is the mean square error (MSE) defined as:

Where, nxm is the number of total pixels. f (i,j) and f(i,j)' are the pixel values in the original and reconstructed image. The peak to peak signal to noise ratio (PSNR in dB) [11-13] is calculated as

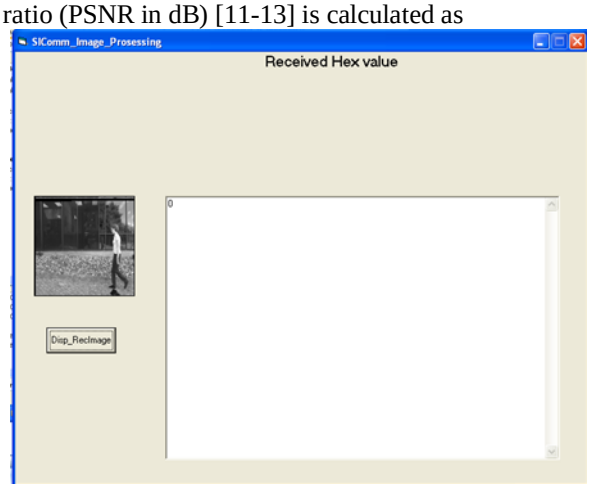

Fig 5 current image

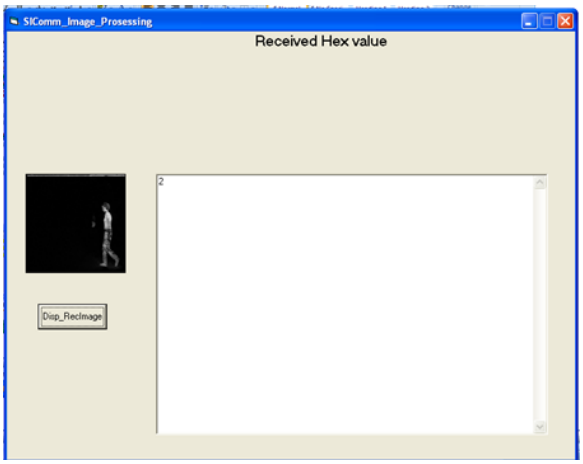

Fig 6 output image And the synthesis report is below

```
Selected Device : 3s500efg320-4

 Number of Slices:                  2649  out of   4656   56%
 Number of Slice Flip Flops:        3343  out of   9312   35%
 Number of 4 input LUTs:            3794  out of   9312   40%
    Number used as logic:           3118
    Number used as Shift registers:  356
    Number used as RAMs:             320
 Number of IOs:                       83
 Number of bonded IOBs:               40  out of    232   17%
    IOB Flip Flops:                   55
 Number of BRAMs:                      7  out of     20   35%
 Number of MULT18X18SIOs:              3  out of     20   15%
 Number of GCLKs:                      7  out of     24   29%
 Number of DCMs:                       2  out of      4   50%

Timing Summary:
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Speed Grade: -4

   Minimum period: 12.384ns (Maximum Frequency: 80.749MHz)
   Minimum input arrival time before clock: 41.553ns
   Maximum output required time after clock: 13.840ns
   Maximum combinational path delay: 3.344ns
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Fig. 7 Synthesis report

VI. Conclusions

In this paper, a Background Subtraction-based reconfigurable system is designed using the EDK tool. Hardware architectures of Motion human detection algorithm have been implemented as a coprocessor in an embedded system. the hardware cost of these architecture is compared for benchmark images. This type of work using EDK can be extended to other applications of embedded system. These two architectures applications compared for benchmark images. This type of work using EDK can be extended to other applications of embedded systems.

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