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An Analytical Delay Expression For Deep Sub-Micron RLC Interconnect

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ABSTRACT
Continuously scaling down devices is the main goal in very deep sub-micron (VDSM) technology. Though using VDSM technology we are achieving many advantages. But circuit performances are badly affected because of secondary effects like crosstalk noise. According to International Technical Roadmap for Semiconductors(ITRS) 2011 report today's DSM technology outsmarted Moore's law to work in a new industrial trend called "More than Moore" (MtM). To accomplish this, it is necessary to analyze the timing behavior of the interconnect. Various techniques have been proposed for the delay analysis of global interconnects. Those techniques are based on either simulation techniques or analytical formulae. Simulation tools such as SPICE give the most accurate result for verifying timing issues. In our model aggressor and victim lines are represented using a distributed network which is used to derive a closed form on chip analytical model for RLC global interconnects. Then the model is used to get a simplified expression for delay. Results of proposed model are then compared with the results of BSim4 120nm technology which shows very marginal error with faster simulation time.

Keywords **–** Crosstalk, Coupling, Delay, Interconnect, VLSI

I. INTRODUCTION

An electronic system consists of 2 parts: the basic components(transistor, diode, passive circuit elements, MEMS etc.) and the highly complex interconnect fabric linking them(from local to global in a hierarchical manner). As global interconnects are responsible for power supply, so any disturbance in global interconnect can effect a lot to signal propagation along it and the victim (idle) interconnect. Circuit integration densities rise with each very deep sub-micron (VDSM) due to smaller devices and larger dies. By using VDSM technology we are achieving many advantages. But the classical RC modelling is not enough for global interconnection at high frequencies and low power technology. Working in VDSM technology we cannot ignore wire resistances, capacitances and inductances. So to handle this twofold nature of VDSM technology here in our proposed model we focus on global interconnects where we consider wire resistances, capacitances and inductances. Various techniques have been proposed for the delay analysis of global interconnects. Those techniques are based either on simulation techniques or analytical formulae. Simulation tools such as SPICE give the most accurate result for verifying timing issues. The crosstalk effects because of capacitive coupling and inductive coupling are considered on different nodes of global interconnects. Then using derived expression delay is calculated and compared with BSim4 120nm technology.

II. PROPOSED MODEL

In this section we derived the expression for delay and bandwidth for following interconnects coupling circuit.

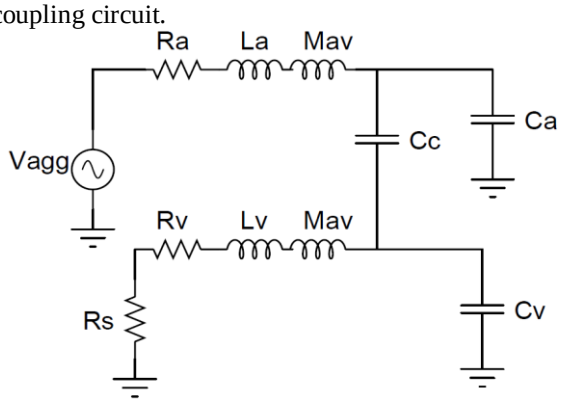

Figure 1: Proposed Model

In above figure upper line is the aggressor line and below is the victim line. Both the lines are connected by coupling capacitance C_c. This coupling capacitance is the result of electromagnetic crosstalk effect of aggressor line on idle(victim) line.

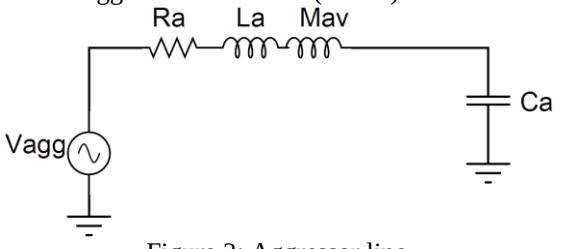

Figure 2: Aggressor line

Above figure shows parameters of aggressor line.V_{agg} is the signal voltage to aggressor line where R_a, L_a , C_a and M_{av} are aggressor line resistance, inductance, capacitances and mutual inductance respectively.

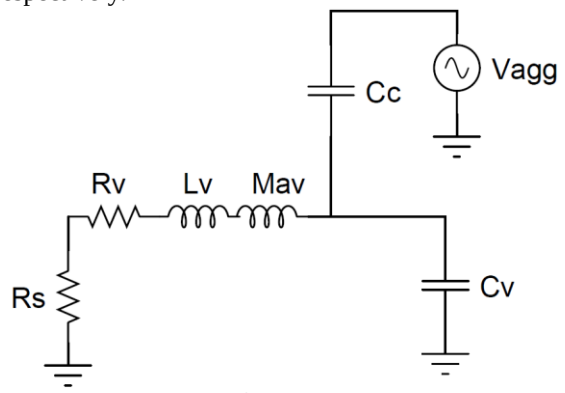

Figure 3: Victim Line

Above figure represents coupling voltage $V_{agg}(S)$ because of crosstalk noise of aggressor line.

Similarly R_v, L_v, C_v and M_{av} are victim line resistance, inductance, capacitances and mutual inductance respectively. In figure 2 and 3 aggressor and victim line are represented individually. Then these models are used for deriving analytical expression for delay.

Delay Calculation

Here we have taken figure 3 as this line produces an unexpected output because of the coupling voltage V_{agg}. Now figure 3 can be simplified as shown below.

$$V_{agg}(t)=\begin{cases}\frac{t}{\tau_a}V_{dd} & 0<t<\tau_a\\ V_{dd} & t>\tau_a\end{cases} \quad (1)$$

It can be represented in S-domain as

$$V_{agg}(s)=\frac{1}{s^2\tau_a}V_{dd}$$

(2)

Here for easily deriving the expressions in final expression we have taken V_{dd}=1.

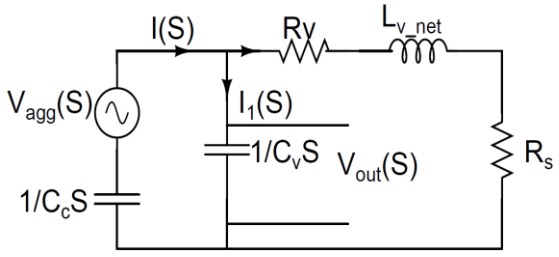

Figure 4: Victim Line equivalent circuit

Proposed model is based on the above circuit. Figure represents victim line parameters and $V_{out}(S)$ is the noise voltage because of crosstalk.

Now applying KVL to first loop

$$\frac{I(S)}{C_cS}+V_{agg}(S)-I_1(S)\frac{1}{C_vS}=0$$

$$\frac{I(S)}{C_cS}+V_{agg}(S)=\frac{I_1(S)}{C_vS}$$

$$I(S)=(\frac{I_1(S)}{C_vS}-V_{agg})C_cS$$

(3)

In practice net inductance of an interconnect considering loop inductance and wire inductance Net inductance implies closely spaced wires do not reduce their net inductance as expected

$$L_{pnet}=\frac{L_{p1}+L_{p2}-M_p{}^2}{L_{p1}+L_{p2}-2M_p}$$

If $L_{p1}=L_{p2}=L_p$

$$L_{pnet}=\frac{L_p+M_p}{2}$$

Net inductance implies closely spaced wires don't reduce their net inductance.

Now applying KVL to second loop

$$\frac{I_1(S)}{C_vS}-\{I(S)-I_1(S)\}[R_v+(\frac{L_p+M_p}{2})S+R_s]=0$$

$$V_{out}(S)=\left[\frac{-V_{agg}C_cS}{\frac{2}{C_vS\left[2R_v+(L_p+M_p)S\right]}+1-\frac{C_c}{C_v}}\right]*\frac{1}{C_vS}$$

$$I_1(S)\left[\frac{1}{C_vS}+R_v+(\frac{L_p+M_p}{2})S+R_s\right]=I(S)\left[R_v+(\frac{L_p+M_p}{2})S+R_s\right]$$

$$I_1(S)=\frac{I(S)\left[R_v+(\frac{L_p+M_p}{2})S+R_s\right]}{\left[\frac{1}{C_vS}+R_v+(\frac{L_p+M_p}{2})S+R_s\right]}$$

(4)

Using (3) in (4)

$$I_1(S)=\frac{\left[\left(\frac{I_1(S)}{C_vS}-V_{agg}\right)C_cS\right]\left[R_v+(\frac{L_p+M_p}{2})S+R_s\right]}{\left[\frac{1}{C_vS}+R_v+(\frac{L_p+M_p}{2})S+R_s\right]}$$

(5)

Now solving above equation

$$I_1(S)=\frac{-V_{agg}C_cS}{\frac{2}{C_vS\left[2R_v+(L_p+M_p)S+2R_s\right]}+1-\frac{C_c}{C_v}}$$

If $R_s=0$

$$I_1(S) = \frac{-V_{agg} C_c S}{\frac{2}{C_v S\left[2R_v + (L_p + M_p)S + \right]} + 1 - \frac{C_c}{C_v}}$$

So

$$V_{out} = I_1(S) * \frac{1}{C_v S} \quad (6)$$

$$V_{out}(S) = \left[\frac{-V_{agg} C_c S}{\frac{2}{C_v S\left[2R_v + (L_p + M_p)S\right]} + 1 - \frac{C_c}{C_v}} \right] * \frac{1}{C_v S} \quad (7)$$

For calculation of delay we consider 50% rise time when $V_{out}(t)=0.5V_{dd}$

Now for delay calculation equating $V_{out}(t)=0.5V_{dd}$

$$V_{out}(S) = \frac{0.5V_{dd}}{S}$$

Using above value in (7)

$$\frac{0.5V_{dd}}{S} = \left[\frac{\frac{-V_{dd}}{S^2 t_{50\%}} C_c S}{\frac{2}{C_v S\left[2R_v + (L_p + M_p)S\right]} + 1 - \frac{C_c}{C_v}} \right] * \frac{1}{C_v S}$$

Solving above equation and taking inverse Laplace transform

$$t_{50\%} = 2 * \left[\frac{C_C R_v}{2 + C_v X - C_c X} \right]$$

Where

$$X = 2R_v + (L_p + M_p)$$

Analytically M_p can be found out by using[5]

$$M_p = 2 * 10^{-7} \left[\ln\left(\frac{l}{s} + \sqrt{\left(\frac{l}{s}\right)^2 + 1} \right) - \sqrt{1 + \left(\frac{s}{l}\right)^2} + \frac{s}{l} \right]$$

III. SIMULATION RESULT AND DISCUSSION

The configuration of circuit for simulation is shown in Figure 1. The high-speed interconnect system consist of two coupled interconnect lines and ground and the length of the lines is d=100 um with a separation of 'S'. The extracted values for the parameters R, L, and C are given in Table I.

Table I:RLC Parameters for a Minimum-Sized Wires in a 0.12um Technology

Parameter(s)	Value/100um
Resistance(R_v)	287Ω
Inductance(L_v)	0.07 nH
Coupling Capacitance(Cc)	0.279fF
Capacitance(C_v)	3.95fF/m
Wire Separation(S)	0.6um

Table-II compares the delay we got using derived expression with SPICE simulator values and the average percentage of error is about 0.0540%.

Table II: Delay comparison of Proposed model with SPICE model

R_s(Ω)	L_v(nH)	C_c(fF)	SPICE Delay(ps)	Proposed Model(ps)	% Error
50	0.07	0.279	20.54	20.25	0.0141
100	0.07	0.279	42.85	41.45	0.0325
450	0.07	0.279	229.47	214.66	0.0645
1000	0.07	0.279	480.13	429.63	0.1051

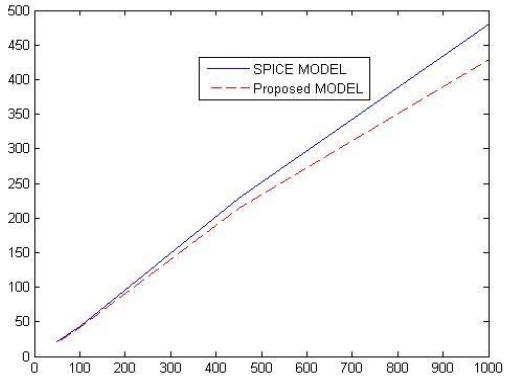

Figure 5: Deviation from SPICE Model

Above figure shows the deviation of proposed model from SPICE model.

IV. CONCLUSION

In this study simple and explicit analytical expressions have been proposed for calculating delay for global interconnects in very deep sub-micron (VDSM) technology. It is expected that these expressions will also applicable to 90nm and 45nm technology. These expressions are expected to be used efficiently in high speed and large scale circuits. In future we will try to simplify these equations to more simple form as possible with more non-linear parameters.

V. ACKNOWLEDGEMENTS

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