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Design Of Low Power Cmos High Performance True Single Phase Clock Dual Modulus Prescaler

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ABSTRACT
Dual-modulus prescaler is a critical block in power conscious PLL design. By modifying the second branch in the TSPC DFF, two TSPC DFFs can be cascaded directly to provide multiple division ratios. Domino Logic D-flip-flop is used to improve operating speed of true single-phase clock (TSPC), which results Charge sharing, Glitches and Critical path Delay due to the logic gates for mode selection. In this work True Single Phase Clock (TSPC) based on Ratioed logic D flip-flop and Transmission Gates (TGs) is implemented in 0.18μm CMOS process. A Glitch elimination TSPC D-flip flop is used in the synchronous counter. TGs are used in the critical path and the control logic for mode selection. The power efficient TSPC design technique is applied to 3/4 and 15/16 prescalers, and their performances are compared with previous work.The power efficient dual modulus 3/4 and 15/16 prescalers are designed using Eldo Simulation tool in Mentor Graphics and its performance are compared. Simulation and measurement results show high-speed, low-power, low PDP and multiple division ratio capabilities of the power efficient technique with a frequency range of 0.5-3.125GHz. The improved speed, the power efficiency, and the flexibility will promote its wide deployment in Multi gigahertz range applications.
Keywords -Dual modulus, frequency divider, prescaler, true single-phase clocked (TSPC) logic.

I. INTRODUCTION

The phase locked (PLL) method of frequency synthesis is now the most commonly used method of producing high frequency oscillations in modern communications equipment. There would not be an amateur or commercial transceiver of any worth today that does not employ at least one if not several, Phase locked loop system s, to generate stable high frequency oscillation. PLL circuits are now frequently being used to demodulate FM signals, making obsolete the Foster-seerly and ratio detectors. Other applications for PLL circuits include AM demodulator, FSK decoders, Two-tone decoders and motor speed controls. High-speed dual-modulus frequency prescalers play an important role in a phase-locked loop(PLL) design. They allow multiple division ratios using a single divider. Power consumption, speed, and the number of available division ratios are the main design criteria for frequency prescalers. Several topologies are available for frequency prescalers in the GHz range, including current-mode logic (CML) [1]–[3], true single-phase clocked (TSPC) logic [6], [7], and extended TSPC (ETSPC) logic [4], [5. From this TSPC prescaler is a preferred choice when it satisfies the speed requirement with low power consumption. There are two basic dual-modulus TSPC prescalers: ÷2/3 and ÷3/4, as shown in Fig. 1

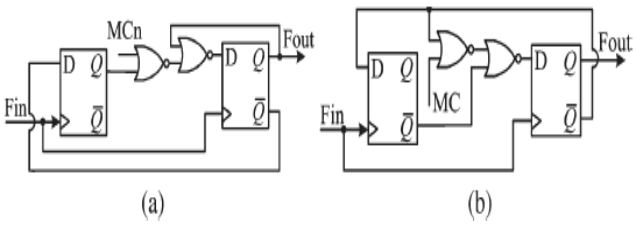


Fig.1. Block diagram of (a) the ÷2/3 frequency (b) ÷3/4 frequency prescalers

Due to incorporation of logic Gates between two D flip-flops (DFFs), speed of dual-modulus prescalers is usually much slower than that of a ÷2 divider consisting of a TSPC DFF [8]. The optimization of the D flip-flop in the synchronous stage is essential to increase the operating frequency and reduce the power consumption. One of the common techniques to improve speed is combining logic gates with DFFs, such as the one demonstrated in [7]. As shown in Fig. 2 A DMP usually comprises asynchronous dual-modulus counter and an asynchronous counter. The critical path delay and the speed of the D-type flip-flop (DFF) in the synchronous counter limit its speed particularly at high moduli. This type of topology stacks four transistors in the first branch of a DFF to incorporate a logic function limiting the improvement in speed.

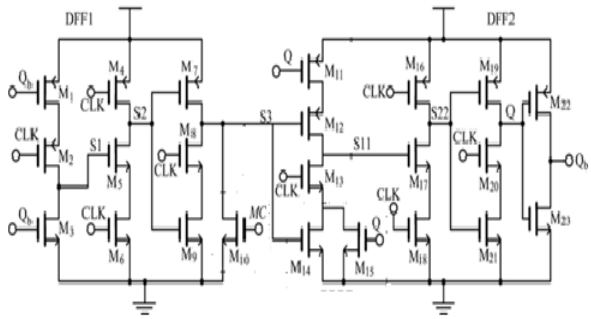


Fig.2. TSPC ÷2/3 frequency prescaler combining the NOR gates into the DFFs

We also note that the ÷3/4 prescaler is rarely used because the two logic gates shown in Fig. 1(b) cannot be easily separated and combined with DFFs. Lack of a high-speed ÷3/4 prescaler poses limitations in supporting multiple division ratios.

In this brief, we present a design technique that improves speed of TSPC prescalers without a power penalty. Based on the proposed technique, the maximum speed of TSPC prescalers can be increased by more than 40% comparing with conventional designs. Moreover, a divide-by-3 prescaler that is able to work almost at the speed of the ÷2 divider consisting of a TSPC DFF can be realized. Section 2 discusses design and analysis. Section 3 shows simulation and measurement results, followed by the conclusions in Section 4.

II. ANALYSIS OF TSPC PRESCALERS

A high-speed TSPC DFF proposed in [6] is shown in Fig. 3, Functions of the three branches in a TSPC DFF can be summarized as follows. The first branch samples input data during a negative cycle of a clock signal and holds the data during a positive cycle, the second branch precharges a node T during the negative clock cycle and evaluates the data during the positive cycle, and the third one passes the evaluated data during the positive cycle and holds the output during the negative cycle. Therefore, the evaluation result in the second branch decides the output of the DFF, since the second branch works as domino logic. Adding a transistor to the node T creates a NOR logic gate that can change the output value without passing through the first branch. We exploit this behaviour to design high-speed dual-modulus prescalers.

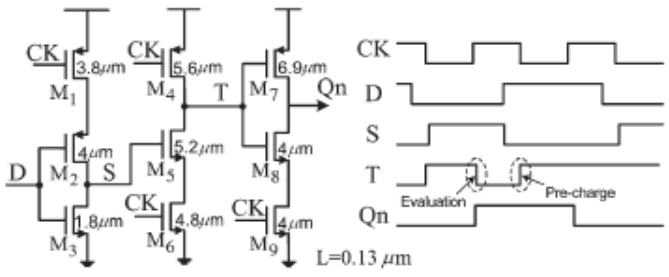
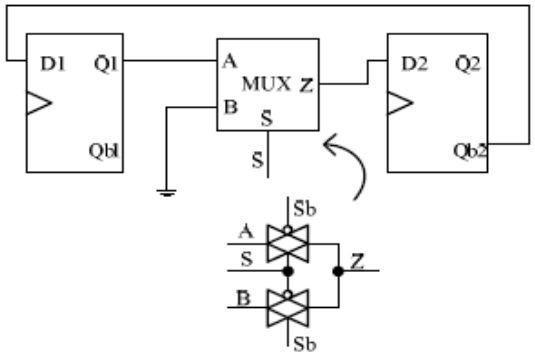
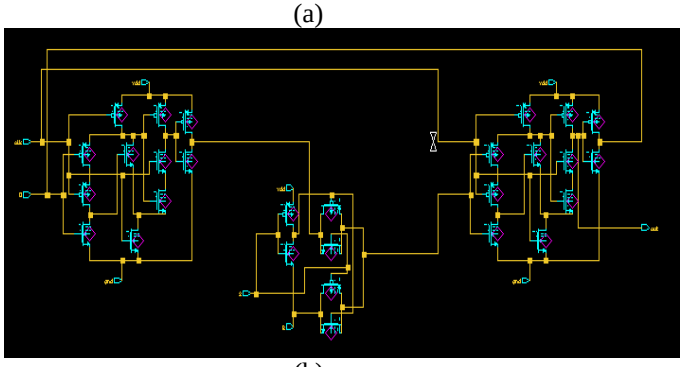


Fig.3. Schematic and waveforms of the TSPC DFF



(a)



(b)

Figure 4. Proposed high speed ÷3/4 frequency prescaler (a) schematic (b) Implementation of the prescaler when divide by 3

Power Efficient 3/4 DMP is shown in Fig.4. A ÷3/4 prescaler has some modifications, which extends the output by one cycle in every two cycles, the ÷3/4 prescaler removes one cycle in every four cycles by comparing the outputs of the two DFFs. To improve speed and Reduce power consumption; we remove separated logic gates by creating a feed through path every three cycles.

Minimization of the delay in the critical path is another important factor in the design of high-speed DMP. The critical path delay is primarily due to the delay of logic gates used for mode selection. The transmission gate (TG) is implemented using two CMOS which can be used to form logic gates for mode selection. Fig.4 shows a circuit for divide-by-3/4 counter which use TGs as logic gate and Control logic for mode selection. It has a higher speed by eliminating the NOR-gate introduced critical path delay, as well as lower power consumption by minimizing the number of full-speed DFF's in the 1st stage. The MUX shown in Fig.4 is a two-input path selector, logically, the output of the circuit can be written as

$$Z = AS + BS$$

When the selector signal S is high, A is passed to the output while a on S passes B to the output. Table I represents its states of transition during the mode of division by 4 and 3 respectively. The circuit operation can be illustrated as follow: When mode control signal is put in divide by 4 modes, S is high; A is passed to the output. This allows Q2=D2=Q1 and circuit operates in divide-by-4 mode.

Q1Q2 cycles through 00 to 10 to 11 to 01 to 00 and so on. Whereas, when mode control is in divide by3 mode, S is low, B is passed to the output. This resets Q2=D2=0 resulting in the divide-by-3 mode operation of the circuit. Q1Q2 skip state 01, changing directly from 11 to 00.

To show the speed improvement in the proposed ÷3/4 prescaler, we compare the critical paths of the conventional designs and the proposed one. The critical path delay can be calculated and compared by referencing the gate delay to a basic inverter. Assuming that the basic inverter with a PMOS width of 4 μm and an NMOS width of 1.8 μm has an intrinsic delay and logical effort of 1 and all transistors have the minimum gate length, the path delay can be calculated from the following equation:

$$T_p = T_{p0}\sum_{j=1}^{N}(R_j + G_j F_j)$$

Where *Tp*, *Tp*0, *Rj*, *Gj*, and *Fj* are the total delay on the critical path, the delay of a basic inverter, the ratio of the intrinsic delays of the logic gate, the logical effort, and the electrical effort.

The critical paths in the proposed divider and the conventional one with two NOR gates, including the intrinsic delays and logical efforts of each gates. The path delays of the proposed divider and the conventional one are 11 × *Tp*0 and 14.4 × *Tp*0, respectively. The path delay calculation clearly shows that the proposed design is faster.

2.1 Power Efficient 15/16 Prescaler

Power Efficient 15/16 DMP is shown in Fig.5. It is comprised of a synchronous dual modulus divide-by-3/4 counter as described above and an asynchronous divide-by- 8 counters. The control logic also uses TGs for simplicity and reducing power consumption.

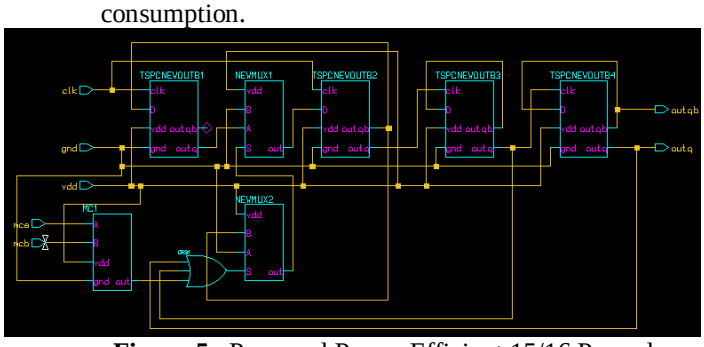


Figure 5 Proposed Power Efficient 15/16 Prescaler

The on-resistance of the transmission gate can be made small by proper sizing. So the extra delay introduced in the critical signal path is much smaller than that of the NOR gates in the conventional DMP. The TGs are used to form OR gate shown in Fig.5. Consider the case when A and B is low, M1 is off, and TGs is on. Since the input B is low, a low is passed to the output. If A is high, M1 is on and A is passed to the output. If B is high and A is low, B is passed to the output through the TGs. If both A and B are high, the TGs are off and M1 is on passing A, a high, to the output.

Table 1 represents its states of transition during the mode of division by 15 and 16 respectively. Logical analysis of circuit shows that the relation between select signals S, Qb2 and mode can be expressed as:

$$S = Qb2 + Q3 + Q4 + mode$$

TABLE 1 State Table for Divide-By- 15/16 Prescaler

S	Mode	Present State Q1Q2Q3Q4	Next State Q1'Q2'Q3'Q4'	Divider
1	1/0	0000	1000	Mode=1 S=1 Divider_by_16
1	1/0	1000	1111	
1	1/0	1111	0111	
1	1/0	0111	0011	
1	1/0	0011	1011	
1	1/0	1011	1101	
1	1/0	1101	0101	
1	1/0	0101	0001	
1	1/0	0001	1001	
1	1/0	1001	1110	
1	1/0	1110	0110	
1	1/0	0110	0010	
1	1/0	0010	1010	Mode=0 S=0 Divider_by_15
1	1/0	1010	1100	
1/0	1/0	1100	0100/0000	
1	1	0100	0000	

Unlike conventional DMP, rather than using static CMOS logic gates, TGs are used to realize the relation S,Qb2 and mode in the proposed design. It minimized the delay involved in the critical path.This analysis shows that TSPC architectures are more suitable for ultra low power applications since they have lower short circuit power, while their switching power and propagation delay can be reduced with different techniques.

III. SIMULATION AND MEASUREMENT

We analyze and compare the conventional and proposed prescalers designed in a 180-nm CMOS technology using The Eldo simulation Tool in Mentor Graphics is used to obtain the simulated output for low power true single phase clock (TSPC) 3/4 and 15/16 prescaler. All of the designs use the TSPC cell shown in Fig. 3.

A single-TSPC divider is included as a reference because it defines the maximum speed and the lowest power a dual modulus prescaler can reach. The power comparison uses the same assumptions, except that for those prescalers that consume different powers in two different modes, we use the average power consumption of the two modes. The power

consumptions of the isolation inverters are not included. Fig. 8 shows the power consumption versus the operating frequency of the prescalers.

For most of the operating frequencies, the proposed 2/3 and 3/4 prescaler consumes less power. The TSPC flip-flop provides the lowest power consumption with the highest maximum speed, as expected, and the conventional designs show the lowest maximum speed with the highest power consumption. We note that the divide-by-3 prescaler illustrated in Fig. 4(a) has almost the same speed as the TSPC flip-flop, which makes it attractive for a high-speed design.

3.1 Power Analysis

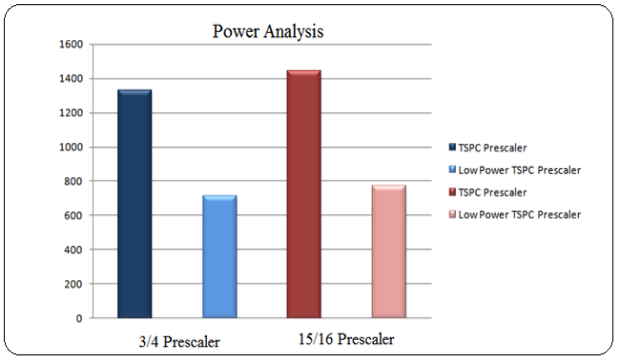


Figure 7 Power Comparison of prescalers

Fig.7 shows that the power dissipation of Low Power TSPC Prescalers and TSPC prescalers. The power dissipation of Low Power TSPC 3/4 and 15/16 Prescalers are 46% and 42% less compared with the conventional TSPC Prescalers respectively

3.2 Delay Analysis

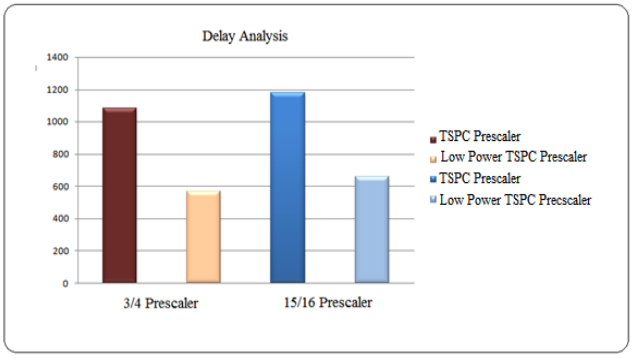


Figure 8 Delay Comparison of Prescaler

Fig.8 Shows that the Delay Parameters of Low Power TSPC Prescalers and TSPC prescalers. The Delay of Low Power TSPC 3/4 and 15/16 Prescalers 47% and 43% less compared with the conventional TSPC Prescalers respectively.

3.3 Simulation Results

The Eldo simulation Tool in Mentor Graphics is used to obtain the simulated output for low power true single phase clock (TSPC) 3/4 and 15/16 prescaler. The simulated waveforms are obtained by assigning the inputs at various levels of extraction and the corresponding outputs are obtained from the assigned inputs. The outputs obtained are complementary with respect to the corresponding complementary inputs. We analyze and compare the proposed prescalers. The simulated waveforms of the proposed work are shown here.

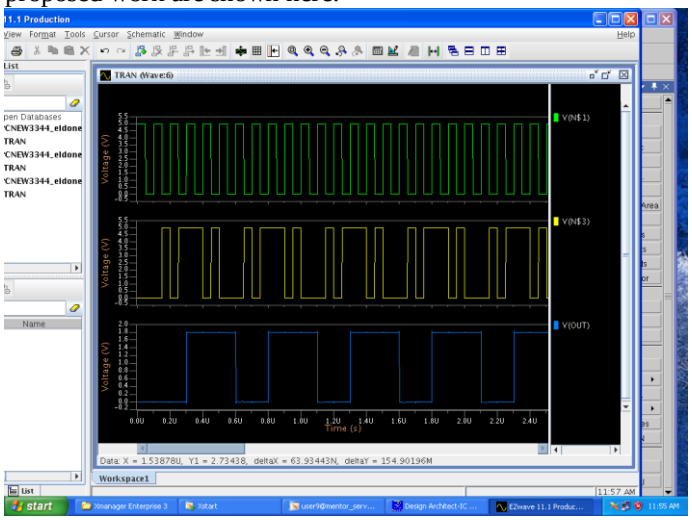


Figure 9 Simulation Output of Low Power TSPC 3/4 Prescaler

Fig.9 shows the output waveform of the proposed 3/4 dual-mode prescaler at 2.5GHz in divide-by-3 and divide-by-4 modes respectively.

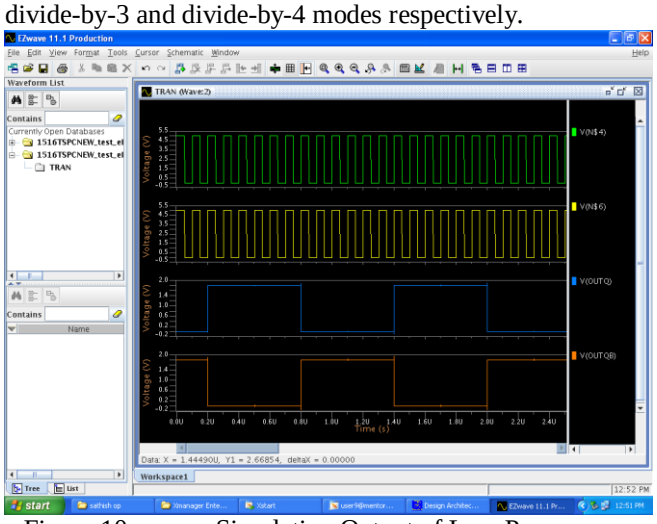


Figure 10 Simulation Output of Low Power TSPC 15/16 Prescaler

The PLL and the VCO are originally intended for an application with maximum frequency of 5 GHz, which is lower than the maximum operating speed of the proposed prescalers. For this reason, the VCO frequency can only be tuned from 3.4 to 5 GHz. The measured waveforms and power consumption values agree well with the simulations results.

Table 2 illustrates Power, Delay and Power Delay Product parameters of True Single Phase Clock (TSPC) Prescalers and Low Power 2/3, 3/4 Dual Modulus prescalers. Table 2 shows that power consumption is reduced compared to conventional

True Single Phase Clock (TSPC) Prescalers. Similarly in Low Power Dual Modulus prescaler delay is very less which results high speed operation in various high frequency Fig. 13 shows the measured output frequencies in the face of different division ratios with input frequencies up to 5 GHz. This proposed technique not only improves flexibility of high-speed frequency divider design with multiple division ratios but also reduces power consumption. Delay and Power Delay Product (PDP) are reduced than their previous work.The improved speed, the power efficiency, and the flexibility will promote its wide deployment in multi gigahertz range applications The DMP is suitable for high-speed, wide-band and low power operation of Wireless Communications.

Table II Comparison between TSPC Dual Modulus Prescaler

PARAMETERS	**TSPC PRESCALER**		**LOW POWER TSPC PRESCALER**	
	3/4 prescaler	15/16 prescaler	3/4 prescaler	15/16 prescaler
Number of sensitivity nodes	14	14	7	12
Delay(ps)	1082.7	1176.6	567.8	656.6
Power(pw)	1328.2	1443.1	714.6	774.5
PDP(aJ)	1.437	1.697	0.405	0.508

IV. CONCLUSION

Dual-modulus prescaler is a critical block in power conscious PLL design. True Single Phase Clock (TSPC) based on Ratioed logic D flip-flop and Transmission Gates (TGs) is implemented and this technique is applied to the 3/4 and 15/16 prescalers. Comparing with conventional designs, the proposed 3/4 and 15/16 prescalers shows a 46% and 42% reduction of power consumption, 47% and 43% speed increment at maximum operating frequency of a single TSPC flip-flop respectively. Delay and Power Delay Product (PDP) are reduced than their previous work.The improved speed, the power efficiency, and the flexibility will promote its wide deployment in multi gigahertz range applications

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