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Efficient VLSI Architecture For1-D Dwtusing 9/7 Filter Based On 2's Complement DBA

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Abstract
A 1-D discrete wavelet transform (DWT) hardware design based on 2's complement design based architecture(DBA) is presented in this paper. We have proposed based on arithmetic for low complexity and efficient implementation of 1-D discrete wavelet transform. The 2's complement design based technique has been applied to reduce the number of full adders. This architecture is suitable for high speed on-line applications, the most important one being image processing. With this architecture the speed of the 1-D discrete wavelet transform is increased. It has 100% hardware utilization efficiency.
***Keywords*:**1-D Discrete Wavelet Transform (DWT), 2's Complement Design Based Architecture (DBA), Xilinx simulation.

I. INTRODUCTION

Wavelets, based on the time-scaling representations provide an alternative to the time-frequency representation in signal processing domain. The shifting (or translation) and the scaling (or dilation) are unique to wavelets. The wavelet is a kind of bases which are generated by dilation and translation of a function [1], [2]. The wavelet analysis method has a good ability at localizing signal in both time and frequency plane[4].Due to the characteristic of flexible TF decomposition, 1-D DWT has also been widely used in many applications, especially in image and video coding, speech and audio coding, speech enhancement, speech recognition, hearing aid and digital commutation [2],[3],[4].

In this paper, in the simplest form, the bit-level multiplication of two number can be performed by shift and add operation. It has been observed that the complexity of a shift-add type signed multiplier is depends on the number of one's of the 2's complement representation of the multiplicand number with the shifted partial sum whereas the zeros will only shift the partial sum. It is assumed that the shifting does not required any hardware as it can be done by hardwiring. The number of one's of the 2's complement number, therefore, will determine the numbers of full adder (FA)required implementing the multiplier.
Several designs have been proposed for the multiplier-less implementation of DWT based on the principle of distributed arithmetic (DA) [1]–[3]. The structure of distributes the bits of the fixed coefficients instead of the bits of input samples. Consequently, the adder-complexity of the structure of depends on the DA-matrix of the fixed coefficients [2].

Chengjun*et al* [8] have approximated the 9/7 filter coefficients and expressed the 9/7 filter outputs in terms of 5/3 filter outputs. By that approach, they have significantly reduced the adder-complexity of the 9/7 DWT. Gourav *et al* [9] have suggested an LUT-less DA-based design for the implementation of 1-D DWT. They have eliminated the ROMcells required by the DA-based structures at the cost of additional adders and multiplexors. The adder-complexity of this structure is significantly higher than the other multiplier-less structures.

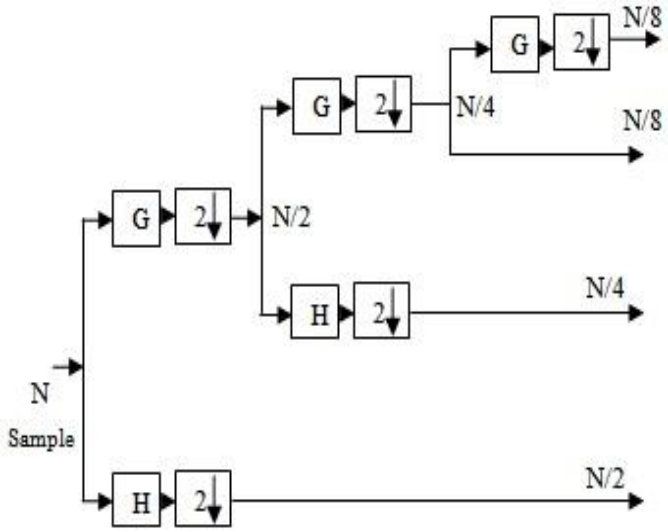
In this paper, we have introduced a new architecture for the 1-D discrete wavelet transform using 2's complement based technique. The algorithm for the tree structure of 1-D discrete wavelet transform is analyzed in the sectionII. The low complexity design for 1-D DWT is analyzed in the section III**.** 2's complement design for 1-D DWT is analyzed in the section IV. Proposed architecture for 2's complement designfor 1-D DWT in the section V. Simulation result and conclusion in the section VI and VII

II. 1-D DISCRETE WAVELET TRANSFORM

The model used in [5] to implement the tree structure of 1-D discrete wavelet packet transform (DWT) is based on the filtering process. Figure1 depicted a complete 3-level 1-DWT. In this figure G and H is the high pass and low pass filter respectively. Computation period is the number of the input cycles for one time produces output samples. In general, the computation period is M= for a j-level 1-D DWT. The period of the 3-level computation is 8. Figure 1, The Sub band Coding Algorithm As an example, suppose that the original signal X[n] has N- sample points, spanning a frequency band of zero to π rad/s. At the first decomposition level, the signal passed through the high pass and low pass filters, followed by subsampling by 2. The output of the high pass filter has N/2- sample points (hence half the time

resolution) but it only spans the frequencies □/2 to □ rad/s (hence double the frequency resolution).

The output of the low-pass filer also has N/2-sample points, but it spans the other half of the frequency band, frequencies from 0 to □/2 rad/s. Again low-pass filter output passed through the same low pass and high passes filters for further decomposition. The output of the second low pass filter followed by subsampling has N/4 samples spanning a frequency band of 0 to □ /4 rad/s. The second high-pass filtered signal constitutes the second level of 2-D DWT coefficients. This signal has half the time resolution, but twice the frequency resolution of the first level signal. This process continues until two samples are left.For this specific example there would be 3 levels of decomposition, each having half **the** number of samples of the previous level.



The 1-D DWT of the original signal is then obtained by concatenating all coefficients starting from the last level of decomposition (remaining two samples, in this case). The DWT will then have the same number of coefficients as the original signal.

III. LOW-COMPLEXITY DESIGNS FOR 1-D DWT

DWPT computation is nothing but two-channel FIR filter computation. Low-pass and high-pass down sampled filter computations are performed on the input to calculate the DWPT coefficients. Low-pass down sampled filter is the average between two samples and high-pass filter is the difference b/w two samples. The DWPT algorithms for 1-level decomposition are given as;

$$Y_{high}[k] = \sum_n h[n] * x[2k-n] \quad (1)$$

$$Y_{low}[k] = \sum_n g[n] * x[2k-n] \quad (2)$$

Where x(n) is the input and $Y_{high}[k]$&$Y_{low}[k]$ are respectively the low-pass and high-pass 1-D DWT coefficients, h[n] and g[n] are respectively, the low-pass and high-pass filter coefficients. We have assumed the 9/7wavelet filter coefficients for multiplier-less design. However, similar type of design can be derived for other type of wavelet filters as well. The 9 low-pass filter and 7 high-pass filter coefficients are taken from [7]. The corresponding high-pass filter coefficients are calculated using the following relation:

$$g(n) = (-1)^k h(N-n) \quad (3)$$

Table1: Filter Coefficients of 9/7 Wavelet Filter.

	Coefficients	Multiplied by 100	8 bit binary representation with 2's complement of negative no.
h0	0.60294901823636	60	00111100
h1	0.26686441184287	26	00011010
h2	-0.07822326652899	-7	00001001
h3	-0.01686411844287	-1	00000011
h4	0.02674875741081	2	00000010
g0	0.5575435262285	55	00110111
g1	-0.29563588155713	-29	00100011
g2	-0.02877176311425	-2	00000110
g3	0.04563588155713	4	00000100

Where, h(n) and g(n) are, respectively, the low and high-pass filter coefficients. N is the filter order. The 8 bit 2'complement representation of the low and high-pass filter coefficient is given in table1. Equation can be rewritten low and high-pass FIR filter as:

$$Y_h[k] = \big(X(n) + X(n-6)\big)g0 + \big(X(n-1)\,X(n-5)\big)\,g1 + \big(X(n-2) + X(n-4)\big)g2 + X(n-3)g3 \quad (4)$$

$$Y_l[k] = \big(X(n) + X(n-8)\big)h0 + \big(X(n-1)\,X(n-7)\big)\,h1 + \big(X(n-2) + X(n-6)\big)h2 + \big(X(n-3) + X(n-5)\big)h3 + X(n-3)h4 \quad (5)$$

IV. 2's COMPLEMENT DESIGNED FOR 1-D DWT

Each of the multiplier unit is replaced with shifters and adders/subtraction for 2's complementimplementation of DWT. The constant multiplication factors of [5] are replaced with shift and adder/subtraction operation and rewritten as

Low pass filter

$$Y_h[k] = [x(n)>>2 + x(n)>>3 + x(n)>>4 + x(n)>>5 + x(n)>>7 + x(n)>>8] + [x(n-1) >> 1 + x(n-1) >> 2 + x(n-1)>> 4 + x(n-1) >> 6 + x(n-1) >> 7] + [x(n-2)>>3 + x(n-2)>>4 + x(n-2)>>5 + x(n-2)>>8] + [x(n-3)>>1 + x(n-3)>>2 + x(n-3)>>4 + x(n-3)>>5 + x(n-3)>>6 + x(n-3)>>7 + x(n-3)>>8] \quad (6)$$

High pass filter

$Y_g[k]$ = [x(n)>>1 + x(n)>>2 + x(n)>>4 + x(n)>>5 + x(n)>>7 + x(n)>>8] + [x(n-1) >> 1 + x(n-1) >> 2 + x(n-1) >> 6 + x(n-1) >> 7 + x(n-1) >> 8] + [x(n-2)>>1 + x(n-2)>>2 + x(n-2)>>4 + x(n-2)>>6 + x(n-2)>>7] + [x(n-3)>>1 + x(n-3)>>6 + x(n-3)>>8] (7)

V. PROPOSED ARCHITECTURE

Figure2 depicted a complete 2's complement design based architecture (DBA). In this paper, the original signal X[n] has N- sample points, is passed through register. The symmetric properties are used in 2's complement design based architecture (DBA), so first and last sample of the register are add and apply the 2's complement design based technique as show as Figure 2. The 2's complement design based technique has been applied to reduce the number of full adders. Full adder consists of two half adder and or gate. Or gate means one or more than one input high then output always high. 2's complement means only shift and adder and this is the multiplier-less technique.

VI. SIMULATION RESULT

We have simulated this architecture in Xilinx 8.2i. The result is shown in Table-2 and Table-3. Table-2 shows the multiplier based DWPT and Table-3 shows the 2's Complement based design. In multiplier based technique the number is slices is more than the 2's Complement based technique but time is increased. The area and power requirement is also reduced. Here the comparison shows first level decomposition to second level decomposition and second level to third level decomposition the number of slices, number of LUTs and flip-flops reduced significantly and time is little bit increased. This is the main advantage of proposed architecture.

Table2: Multiplied based technique

	Number of slices	Number of slice flip flop	Number of 4 input LUTs	Required time($nses$)
First	135	32	225	18.165
Up to Second	371	87	641	23.422
Up to Third	672	172	1084	31.930

Table3: Proposed architecture (2's complement based design)

	Number of slices	Number of slice flip flop	Number of 4 input LUTs	Required time($nsec$)
First	106	21	189	11.563
Up to Second	229	63	414	18.757
Up to Third	389	127	684	25.035

I. CONCLUSION

The main objective of this work was to design a processor specialized for 1-D discrete wavelet transforms that could be used for image processing, such as image compression. In this paper we have used 2's complement design based number system to represent the filter coefficient of the wavelet filter with minimum number of one's consequently; Then we applied the 2's complement design based technique to further reduce the power and area. In this architecture the used of the low and high pass filter. Low pass filter is the average between two sample and high pass filter is the difference between two samples. So minimum 10-15% reduces the power and 10-20 % reduces the area in Multiplier less based design technique (2's complement design based).

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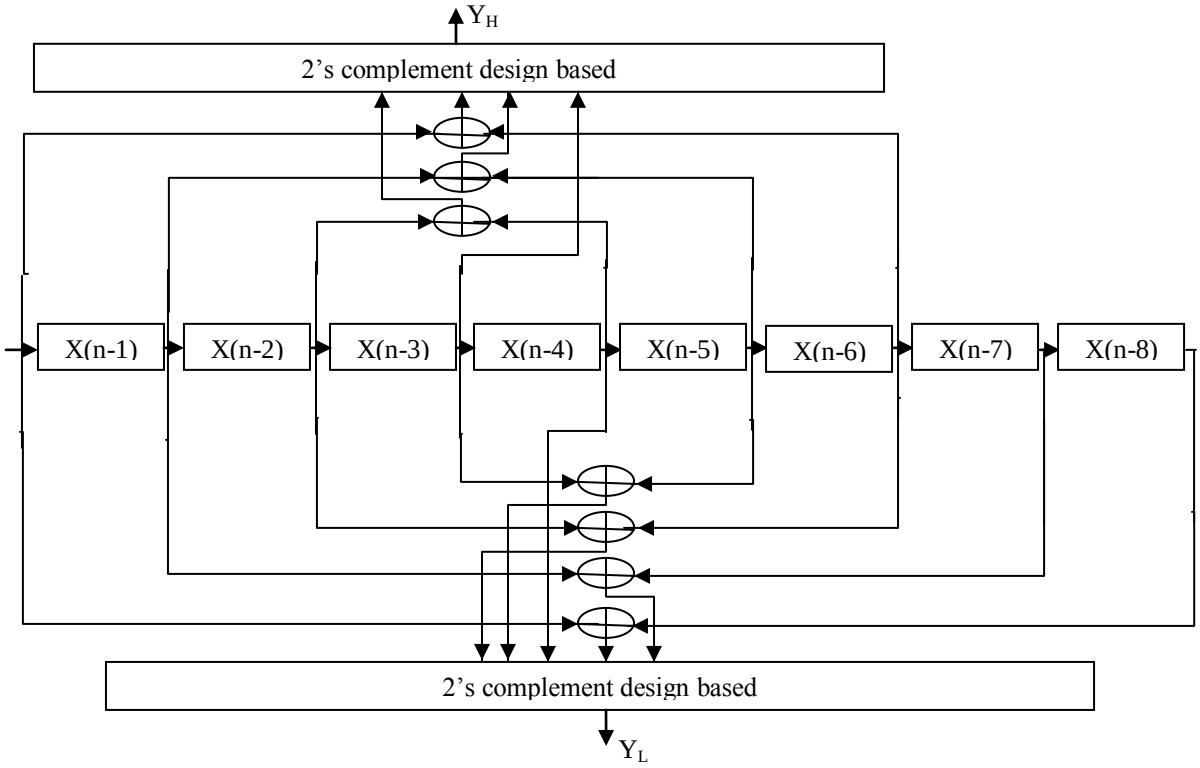

Figure 2: proposed Multiplier-less 9/7 Wavelet filter using 2's complement design based architecture (DBA)