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Analysis of Power Semiconductor Device to Regulate the Load Voltage Using Dynamic Voltage Restorer (Dvr)

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ABSTRACT
This paper deals with simulation and implementation of three level inverter based Dynamic Voltage Restorer (DVR). The control of DVR that injects a voltage in series with a distribution feeder is presented. DVR is a power electronic controller that can protect sensitive loads from disturbances in supply system. DVR can regulate the voltage at the load. The design issues, implementation procedures and system analysis for a fast transient control scheme for three phase capacitor-supported dynamic voltage restorers (DVR) are presented in this paper. The dynamic behaviors of the prototype under different sagged and swelled conditions and depths will be investigated. The dynamic voltage restorer (DVR) is one of the modern devices used in distribution systems to protect consumers against sudden changes in voltage magnitude. The analysis for a fast transient control scheme for three phase capacitor-supported dynamic voltage restorer (DVR) is presented in this paper. This work provides us to find the optimal location and the optimal DVR settings to enhance the distribution related loading issues. Conventional voltage-restoration technique is based on injecting voltage being in-phase with the supply voltage. The injected voltage magnitude will be the minimum, but the energy injected by the DVR is no minimal. In order to minimize the required capacity of the dc source, a minimum energy injection concept is taken into the considerations. It is based on maximizing the active power delivered by the supply mains and the reactive power handled by the DVR during the sag and swell cases. The review model has been built and tested the dynamic behaviors of the model under different sagged and swelled conditions and depths will be investigated. The quality of the load voltage under unbalanced and distorted phase voltages, and nonlinear inductive load is analyzed.

I. INTRODUCTION

1.1 Power Quality

The term "Power Quality" means different things to different people. One definition is the relative frequency and severity of deviations in the incoming power supplied to electrical equipment from the steady 50 Hz, sinusoidal waveform of voltage or current. These deviations may affect the safe or reliable operation of equipment such as computers. Thus terms like "poor power quality" mean that there is ample deviation from norms in the power supply that may cause equipment malfunction or failure. In certain commercial and industrial electrical applications, it is critical that high quality and uninterrupted power be supplied; for fear that significant economic losses can be incurred. Current worst-case estimates of economic losses directly attributable to power quality problems are, in the range of $15 billion to $30 billion per year, which represents only 0.002% to 0.004% of annual U.S output.

Without good power quality, commercial buildings and industrial facilities can suffer from repeated equipment failures, safety hazards, process interruptions and shutdowns. Even two cycles of a 25% voltage dip can cause unprotected microprocessors to malfunction. Electronic controllers on variable speed motors are even more vulnerable to voltage sags than computers. Surges, transients, noise and sags are the different power quality events. It's important to be familiar with the most common and disruptive types of power quality events and their typical solutions.

1.2 Power Quality Events

Power quality phenomena can be divided in to two types, which need to be treated in a different way.

- A characteristic of voltage or current (frequency or power factor) is never exactly equal to its nominal or desired value. The small deviations from the nominal or desired value are called "voltage variations" or "current variations".
- Occasionally the voltage or current deviates significantly from its normal or ideal wave shape. These sudden deviations are called "events".

1.2.1 Interruptions

A "voltage interruption", "supply interruption" or just "interruption" is a condition in which the voltage at the supply terminals is close to zero. Close to zero as defined by the IEC (International Electrotechnical Committee) is "lower than 1% of the declared voltage" and by the IEEE (IEEE Std. 1159:1995) is "lower than 10%".

1.2.2 Under Voltages

Under voltages of various duration are known under different names. Short duration under voltages is called "voltage sags" or "voltage dips". Long duration under voltage is normally simply referred to as "under voltage". According to the IEC, a supply voltage dip is a sudden reduction in the supply voltage to a value between 90% and 1% of the declared voltage, followed by a recovery between 10 ms and 1 minute later. For the IEEE a voltage drop is only a sag if the during sag voltage is between 10% and 90% of the nominal voltage.

1.2.3 Over Voltages

Over voltage events are also given different names based on their duration. Over voltages of very short duration and high magnitude are called "transient over voltages", "voltage spikes", or sometimes "voltage surges". The latter term is rather confusing as it sometimes used to refer to over voltages with in duration about 1 cycle and 1 minute. The latter event is more correctly called "voltage swell". Longer duration over voltages is simply referred to as "over voltages".

1.2.4 Transients

The term transient has long been used in the analysis of power system variations to denote an event that is undesirable but momentary in nature. Broadly speaking transients can be classified in to two categories known as impulsive transients and oscillatory transients.

- **Impulsive transients:** An impulsive transient is a sudden, non-power frequency change in the steady state condition of voltage, current, or both, that is unidirectional in polarity (primarily either positive or negative). Impulsive transients are normally characterized by their rise and decay times, which can also be revealed by their spectral content. For example, a 1.2 x 50-µsec 2000-V impulsive transient nominally rises from zero to its peak value of 2000 V in 1.2µsec, and then decays to half of its peak value in 50µsec.
- **Oscillatory transients:** An oscillatory transient is a sudden, non-power frequency change in the steady state condition of voltage, current, or both, that includes both positive and negative polarity values. An oscillatory transient consists of a voltage or current whose instantaneous value changes polarity rapidly. It is described by its spectral content (predominate frequency), duration, and magnitude.

1.2.5 Voltage unbalance

Voltage unbalance is sometimes defined as the maximum deviation from the average of the three phase voltages or currents, divided by the average of the three phase voltages or currents, expressed in percent. Imbalance can also be defined using symmetrical components. The ratio of either the negative- or zero sequence components to the positive sequence component can be used to specify the percent unbalance.

1.2.6 Waveform distortion

Waveform distortion is defined as a steady state deviation from an ideal sine wave of power frequency principally characterized by the spectral content of the deviation**.** There are five types of waveform distortion. They are DC Offset, Harmonics, Interharmonics , Notching and Noise

- **DC Offset:** The presence of a dc voltage or current in an ac power system is termed DC Offset.
- **Harmonics:** Harmonics are sinusoidal voltages or currents having frequencies that are integer multiples of the frequency at which the supply system is designed to operate. Distorted waveforms can be decomposed into a sum of the fundamental frequency and the harmonics. Harmonic distortion originates in the nonlinear characteristics of devices and loads on the power system.
- **Interharmonics**: Voltages or currents having frequency components that are not integer multiples of the frequency at which the supply system is designed to operate (e.g., 50 Hz or 60 Hz) are called interharmonics. They can appear as discrete frequencies or as a wide-band spectrum.
- **Notching**: Notching is a periodic voltage disturbance caused by the normal operation of power electronics devices when current is commutated from one phase to another. The frequency components associated with notching can be quite high and may not be readily characterized with measurement equipment normally used for harmonic analysis.
- **Noise:** Noise is defined as unwanted electrical signals with broadband spectral content lower than 200 kHz superimposed upon the power system voltage or current in phase conductors, or found on neutral conductors or signal lines.

1.2.7 Power frequency variations

Power Frequency Variations are defined as the deviation of the power system fundamental frequency from it specified nominal value (e.g. 50 Hz or 60 Hz). The power system frequency is directly related to the rotational speed of the generators supplying the system. There are slight variations in frequency as the dynamic balance between load and generation changes. The size of the frequency shift and its duration depends on the load characteristics and the response of the generation control system to load changes. Frequency variations that go outside of accepted limits for normal steady state operation of the power system can be caused by faults on the bulk power transmission system, a large block of load being disconnected, or a large source of generation going off-line.

1.2.8 Voltage fluctuations

Voltage fluctuations are systematic variations of the voltage envelope or a series of random voltage changes, the magnitude of which does not normally exceed the voltage ranges specified by ANSI C84.1 (American National Standard for Electric Power Systems and equipment) of 0.9 pu to 1.1 pu. Loads, which can exhibit continuous, rapid variations in the load current magnitude, can cause voltage variations that are often referred to as flicker. The term flicker is derived from the impact of the voltage fluctuation on lamps such that they are perceived to flicker by the human eye. All the definitions of power quality events are taken from Reference [1]. As the main emphasis is on voltage sags and how they are effecting sensitive equipment, the detailed analysis of voltage sags is discussed in the next chapter.

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5.1 Conclusion

REFERENCES

II. ANALYSIS OF VOLTAGE SAG

A power distribution system is similar to a vast network of rivers. It is important to remove any system faults so that the rest of the power distribution service is not interrupted or damaged. When a fault occurs somewhere in a power distribution system, the voltage is affected throughout the power system. Among various power quality problems, the majority of events are associated with either *voltage sag or a voltage swell*, and they often cause serious power interruptions. A voltage sag condition implies that the voltage on one or more phases drops below the specified tolerance for a short period of time. A voltage swell condition occurs when the voltage of one or more phases rises above the specified tolerance for a short period of time. The causes of voltage sags and swells are associated with faults within the power distribution system. Users located a close distance to the fault experience voltage sags much greater in magnitude and duration than users located farther away, and as the electrical system recovers after removing the fault, voltage swells are produced throughout the system for short periods of time. Often all users who are served by the power distribution system have power interruptions during a fault because of the effects of a voltage sag or voltage swell produced in the system by the fault. The objective of this project is to model different types of custom power devices that can compensate for voltage sag and swell conditions in three-phase power systems.

Power systems supply power for a wide variety of different user applications, and sensitivity to voltage sags and swells varies widely for different applications. Some applications such as automated manufacturing processes are more sensitive to voltage sags and swells than other applications. For sensitive loads, even voltage sag of short duration can cause serious problems in the manufacturing process. Normally, a voltage interruption triggers a protection device, which causes the entire branch of the system to shut down.

2.2 Voltage Sag Definition

A ***Voltage Sag*** as defined by *IEEE Standard 1159-1995*, IEEE Recommended Practice for Monitoring Electric Power Quality, is a decrease in RMS voltage at the power frequency for durations from 0.5 cycles to 1 minute, reported as the remaining voltage. Voltage sags are given a great deal of attention because of the wide usage of voltage-sensitive loads such as adjustable speed drives (ASD), process control equipment, and computers. In case of sensitive loads, even a shallow voltage dip can cause malfunctions and a stoppage of operation, which results in the loss of production.

Three power quality surveys for North America had been done by the National Power Laboratory (NPL), the Canadian Electrical Association (CEA), and the Electric Power Research Institute (EPRI). Table 1.1 shows summary of these three power quality surveys. In each of the three surveys, the definition of a power disturbance event is different. For instance, "voltage sag" is defined as being less than 92% and 90% of nominal voltage for the CEA and the EPRI survey, respectively. In case of "voltage swell", the CEA defines it as the voltage level greater than 104% of nominal voltage, while that of the EPRI is 110%.This shows the voltage sag events defined by 0% to 87% of nominal voltage comprise 68% of power disturbances, in which no filter was applied for NPL data. Where, no filter means that every power disturbance is recorded. In the NPL survey, the voltage

range of 106% to 110% of nominal voltage is considered to be a voltage swell event. If the EPRI definition of voltage swell, greater than 110% of nominal voltage, is applied to the same data, it results in that voltage sags events having 0-87% consists of 93.3% of total event, and voltage sag having 50%-87% of nominal voltage consists of 70% of total disturbances.

In addition, the EPRI survey shows that in most of the cases (92%), the voltage sags have duration of less than 2 seconds and down to 40-50% of nominal voltage. Besides the above three surveys, many papers have reported power quality surveys. The survey reported in shows that 68% of the power disturbances were voltage sags, and these types of disturbances were the only cause of production losses. From power quality surveys, it can be concluded that voltage sags are the most common power disturbances and main cause of power disruption. Therefore, this thesis focuses on voltage sags and their mitigation techniques.

Table 2.1 Summary of the CEA, NPL, and EPRI power quality survey

Survey	period	Number of site	Measure Parameter	Voltage rating
CEA	1991-1994	550	Voltage	120-347
NPL	1990-1995	130	Voltage	—
EPRI	1993-1995	227	Voltage and current	4.16-34.5

2.3 Nature of Voltage Sag

Nature of the sag depends on the cause and load where sag is observed i.e., if the sag is observed at constant impendence load due to a SLG fault as shown in Fig. 2.1, whose R.M.S voltage waveform will be in rectangular in shape as shown in Fig. 2.2 and it restores its normal voltage almost instantaneously as soon as the fault is cleared. If the voltage sag is observed at induction motor as a load, due to its dynamic behavior nature , its sag will be prolonging in nature i.e., it cannot restore its normal voltage instantaneously as soon as the fault is cleared as shown in Fig. 2.3 and its waveform will be in non- rectangular shape.

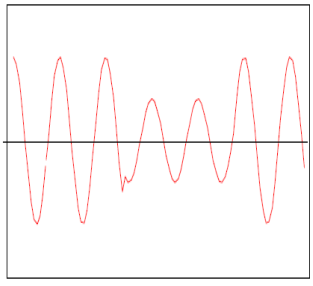


Fig. 2.1 Voltage Sag caused by SLG fault

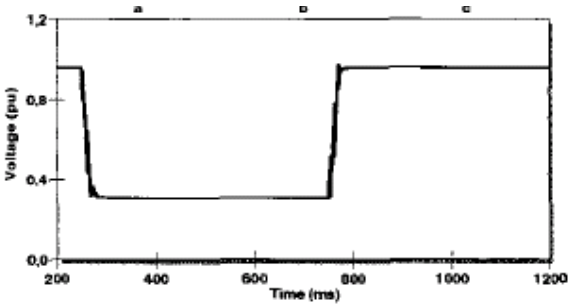


Fig. 2.2 Voltage sag at constant impendence load due to SLG fault (r.m.s voltage)

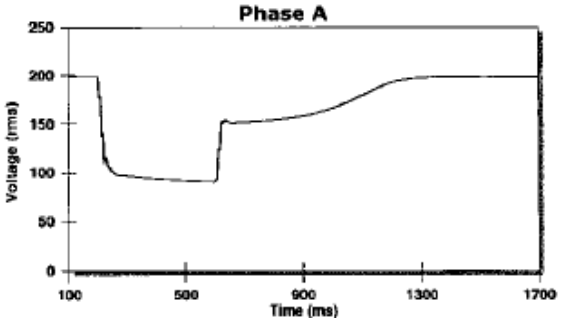


Fig. 2.3 Voltage sag at induction motor load due to SLG fault (rms voltage)

2.4 Main Causes of Voltage Sags

- **Faults in power systems:** Faults in the distribution or transmission line can be classified as three phase faults (L-L-L), single-line-to-ground (SLG), and line-to-line (L-L) faults. SLG faults often result from severe weather conditions such as lightning, ice, and wind. Animal or human activity such as construction or accidents also causes SLG faults. Lightning may cause flashover across conductor insulators and is the major source of SLG faults. Many statistical power quality studies have been performed in various locations and show that most voltage sags are caused by SLG faults. SLG faults can occur at any place in the power system and are nuisance to industrial and commercial customers. Most Severe fault in power systems are the three phase faults and sag due to three phase faults causes maximum damage to the power system.

- **Switching ON large loads: Normally** switching on large inductive load suddenly creates voltage sag and switching on a large capacitive load suddenly causes voltage swell for a few cycles, which may affect the sensitive loads (PLC's, Paper mills etc.,) connected to the same system and causes a huge loss to the industry.

- **Starting large motors** create voltage sags. In case of starting large motors, the voltage sags are usually shallow and last a relatively long time. During start-up, an induction motor takes

a larger current than normal, typically five to six times as large. This current remains high until the motor reaches its normal speed, typically between several seconds and one minute. The drop in voltage depends strongly on the system parameters.

2.5 Characterization of Voltage Sags

Magnitude and duration are the main characteristics of voltage sag. But they do not completely characterize the sag. Voltage during sag contains a rather large amount of higher frequency components. Also the voltage shows a small overshoot immediately after the sag. Most of the current interest in voltage sags is directed to voltage sags due to short circuit faults. These voltage sags are the ones, which cause the majority of the equipment trips. But the starting of induction motors also leads to voltage sags. Voltage sags due to induction motor starting lasts longer than those due to short circuit faults. Typical durations are seconds to tens of seconds.

2.5.1 Methods to calculate the magnitude of Sag

The magnitude of voltage sag can be determined in a number of ways. Most existing monitors obtain the sag magnitude from the rms voltages. There are several alternative ways of quantifying the voltage level. Two obvious examples are the magnitude of the fundamental component of the voltage and peak voltage over each cycle or half cycle. As long as the voltage is sinusoidal, it does not matter whether rms voltage, fundamental voltage, or peak voltage is used to obtain the sag magnitude. But especially during voltage sag this is often not the case.

2.5.1.1 RMS Voltage

As voltage sags are initially recorded as sampled points in time, the rms voltage will have to be calculated from the sampled time domain voltages. This is done by the following equation (1).

$$V_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n} v_i^2}$$

where n is the number of samples per cycle
Vi is the sampled voltages in time domain

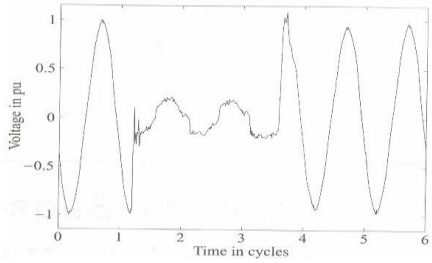


Fig. 2.4 Voltage sag due to a short circuit fault - voltage in one phase in time domain

Equation (1) above has been applied to sag shown in Fig. 2.4. The results are shown in the Fig.s.2.5 and. In Fig. 2.5 rms voltage has been calculated over a window of one cycle, which was 256 samples for the recording used. We see that the rms voltage does not immediately drop to a lower value but takes one cycle for transition. We also see that rms value during the sag is not completely constant and that the voltage does not immediately recover after the fault. A surprising observation is that the rms voltage immediately after the fault is only about 90% of the pre sag voltage. In Fig. 2.6 rms voltage is calculated over the preceding 128 points. The transition now takes place in one half- cycle. A shorter window than one half cycle is not useful. Any other window length will produce an oscillation in the result with a frequency equal to twice the fundamental frequency.

2.5.1.2 Fundamental Voltage Component:

Using the fundamental component of the voltage has the advantage that the phase angle jump can be determined in the same way. The fundamental voltage component as a function of time can be calculated as

$$V_{fund}(t) = \frac{2}{T}\int_{t-T}^{t} V(t)e^{jw_o t}dt$$

where $w_o = 2\pi/T$

T is time period of one cycle of fundamental frequency.

Note that this results in a complex voltage as a function of time. The absolute value of this complex voltage is the voltage magnitude as a function of time. Its phase angle can be used to obtain the phase angle jump. The fundamental component has been obtained for the voltage sag shown in Fig. 2.4. The absolute value of the fundamental component is shown in Fig. 2.7.

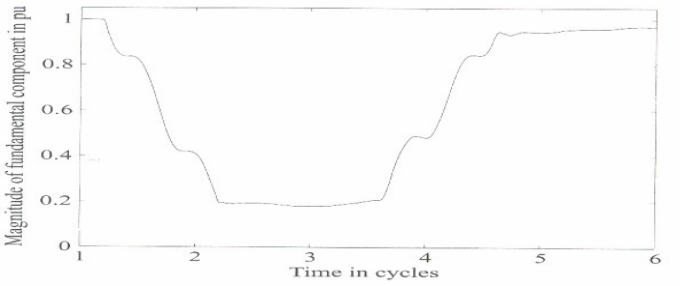


Fig. 2.7 Magnitude of the fundamental component of the voltage sag.

2.5.2 Obtaining One Sag Magnitude

Till now we calculated sag magnitude as a function of time either as the rms voltage, as the peak voltage, or as the fundamental voltage component obtained over a certain window. There are various ways of obtaining one value for the sag magnitude from the magnitude as a function of time. Most monitors take the lowest value. Thinking about equipment sensitivity, this corresponds to the assumption that the equipment trips instantaneously when the voltage drops below certain value. As most sag have a rather constant rms value during the deep part of the sag, using the lowest value appears an

acceptable assumption. One common practice is to characterize the sag through the remaining voltage during the sag. This is then given as a percentage of the nominal voltage. Thus a 70% sag in 120-volt system means that the voltage dropped to 84 volts. Using the remaining voltage as the sag magnitude, leads to some obvious confusions. The main source of confusion is that a larger sag magnitude indicates a less severe event. In fact a sag magnitude of 100% corresponds to no sag at all. The use of terms like "large sag" and "small sag" would be extremely confusing. Instead we will talk about "deep sag" and "shallow sag". Deep sag is sag with a low magnitude; shallow sag has a large magnitude.

2.5.3 Voltage Divider Model for Voltage Sag

To quantify sag magnitude in radial systems, the voltage divider shown in Fig. 2.9 can be used. Using this model some important properties of the sags can be predicted. As shown in Fig. 6 there are two impedances; Zs is the source impedance at the point of common coupling; and Zf is the impedance between the point of common coupling and the fault. The point of common coupling is the point from which both the fault and load are fed. In other words it is the place where the load current branches off from the fault current. Point of common coupling is abbreviated as PCC in the voltage divider model, the load current before as well as during the fault is neglected. There is thus no voltage drop between the load and the PCC.

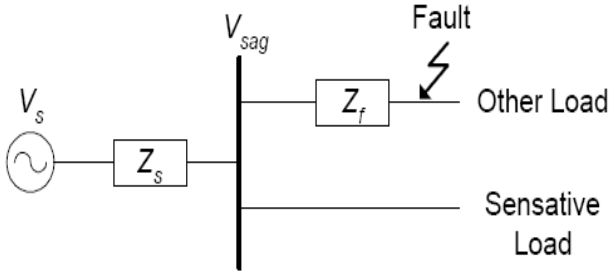


Fig. 2.9 Voltage divider for voltage sag

The voltage at the PCC, and thus the voltage at the equipment terminals, can be found from

$$V_{sag} = \left(\frac{Z_F}{Z_S + Z_F}\right) E \qquad \text{.....(4)}$$

Assume that pre event voltage is exactly 1 p.u. Thus E=1. This results in to the following expression for the sag magnitude.

$$V_{sag} = \left(\frac{Z_F}{Z_S + Z_F}\right) \qquad \text{.....(5)}$$

Any fault impedance should be included in the feeder impedance ZF. We see from above equation that the sag becomes deeper for faults electrically closer to the customer and for systems with a smaller fault level. The above equation can be used to calculate the sag magnitude as a function of distance to the fault. Therefore we have to write ZF = z * L with z the impedance of the feeder per unit length and L the distance between the fault and the PCC leading to

$$V_{sag} = \left(\frac{zL}{Z_S + zL}\right) \qquad \text{.....(6)}$$

2.5.4 Influence of Cross Section

Overhead lines of different cross section have different impedance, and lines and cables also have different impedance. It is thus to be expected that the cross section of the line or cable influences the sag magnitude as well. To show this influence Fig. 2.10 plots the sag magnitude as a function of the distance between the fault and the PCC. The smaller the cross section, the higher the impedance of the feeder and thus lower the voltage drop.

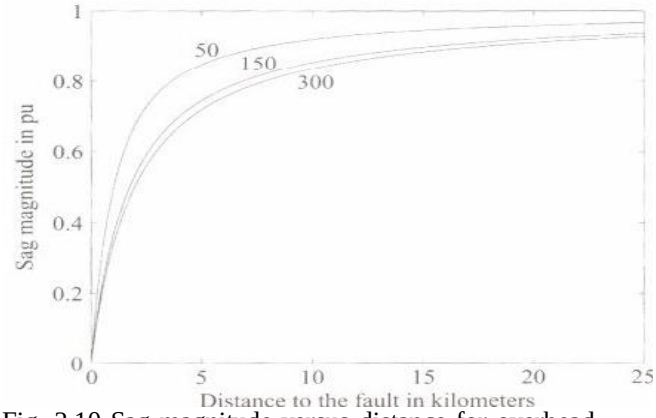


Fig. 2.10 Sag magnitude versus distance for overhead lines with different cross sections

2.5.5 Faults behind Transformers

The impedance between the fault and the PCC in Fig. 2.8 not only consists of lines or cables but also of power transformers. As transformers have rather large impedance, among others to limit the fault level on the low voltage side, the presence of a transformer between the fault and the PCC will lead to relatively shallow sags.

2.5.6 Fault Levels

Often the source impedance at a certain bus is not immediately available, but instead the fault level is. One can of course translate the fault level in to source impedance and calculate the sag magnitude. One may calculate the sag magnitude directly if the fault levels both at the PCC and at the fault position are known. Let SFLT be the fault level at the fault position and SPCC at the point of common coupling. For a rated voltage Vn the relations between fault level and source impedance are as follows.

$$S_{FLT} = \frac{V_n^2}{Z_s + Z_f} \qquad \text{-------(7)}$$

$$S_{Pcc} = \frac{V_n^2}{Z_s} \qquad \text{--------(8)}$$

Therefore the voltage at the PCC can be written as

$$V_{sag} = \frac{S_{FLT}}{S_{pcc}} \qquad \text{----------(9)}$$

2.5.7 Critical Distance

Equation 6 gives the voltage magnitude as a function of the distance to the fault. From this equation we can obtain the distance at which a fault will lead to sag of a certain magnitude. If we assume equal X/R ratio of source and feeder, we obtain

$$L_{crit} = \frac{Z_s}{Z} = \frac{V}{1-V} \quad \text{.....(10)}$$

We refer to this distance as the critical distance for a voltage V. Suppose that a piece of equipment trips when the voltage drops below a certain level (critical voltage). The definition of critical distance is such that each fault with in critical distance will cause the equipment to trip. If we assume further that the number of faults is proportional to the line length with in the critical distance, we would expect that the number of sags below a level V is proportional to $\frac{V}{1-V}$.

2.6 ***Non-Radial systems***

Radial systems are common in low-voltage and medium voltage networks. At higher voltage levels other supply arrangements are common.

2.6.1 Local Generators

The connection of a local generator to a distribution network as shown in Fig. 2.11 mitigates voltage sags of the indicated load in two different ways. The generator increases the fault level at the distribution bus, which mitigates voltage sags due to faults on the distribution feeders. This especially holds for a weak system. For a strong system, the fault level cannot be increased much with out the risk of exceeding the maximum allowable short circuit current of the switchgear. The installation of local generation requires a large impedance of the feeding transformer. A local generator also mitigates sags due to faults in the rest of the system. During such a fault the generator keeps up the voltage at its local bus by feeding in to the fault.

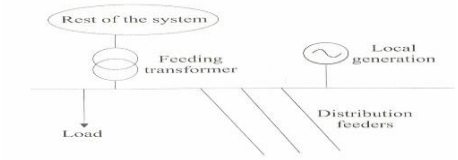


Fig. 2.11 Connection of a local generator to a distribution bus

2.7 **Duration of sags**

The drop in voltage during sag due to short circuit present in the system is already seen. The moment the short circuit fault is cleared by the protection, the voltage can return to its original value. The duration of sag is mainly determined by the fault clearing time, but it may be longer than the fault clearing time. Faults in transmission systems are cleared faster than the faults in distribution systems. In transmission systems, the critical fault clearing time is rather small. Thus, fast protection and fast circuit breakers are essential. Also transmission and sub transmission systems are normally operated as a grid, requiring distance protection or differential protection, both of which are rather fast. The principal form of protection in distribution systems is over current protection. This requires often some time grading which increases the fault clearing time. An exception is systems in which current limiting fuses are used. These have the ability to clear a fault with in one half cycle. Thus it is clear that sag duration will be longer when sag originates in the lower voltage level. For overhead lines the influence is rather small as the reactance dominates the impedance. For underground cables, the influence is much bigger. The inductance of cables is significantly smaller than for overhead lines, so that the resistance has more influence on the impedance and thus on the sag magnitude.

2.7.1 **Measurement of Sag Duration**

For sag shown in the Fig. 2.4 it is obvious that the duration is about 2 cycles. However to come up with an automatic way for a power quality monitor to obtain the sag duration is not straightforward. A commonly used definition of sag duration is the number of cycles during which the rms voltage is below a given threshold. This threshold will be somewhat different for each monitor but typical values are around 90%. A power quality monitor will typically calculate the rms value once every cycle. This gives an over estimation of the sag duration as shown in Fig. 2.14.

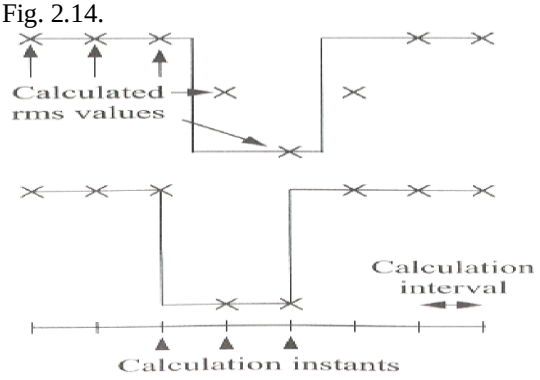


Fig. 2.14 Estimation of sag duration by power quality monitor for a two-cycle sag.

The normal situation is shown in the upper Fig.. The rms calculation is performed at regular instants in time and the voltage sag starts some where in between those two instants. As there is no correlation between the calculation instants and the sag commencement, this is the most likely situation. We see that the rms voltage is low for three samples in a row. The sag duration according to the monitor will be three cycles. Here it is assumed that the sag is deep enough for the intermediate rms value to be below the threshold. The bottom curve of Fig. 2.14 shows the rare situation where the sag commencement almost

coincides with one of the instants on which the rms voltage is calculated. In that case monitor gives the correct sag duration. Calculating the rms voltage once a cycle, it is obvious that the resulting sag will be an integer number of cycles. For 2.5 cycle sag the computed sag duration will be either two or three cycles. For large thresholds the recorded sag duration will be an over estimation. A 90% threshold gives 2.8 cycle sag duration and 80% threshold 2.5 cycles duration. For Lower thresholds the recorded sag duration is an under estimation. A 60% threshold gives 2.1-cycle duration and 40% threshold 2.0-cycle duration. In reality threshold this low will not be used. The duration of deep sags will be over estimated, and the duration of shallow ones under estimated. As the shortest duration window for calculating the sag magnitude is one half cycle, an error up to one half cycle must be accepted. Several methods have been suggested to measure sag initiation and voltage recovery more accurately. The above-mentioned error in sag duration is only significant for short duration sags. For longer sags it does not really matter. But for longer sags the so-called post fault sag will give a serious uncertainty in sag duration. When the fault is cleared the voltage does not recover immediately. The rms voltage after the sag is slightly lower than before the sag. The effect can be especially severe for sags due to three phase faults. Due to drop in voltage during the sag, induction motors will slow down. The torque produced by an induction motor is proportional to the square of the voltage, so even a rather small drop in voltage can already produce a large drop in torque and thus in speed. The moment the fault is cleared and the voltage comes back, the induction motors start to draw a large current up to ten times their normal current. Immediately after the sag, the air gap field will have to be built up again. In other words the induction motors behaves like a short-circuited transformer. After the flux has come back in to the air gap, the motor can start reaccelerating which also requires a rather a large current. It is this post fault inrush current of induction motors which leads to an extended sag. The post fault sag can last several seconds much longer than the actual sag. The post fault sag will cause uncertainty in the sag duration as obtained by a power quality monitor. Different monitors can give different results. This is shown in Fig. 2.15

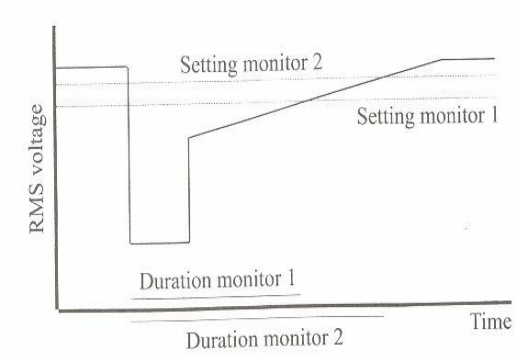


Fig. 2.15 Error in sag duration due to post-fault sag

Assume that monitor 1 has a setting as indicated and monitor 2 a slightly higher setting. Both monitors will record a sag duration much longer than the fault clearing time. The fault clearing time can be estimated from the duration of the deep part of the sag. We see that monitor 2 will record a significantly longer duration than monitor 1.

2.8 Point-on-wave Characteristics

The voltage sag characteristics discussed till now (magnitude and duration) are related to the fundamental frequency component of the voltage. They require the calculation of the rms value of the voltage or the complex voltage over a period of one half cycle or longer. We saw earlier how this leads to an uncertainty in the calculation of sag duration. To obtain a more accurate value for the sag duration one needs to be able to determine "start" and "ending" of the sag with a higher precision. For this we need to find the so called "point-on-wave of sag initiation" and the point-on-wave of voltage recovery".

2.8.1 Point-on-wave of Sag Initiation

The point on wave of sag initiation is the phase angle of the fundamental voltage wave at which the voltage sag starts. This angle corresponds to the angle at which short circuit fault occurs. As most faults are associated with flashover, they are more likely to occur near voltage maximum than near voltage zero. When quantifying the point on wave a reference point is needed. The upward zero crossing of the fundamental voltage is an obvious choice. One is likely to use the last upward zero crossing of the pre event voltage as reference as this closely resembles the fundamental voltage. Fig. 2.16 plots all three phases of the sag. For each phase, the zero point of the horizontal axis is the last upward zero crossing before the start of the event in that phase. We see that point on wave is different in the three phases. This is obvious if one realizes that the event starts at the same moment in time in three phases. As the voltage zero crossings are 120^0 shifted the point on wave value differ by 120^0. In case phase-to-phase voltages are used, the resulting values are again different. When quantifying point-on –wave it is essential to clearly define the reference.

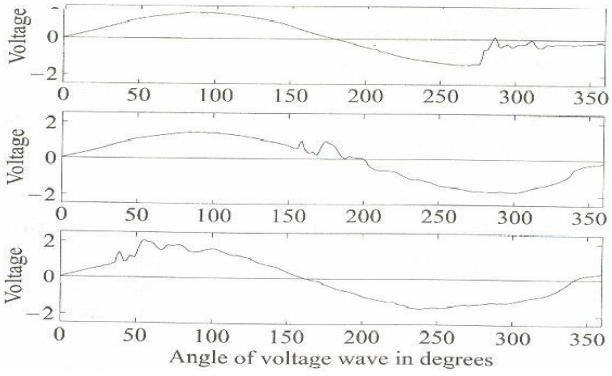


Fig. 2.16 Event initiation in the three phases compared to the last upward zero crossing

2.8.2 Point-on-wave of Voltage Recovery

The point on wave of voltage recovery is the phase angle of the fundamental voltage wave at which the main recovery takes place. We saw before that most existing power quality monitors look for the point at which the voltage recovers to 90% or 95% of the nominal voltage. Voltage recovery corresponds to fault clearing, which takes place at current zero crossing. Because the power system is mainly inductive, current zero crossing corresponds to voltage maximum. Thus we expect points on wave of voltage recovery to be around 90deg or 270deg. This assumes that we use the pre event fundamental voltage as reference, not the during event voltage. It is the pre event voltage, which drives the fault current, and which is thus 90deg shifted compared to the fault current. For a two phase-to-ground or three-phase fault, fault clearing does not take place in all three phases at the same time. This could make a determination of the point on wave of voltage recovery is difficult.

2.9 The Missing Voltage

The missing voltage is another voltage sag characteristic, which has been proposed recently. The missing voltage is a way of describing the change in momentary voltage experienced by the equipment. One can think of the missing voltage as a complex voltage, being the difference in the complex plane between the pre event voltage and the voltage during the sag.

III. FACTS INTRODUCTION

A new concept of **Flexible AC Transmission system (FACTS)** which was introduced In late 1980's by **ELETRICAL POWER RESEARCH INSTITUTE (EPRI)** brought radical changes in the power system operation and control. A new technique using FACTS devices linked to the improvements in semiconductor technology opens new opportunities for controlling power and enhancing the usable capacity of existing transmission lines

The FACTS is not a single high power controller, but rather a collection of controllers, which can be applied individually or in co-ordination with others to control one or more of the interrelated system parameters mentioned above. A well-chosen FACTS controller can overcome the specific limitations of a designated transmission line or a corridor. Because all FACTS controllers represent applications of the same basic technology, there production can eventually take advantage of technologies of scale. Just as a transistor is a basic element for a whole variety of micro-electronic chip and circuits, the Thyristor or high power transistor is the basic element for a variety of high power electronic controllers.

BASIC TYPES OF FACTS DEVICES

In general, FACTS controllers can be divided into four categories:

- Series Connected Controllers
- Shunt Connected Controllers
- Combined Shunt and Series Controllers

BENEFITS FROM THE FACTS TECHNOLOGY

- Control of power flow as ordered
- Increasing of loading capability of lines to their thermal capabilities
- Increase the system security through raising the transient stability limit, limiting short-circuit currents and overloads, managing cascading blackouts and damping electro mechanical oscillations of lower systems and machines
- Provide secure tie line connections to neighboring utilities and regions thereby decreasing overall generation reserve requirements on both sides.
- Provide greater flexibility in siting new generation.
- Upgrade of lines.
- Reduce reactive power flows, thus allowing the lines to carry more active power.
- Reduce loop flows Increase utilization of lowest cost generation

BASIC TYPES OF FACTS CONTROLLERS

FACTS devices are integrated in a system for a variety of reasons, such as power flow control, reactive power (var) compensation, loop flows or ancillary functions like damping of oscillations. These devices can be applied in shunt, in series, and in some cases, both in shunt and series. Series devices include Thyristor-controlled series capacitors (TCSC) and fixed series capacitors (SC). Shunt devices include static var compensators (SVC), and SVC Light® (otherwise known as STATCOM)

5.1-STATIC SERIES COMPENSATORS

Fixed series capacitors (SC):

The series controller can be a variable impedance, such as capacitor, reactor or power electronics based variable source of min frequency, sub synchronous and harmonic frequencies (or a combination) to serve the desired need in principle all controllers inject voltage in series with the line. Even variable impedance multiplied by the current flow through it, represents an injected series voltage in the line. As long as the voltage is in phase quadrature with line current, the series controller only supplies or consumes variable reactive power. Any other phase relationship will involve handling of real power as well. Static series compensation is used in order to decrease the transfer reactance of a power line at power frequency. A series capacitor installation generates reactive power that, in a self-regulating manner, balances a fraction of the line's transfer reactance. The result is improved functionality of the power transmission system through:

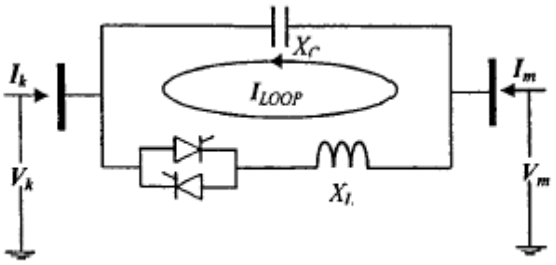
- increased angular stability
- improved voltage stability

Various types of Static series compensators are:

GCSC - GTO Thyristor-controlled series capacitor.

TSSC - Thyristor switched series capacitor.
TCSC - Thyristor-controlled series capacitor.
SSSC - Static synchoronous series compensator.

TCSC - Thyristor-controlled series capacitor:



Thyristor Controlled Series Capacitors (TCSC) provide a proven technology that addresses specific dynamic problems in transmission systems. TCSC's are an excellent tool to introduce if increased damping is required when interconnecting large electrical systems. Additionally, they can overcome the problem of Subsynchronous Resonance (SSR), a phenomenon that involves an interaction between large thermal generating units and series compensated transmission systems.

5.2-STATIC SHUNT COMPENSATORS

As in the case of the series controller, the shunt controllers may have a variable impedance, variable source, or a combination of these. In principle, all shunt controllers inject current into the system at the point of connection. Even variable shunt impedance connected to the line voltage causes a variable current flow and hence represents injection of current into the line. As long as the injected current is in phase quadrature with the line voltage, the shunt controller only supplies or consumes variable reactive power. Any other phase relationship will involve handling of real power as well.

Various types of static shunt compensators are:

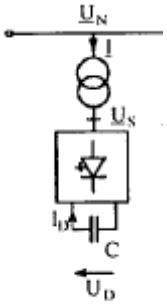
- SVC - Static Var Compensation
- STATCOM – STATic COMpensator.

Static Var Compensation – SVC:

Electrical loads both generate and absorb reactive power. Since the transmitted load varies considerably from one hour to another, the reactive power balance in a grid varies as well. The result can be unacceptable voltage amplitude variations, a voltage depression, or even a voltage collapse. A rapidly operating Static Var Compensator (SVC) can continuously provide the reactive power required to control dynamic voltage swings under various system conditions and thereby improve the power system transmission and distribution performance. Installing an SVC at one or more suitable points in the network can increase transfer capability and reduce losses while maintaining a smooth voltage profile under different network conditions. In addition, an SVC can mitigate active power oscillations through voltage amplitude modulation.

STATCOM:

STATCOM (STATic COMpensator) has a characteristic similar to the synchronous condenser, but as an electronic device, it has no inertia and is superior to the synchronous condenser in several ways - better dynamics, a lower investment cost, and lower operating and maintenance costs. STATCOM is to be selected when the technical performance in a specific application so requires. However, utilizing thyristors with turn-off capability (GTO or IGCT), which is the common approach in the industry, does not allow the full potential of a STATCOM concept to be obtained.

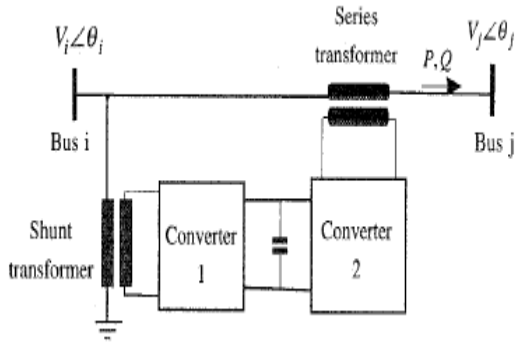


STATCOM are based on voltage source converter technology equipped with IGBT (Insulated Gate Bipolar Transistor).With the advent of STATCOM, better performance can be reached in areas such as:

- dynamic and steady-state voltage control
- transient stability improvements
- power oscillation damping
- ability to control active as well as reactive power.

5.3-Combined series –series controllers:

UPFC (**U**nified **P**ower **F**low **C**ontroller): A combination of static synchronous compensator (STATCOM) and a static synchronous series compensator (SSSC) which are coupled via a common dc link, to allow bi-directional flow of real power between the series output terminals of the SSSC and the shunt output terminals of the STATCOM, and are controlled to provide concurrent real and reactive series line compensation without an external electric energy source. The UPFC ,by means of angularly unconstrained series voltage injection ,is able to control ,concurrently or selectively, the transmission line voltage, impedance, and angle or, alternatively .the real and reactive power flow in the line. The UPFC may also provide independently controllable shunt reactive compensation.



IV. VOLTAGE SAG/SWELL MITIGATION USING DYNAMIC VOLTAGE RESTORER (DVR)

3.1 *Voltage Sag Mitigation Methods*

Power quality problems cannot be avoided for the consumers (end users) who are directly connected together by the interconnected systems. Therefore, consumers must protect themselves from PQ problems with mitigation or power conditioning devices. It is researched by EPRI that 90 % of all power quality problems are voltage sags in the USA and it is assumed that the European power network exhibits similar attributes. In Turkey, the problem should be worse as the power grid is weak and frequent daily interruptions are not unusual. Therefore, the voltage sag correction solutions are the most important issue for consumers.

If protection from power quality problems is treated step by step, the following stages could be obtained.

1. Solutions during production of equipment

The basic and most cost effective solution is to strengthen sensitive devices against power quality problems during production. For example, IT (Information Technology) manufacturers use a specific curve (ITIC curve) that defines performance criteria involving voltage sags. Their manufactured equipment must remain functional within a specific voltage-time duration range during voltage sags. ITIC (Information Technology Industry Council) was formerly known as the CBEMA (Computer & Business Equipment Manufacturers Association). CBEMA generated a curve known as CBEMA curve which shows the susceptibility limits for computer equipment. Then, ITIC developed the CBEMA curve and this is known as ITIC curve now. Shown in Fig. 3.1, the ITIC (CBEMA) curve is a set of curves representing the withstanding capability of computers connected to 120-V, 60-Hz power systems in terms of the magnitude and duration of the voltage disturbance.

Seven regions are described in this curve but the most important regions relevant to this thesis are the following:

i). **Voltage Sags**: Sags down to 80 % of nominal voltage (20 % sag) are assumed to have a typical duration of up to 10 seconds. Sags to 70 % of nominal voltage (30 % sag) are assumed to have a duration of up to 0.5 seconds.

ii). **Line Voltage Swell**: This is the voltage swell region, having an RMS amplitude of up to 120 % of the RMS nominal voltage, with a duration of up to 0.5 seconds.

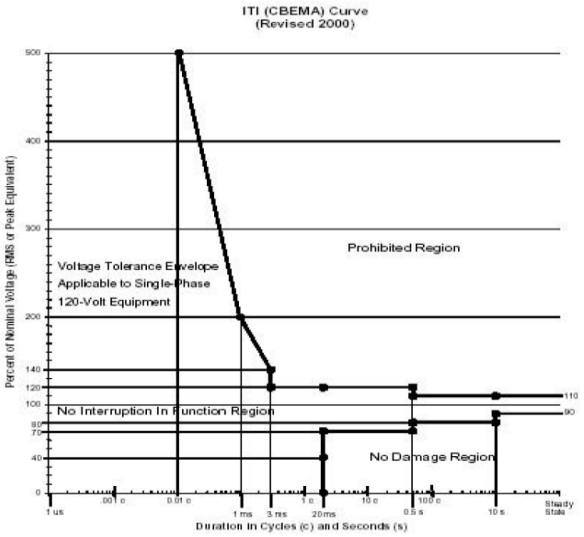


Fig. 3.1 The ITIC curve

iii). **No Damage Region**: In this region, the ITE (Information Technology Equipment) is not expected to operate but it should not be damaged.

iv). **Prohibited Region**: In this region, ITE may be damaged.

2. **Analysis of effects and medium**

The second basic method for solving voltage sag related power quality problems is the analysis of effects and medium which transmits power quality problems. For example, removing the sensitive equipment from the source of problem could be a cost effective solution. In other cases, by improving weak wiring and grounding, the sensitive equipments could be saved. Removing the medium which transmits the power quality problems could also be another cost effective solution.

3**. Power conditioning equipment**

If the above approach can not be implemented, then installing a proper power conditioning equipment is a common solution for the power quality problems. Power conditioning equipment includes devices that reduce or eliminate the effects of a power quality disturbance. Power conditioning usually involves voltage conditioning because most power quality problems are voltage quality problems. Most devices are utilized to condition or modify the voltage magnitude or frequency. Power conditioning can be used to condition the source, the transmitter, or the receiver of the power quality problem. The cost of power conditioning solutions is increased from end-user side

to utility side. Some common power conditioning equipment that correct voltage sags are given below.

1. Line-voltage regulators: These regulators are transformers specially designed to regulate the output voltage when the input voltage changes. They make changes to keep the output voltage relatively constant. Types of line regulators are: Tap changers, buck-boost regulators, CVT (Constant- voltage transformer).

2. M-G Sets (Motor-generator Sets): A motor is connected to the utility supply and runs the generator through a shaft or belt, providing clean power to critical equipment. If power is interrupted, the generator keeps supplying power to critical loads by using diesel or natural gas as the fuel. A rechargeable battery pack or a flywheel can be added to M-G Sets to provide power during ride through. Maintenance and safety are the main concern.

3. **Magnetic Synthesizers**: These regulators employ resonant circuits which are made of nonlinear inductors and capacitors to store energy, pulsating saturation transformers to modify the voltage waveform, and filters to filter out harmonic distortion. They supply power through a zig- zag transformer, which traps triplen harmonic currents and prevents them from reaching the power source. They can be bulky and noisy.

4. SVC (Static VAR Compensators): These regulators utilize a combination of capacitors and reactors to regulate the voltage quickly. They use solid-state switches that insert the capacitors and reactors at the right magnitude to keep the voltage from fluctuating. However they are quite large and expensive.

5. **UPS (Uninterruptible Power Supplies)**: A UPS conditions the voltage, both during voltage sags and outages. It provides a constant voltage from a static source (battery, ferroresonant transformer, superconducting magnet etc.) or rotary source (diesel motor generator set) . The basic building blocks of a UPS system include the battery (with a 5 to 60 minute backup capability depending on its size), an inverter, and a rectifier. They are connected in three different configurations.

i. On-line UPS: Battery backup and continuous sag/swell protection is available all the time. It has a shorter battery life.

ii. Off-line UPS: Time delay of 4-10 milliseconds to engage the UPS during an interruption. It has a longer battery life.

iii. Line interactive UPS: A hybrid of the above two types. It has a shorter time to engage UPS and also saves battery life.

iv. A Rotary UPS module (i.e., a motor-generator set) can be added to the above types to produce a waveform independent of utility voltage and provide a longer backup time during outages.

6. **SMES (Superconducting magnetic energy storage)**: SMES stores electrical energy within a superconducting magnet. It provides a large amount of power (750 kVA to 500 MVA) for a short time (2 seconds) very quickly (within 2 milliseconds).

7**. Fuel Cell Based Inverter System**: The main disadvantage is its high cost.

Present day modern equipments are very sensitive to voltage sags and they need the mitigating device to be very fast in acting, which cannot possible by the above conventional devices. So in order to overcome the above disadvantages, a new category of devices called custom power devices are developed. Custom power devices are the new generation of power electronics-based equipment aimed at enhancing the reliability and quality of power flows in low-voltage distribution networks. There are various custom power devices available such as DVR (dynamic voltage restorer), Dstatcom, UPQC (Unified Power Quality Conditioner) etc., which are based on inverter topology and PWM switching auto transformer, which are based on the converter topology. In the next two chapters Voltage sag mitigation by DVR and Dstatcom are discussed with respect to their modeling and their results are presented to show their effectiveness.

3.2 *Voltage Sag Mitigation using Dynamic Voltage Restorer (DVR)*

A series-connected converter-based mitigation device, the dynamic voltage restorer (DVR),is the most economical and technically advanced mitigation device proposed to protect sensitive loads from voltage sags . The DVR shown in Fig. 3.1 is based on an inverter system that has energy storage for supplying active power, an output filter to make more sinusoidal voltage, and a step up transformer. The DVR is one of the FACTS devices that use the power electronics technology, especially inverter technology and is configured as a series-connected voltage controller. To control the output voltage of the DVR, the inverter supplies the missing load voltage using self-commutable electronic switches such as a gate turn-off thyristor (GTO), an insulated gate bipolar transistor (IGBT), or an insulated gate commutated thyristor (IGCT). The DVR injects the missing voltage in a series. Therefore, it can be called a series voltage controller, but the term DVR is commonly used now. DVRs have a same configuration of SSSC. The DVRs can be operated with a relatively small capacitor to exchange reactive power or can supply active powers to loads with energy storage.

The large capacitor bank, flywheel, superconducting magnetic device, and battery can be used for the energy storage. The DVR, located between the supply and critical loads, has

demonstrated excellent dynamic capability for mitigating voltage sags or swells. Each phase can be controlled independently, and the DVR can adjust the magnitude of the load voltage and the voltage phase angle as well. The advantages of the DVR are its fast response and ability to compensate for voltage sag and a voltage phase shift using an inverter system.

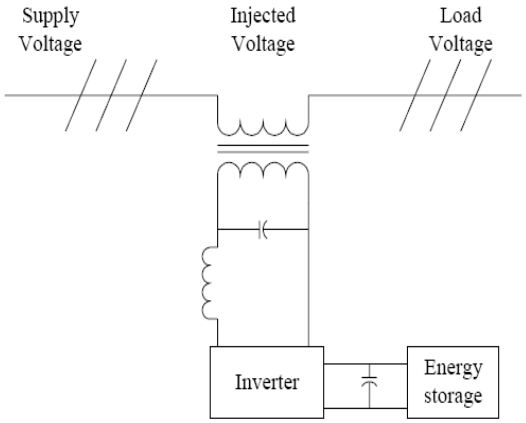


Fig. 3.2 Configuration of Dynamic voltage restorer

3.2.1 Analysis of Dynamic voltage restorer

Operating Principle:

The series voltage controller consists of a voltage source converter in series with the supply voltage, as shown in Fig. 3.2. The voltage at the load terminals equals the sum of the supply voltage and output voltage of the controller as shown in eq 3.1.

$$\bar{V}_{load} = \bar{V}_{cont} + \bar{V}_{sa} \quad \text{……(3.1)}$$

A converter transformer is used to connect the output of the voltage-source converter to the system. A relatively small capacitor is present on dc side of the converter. The voltage over this capacitor is kept constant, by exchanging energy with the energy storage reservoir. The required output voltage is obtained by using a pulse width modulation switching pattern. As the controller will have to supply active as well as reactive power, some kind of energy storage is needed. The amount of energy storage depends on the maximum duration of the sag. The controller is typically designed for certain maximum sag duration and a certain minimum sag voltage.

3.2.2 Voltage Sag Correction by DVR

The schematic diagram of a typical DVR is shown in Fig. 3.3. The circuit on left hand side of the DVR represents the Thevenin equivalent circuit of the system. The system impedance ($Z_{th} = R_{th} + jX_{th}$) depends on the fault level of the load bus. When the system voltage (V_{th}) drops, the DVR injects a series voltage V_{DVR} through the injection transformer so that the desired load voltage magnitude V_L can be maintained. The series injected voltage of the DVR can be written as

$$V_{DVR} = V_L + Z_{th} I_L - V_{th} \quad \text{……..(3.2)}$$

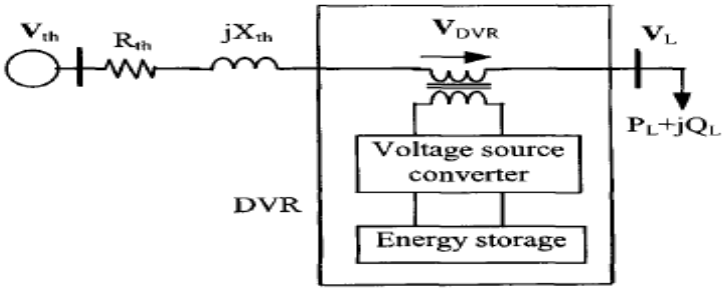


Fig. 3.3 schematic diagram of DVR

Here I_L is the load current is given by

$$I_L = \left(\frac{P_L + jQ_L}{V_L} \right) \quad \text{……(3.3)}$$

Where V_L is considered as a reference, eq (3.2) can be rewritten as

$$V_{DVR} = (V_L + Z_{th} I_L) - V_{th} \quad \text{……(3.4)}$$

Here α, β and δ are the angles of V_{DVR} , $Z_{th,}$ and V_{th} respectively and θ is the load power factor angle ($\theta = \tan^{-1}\left(\frac{Q_L}{P_L}\right)$). The complex power injection of the DVR can be written as

$$S_{DVR} = V_{DVR} I_L^* \quad \text{……..(3.5)}$$

3.2.2.1 Active Power Injection

To assess the storage requirements we calculate the active power delivered by the controller , using the notation in Fig. 3.4. We assume that the voltage at the load terminals is 1 pu along the positive real axis:

$$\bar{V}_{load} = 1 + j0 \quad \text{……(3.6)}$$

The load current is 1 pu in magnitude, with a lagging power factor $\cos\phi$

$$I_{load} = \cos\phi - j\sin\phi \quad (3.7)$$

The voltage sag at the system side of the controller has a magnitude V and phase- angle jump ψ :

$$V_{sag} = V\cos\psi + jV\sin\psi \quad (3.8)$$

The complex power taken by the load is found from

$$P + jQ = V_{load} I_{load}^* = \cos\phi + j\sin\phi \quad (3.9)$$

The complex power taken from the system is

$$P_{sys} + jQ_{sys} = V_{sag} I_{load}^* = V\cos\psi + jV\sin\psi \quad (3.10)$$

The active power that needs to be generated by the controller is the difference between the active power taken from the system and the active part of the load:

$$P_{cont} = P_{load} - P_{sys} \quad (3.11)$$

This can be written as

$$P_{cont} = \left[1 - \frac{V_{cont}}{V_{sag}} \cos\phi\right] \times P_{load} \quad (3.12)$$

For zero phase angle jump, we obtain the following simple expression for the active power requirement of the controller:

$$P_{cont} = [1 - V_{sag}] P_{load} \quad (3.13)$$

The active power requirement is linearly proportional to the drop in voltage. When phase-angle jumps are considered the relation is no longer linear and becomes dependent on the power factor also.

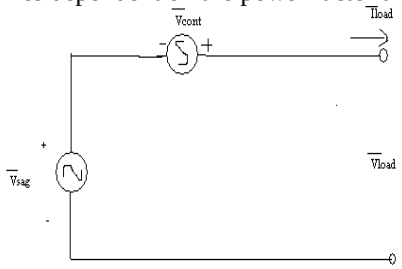


Fig. 3.4 circuit diagram with power system , series controller, and load

V. MODELING OF DVR

4.1. PRINCIPLES OF OPERATION

Fig. 4.1 shows the circuit schematic of the DVR with three phase transmission system. It consists of inverters, output LC filters, and injection transformers. The dc side is connected to a capacitor bank, formed by two capacitors. Each capacitor has the value ofC_d . The inverter shown in Fig. 4.1 is a half bridge configuration. However, the operation is similar in the full bridge configuration. The DVR is operated as a controllable voltage source$v_{d,n}$, where n represents either phase a, b, or c. It is connected between the supply and the load. The relationship among the supply voltage$v_{s,n}$, the load voltage $v_{d,n}$and v_{o1}.

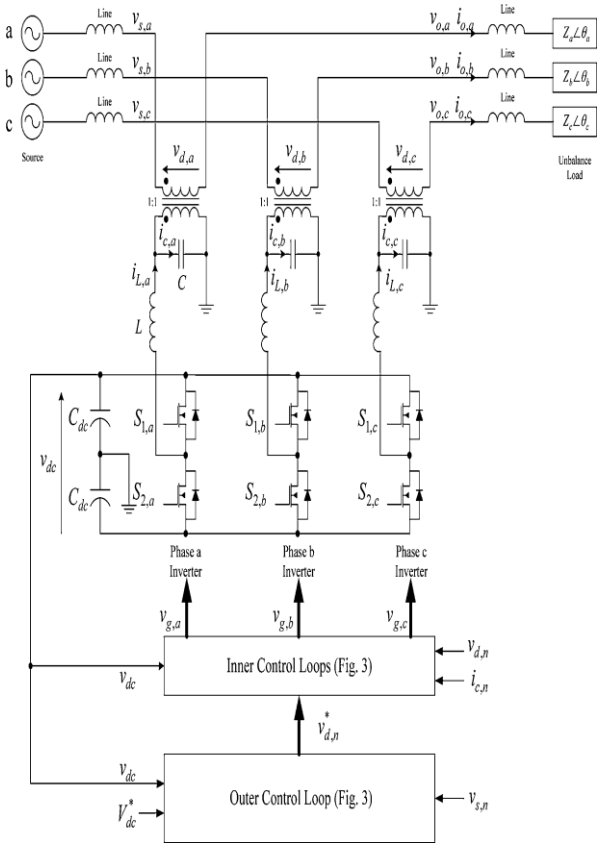


Fig.4.1. Structure of the proposed interlines DVR and its connection to the utility.

$$v_{d,n}(t) = v_{s,n}(t) - v_{o,n}(t) \quad \ldots 4.1$$

Fig. 4.3 shows the phasor diagrams of $\boldsymbol{v_{s,n}}$, $\boldsymbol{v_{o,n}}$, $\boldsymbol{v_{d,n}}$, and the load current$i_{o,n}$ in voltage sag and unbalanced conditions. Fig. 4.2 shows the control block diagram of proposed control scheme. The control scheme consists of two main loops. The first control loop, namely inner loop, is formed in each phase. It is used to generate the gate signals for the switches in the inverter, so that

$v_{d,n}$ will follow the DVR output reference $v^*_{d,n}$. This loop has fast dynamic response to external disturbances. Its operating principle is based on extending the boundary control technique with second-order switching surface in [19]–[21]. The second loop, namely outer loop, is used to generate $v^*_{d,n}$ .Based on (Eq. 4.1)

$$v^*_{d,n}(t) = v_{s,n}(t) - v^*_{o,n}(t) \quad \ldots 4.2$$

Where$v^*_{o,n}$ is the load-voltage reference and is generated by the phase-lock loop (PLL)

The outer loop is used to regulate the dc-link voltage by adjusting the phase of the inverter load voltage with respect to the load current. Its bandwidth is set much lower than the line frequency. The purpose is to attenuate the undesirable signals, which are due to the ac component on the dc-link voltage and the load current, getting into the loop. Since the inner and outer loops have different dynamic behaviors, the controller

will react differently in the voltage sags of short [22]–[25] and long durations. If the duration of the voltage sag is short, typically less than 0.5 s, the inner loop will react immediately and maintain the wave shape of the load voltage. The outer loop is relatively inert during the period. The sagged phase(s) will be supported purely by the capacitor bank. The capacitor voltage will decrease. After the voltage sag, the outer loop will start reacting to the decrease in the capacitor voltage. The capacitor will be charged up from the supply by adjusting the phase angle of the inverter output. If the duration of the voltage sag is long, the inner loop will keep the wave shape of the load voltage and the outer loop will regulate the dc-link voltage. Thus, the sagged phase(s) will be supported by the dc link, while electric energy will also be extracted from the un sagged phase(s) through the dc link. In the steady-state operation, as the frequency response of the inner loop is very fast, the wave shape of the load voltage can be kept sinusoidal, even if there are harmonic distortions in the supply voltage and the load current. Moreover, with the interline energy flow in the outer-loop control; the output quality can be maintained, even if there is an unbalanced supply voltage. At any time, the amplitude of $v_{o,n}^{*}$ is fixed because the load voltage is regulated at the nominal value. $v_{o,n}^{*}$ Has the same frequency as $v_{s,n}$, and the phase angle β between $v_{o,n}^{*}$ and $v_{s,n}$ is controlled by the signal v_{β} shown in Fig. 4.3. The supply voltages can be expressed as follows:

$$v_{s,a}(t) = v_{sm,a}\cos\omega t \quad \ldots 4.3$$

$$v_{s,b}(t) = v_{sm,b}\cos(\omega t - 120) \quad \ldots 4.4$$

$$v_{s,c}(t) = v_{sm,c}\cos(\omega t + 120) \quad \ldots 4.5$$

Where $V_{sm,a}$,$V_{sm,b}$, and $V_{sm,c}$ are the peak values of the supply voltages of the phases a, b, and c, respectively, and ω is the angular line frequency.

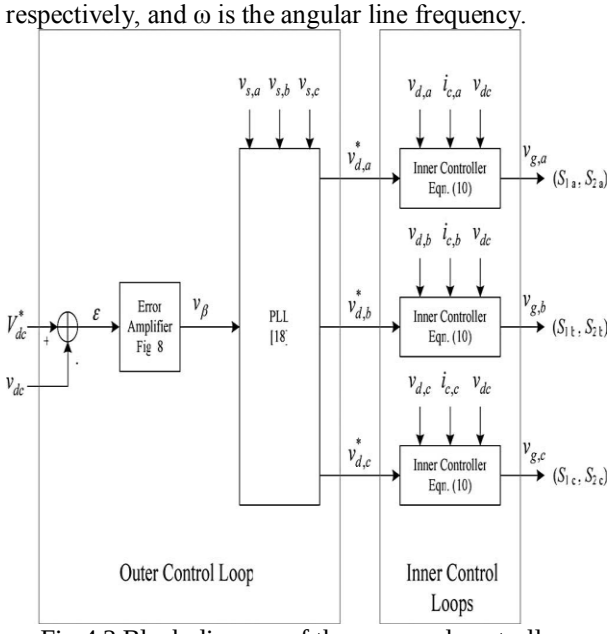


Fig.4.2 Block diagram of the proposed controller

4.2. REVIEW OF INNER LOOP

The inner-loop control strategy is by using boundary control with second order switching surface [19]. A brief review of the inner loop will be given in this section. In one leg of the three-phase half-bridge inverter, which is shown in Fig. 4.1, as S1,n and S2,n are operated in anti phase and the output inductor current is continuous, two possible switching modes are derived, and their state-space equations are shown as follows.

When S1,n is OFF and S2,n is ON

$$\dot{x}_n = \begin{bmatrix} 0 & -1/L \\ 1/C & \left(-\frac{1}{R}\right)*C \end{bmatrix} x_n + \begin{bmatrix} -\frac{1}{2}L & 0 \\ 0 & \left(\frac{1}{R}\right)*C \end{bmatrix} u_n \quad \ldots 4.6$$

$$\upsilon_{d,n} = \begin{bmatrix} 0 & 1 \end{bmatrix} x_n \quad \ldots 4.7$$

When S1,n is ON and S2,n is OFF

$$\dot{x}_n = \begin{bmatrix} 0 & -1/L \\ 1/C & \left(-\frac{1}{R}\right)*C \end{bmatrix} x_n + \begin{bmatrix} \frac{1}{2}L & 0 \\ 0 & \left(\frac{1}{R}\right)*C \end{bmatrix} u_n \quad \ldots 4.8$$

$$\upsilon_{d,n} = \begin{bmatrix} 0 & 1 \end{bmatrix} x_n \quad \ldots 4.9$$

Where $x_n = [\, i_{L,n}\ \upsilon_{C,n}\,]^T$; $u_n = [\, V_{dc}\ \ V_{s,n}\,]^T$ ..4.10

And RL,n is the fictitious resistance showing the ratio between the load voltage and load current. Fig. 4.4(a) and (b) shows the equivalent circuits of the two modes corresponding to Eq. 4.6 to 4.10.

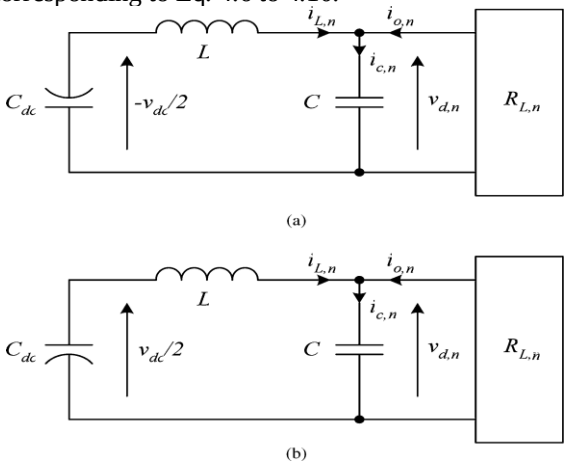


Fig.4.4. Equivalent circuits of one phase in the inverter system.

(a) S1,n is OFF and S2,n is ON (b) S1,n is ON and S2,n is OFF

A. Criteria for Switching S1,n OFF and S2,n ON:

S1,n and S2,n are originally ON and OFF, respectively [19]. S1,n and S2,n are going to switch OFF and ON, respectively. The criteria for switching S1,n OFF and S2,n ON are as follows:

$$\upsilon_{d,n}(t_1) \geq \upsilon_{d,n,max} - \frac{L}{2C}\left[1/(\upsilon_{DC}(t_1)/2) + \upsilon_{d,n}(t_1)\right] i^2_{C,n}(t_1) \quad \ldots 4.11$$

$$i_{C,n}(t_1) \geq 0 \quad \ldots 4.12$$

B. Criteria for Switching S1,n ON and S2,n OFF:

S1,n and S2,n are originally OFF and ON, respectively. S1,n and S2,n are going to switch ON and OFF, respectively [19]. The criteria for switching S1,n ON and S2,n OFF are as follows:

$$\upsilon_{d,n}(t_3) \leq \upsilon_{d,n,min} + \frac{L}{2C}\left[1/(\upsilon_{DC}(t_3)/2) - \upsilon_{d,n}(t_3)\right] i^2_{C,n}(t_3) \quad \ldots 4.13$$

$$i_{C,n}(t_3) \leq 0 \quad \ldots 4.14$$

Based on Eq.(8.6)–(8.9) and $\upsilon_{d,n,min} = \upsilon_{d,n,max} = \upsilon^*_{d,n}$, the general form of $\sigma 2$ is defined as follows:

$$\sigma^2\left[i_{L,n}(t), \upsilon_{d,n}(t)\right] = \frac{1}{k}[\upsilon_{d,n}(t) - \upsilon^*_{d,n}(t)] * \left[\frac{\upsilon(t)}{2} + [sgn[i_{C,n}(t)]\upsilon_{d,n}(t)]\right] + sgn[i_{C,n}(t)]i^2_{C,n}(t)$$

Where k = L/2C

…4.15

4.3. CHARACTERISTICS OF OUTER LOOP

A. Steady-State Characteristics:

The function of the outer loop is to regulate υ_{dc} at the reference value of υ^*_{dc}. By applying the conservation of energy, the DVR will ideally have zero-average real power flow at the steady state.

$$P_{s,a} + P_{s,b} + P_{s,c} = P_{o,a} + P_{o,b} + P_{o,c} \quad \ldots 4.16$$

$$P_a = P_b = P_c = 0 \quad \ldots 4.17$$

$$P_{s,n} = \upsilon_{s,n}\, i_{o,n} \cos(\theta_n - \beta) \quad \ldots 4.18$$

$$P_{o,n} = \upsilon_{o,n}\, i_{o,n} \cos(\theta_n)\ ;\ P_n = \upsilon_{d,n}\, i_{o,n} \cos(\varphi_n) \quad \ldots 4.19$$

where $P_{s,n}$,$P_{o,n}$, and $P_n$are the input, output powers, and power transferred of the each phase, respectively, $i_{o,n}$ is the load current of each phase, θ_n is the phase angle between$v_{o,n}$ and $i_{o,n}$, β is the phase angle between $v_{s,n}$ and $v_{o,n}$, andθ_n is the phase angle between $v_{d,n}$ and $i_{o,n}$. Under supply-voltage interruption, the outer loop will adjust the value of β. The DVR will generate the required magnitude and phase of $v_{d,n}$ in each phase individually. The DVR will then absorb (deliver) electric energy from (to) the dc link. As the adjustment of β is common to the three phases, the sagged phase(s) will be supported by the capacitor bank and the un sagged phase(s). The corresponding equations of$v_{o,n}$ are as follows:

$$\upsilon_{o,a}(t) = V_{om,a}\cos(\omega t - \beta) \quad \ldots 4.20$$

$$\upsilon_{o,b}(t) = V_{om,b}\cos(\omega t - 120^\circ - \beta) \quad \ldots 4.21$$

$$\upsilon_{o,c}(t) = V_{om,c}\cos(\omega t + 120^\circ - \beta) \quad \ldots 4.22$$

Where $V_{om,n}$ is the peak load voltage of phase n.

Fig. 4.3 shows the steady-state phasor diagrams with one-phase sagged and three-phase voltage balancing, respectively. The parameters used are based on Tables 4.1-4.3. In Fig. 4.3(a), $v_{s,n}$ is reduced to 120 V, while the other phases are at the nominal value of 220 V. By increasing the value of β, $V_{d,a}$ is established by the DVR and $V_{o,a}$ can be kept at 220 V. Thus, part of the energy supplied to phase-a load is supported by phase's b and c.

In Fig. 4.3(b), all three phases are unbalanced, where$V_{s,a}$ = 210 V, $V_{s,b}$ = 190 V, and $V_{s,c}$ = 240 V. Again, by adjusting the value of β, $V_{o,a}$, $V_{o,b}$, and $V_{o,c}$ are regulated at 220 V. For the phase transformation between β and θ_n

$$\alpha = -(\beta - \varphi_n - \theta_n) \quad \ldots 4.23$$

Where $\propto_n$ is the phase difference between $V_{s,n}$ and $V_{d,n}$.

Based on Fig. 4.3(a) and by using Equations (4.19) to (4.23), it can be shown that the steady-state power-transfer equation can be expressed as follows:

$$P_n = i_{o,n}\sqrt{v_{o,n}^2 + v_{s,n}^2 - 2v_{o,n}v_{s,n}\cos\beta} \times \cos\left[\beta - \theta_n + \cos^{-1}\left(\frac{v_{s,n} - v_{o,n}\cos\beta}{\sqrt{v_{o,n}^2 + v_{s,n}^2 - 2v_{o,n}v_{s,n}\cos\beta}}\right)\right] \quad \ldots 4.24$$

Detailed derivation of (34) is given in the Appendix. The values of $v_{s,n}$, $v_{o,n}$, $i_{o,n}$, and θ_n are different in each phase. Thus, the power flow of each phase inverter is different. β is controlled by the outer loop in order to achieve power equilibrium in the system, and thus, satisfy eq.4.16 and 4.17.

TABLE 4.1 SPECIFICATIONS OF THE DVR

Parameters	Minimum	Nominal	Maximum
Supply voltage, $v_{s,n}$	110V	220V	280V
Load voltage, $v_{o,n}$	~	220V	~
Output current, $i_{o,n}$	0.1A	~	4A
Power factor, cos θ_n	0	~	0.996
dc link voltage, v_{dc}	200V	380V	450V
$v_{L,D}$		2V	
I_{ripple}		2.6A	
Switching frequency		15kHz	

TABLE 4.2 PARAMETERS OF THE PLL AND TRANSDUCER GAINS

Parameter	Value	Parameter	Value
V_{cc}	5V	K_{pd}	1.59
β_{max}	0.785rad	K_{vco}	150
$V_{\beta max}$	2.5V	f_{LP}	16Hz
K_{TI}	1/80		

TABLE 4.3 COMPONENT VALUES OF THE DVR

Parameter	Value	Parameter	Value
L	1mH	C	9.4 F
R_1	30k	C_1	22 F
R_2	300k	C_2	2.2 F
R_f	10k	C_f	2.2 F
R_c	20k	C_{dc}	1.36mF

B. Small Signal Modeling:

Fig. 4.5 shows the small-signal model of the outer loop. It consists of the transfer characteristics of the inner loop, inverter, PLL, and power-flow controller. As the inner loop has much faster dynamic response than the outer loop, the small-signal transfer function of the inner loop is unity. The transfer function of the inverter describes the small-signal behaviors between β and V_{dc}. The functional blocks of power stage and controller are derived as follows.

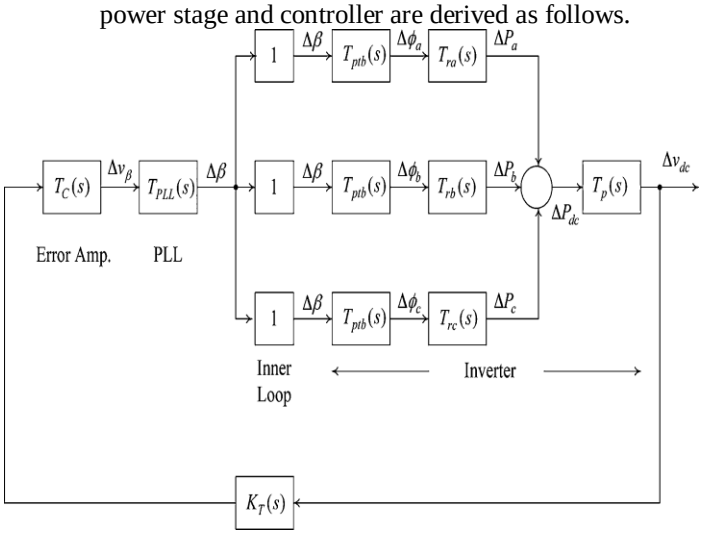


Fig.4.5. Small-signal model of the outer loop

1) Relationship Between V_{dc} and P_{dc}: The small-signal dclink voltage to dc-power-transfer function Tp (s) is as follows:

$$T_p(s) = \frac{\Delta v_{dc(s)}}{\Delta p_{dc(s)}} = \frac{2}{sc_{dc}v_{dc}} \quad \ldots 4.25$$

Where V_{dc} is the steady-state values of V_{dc}.

2) Relationship between Power Flow and the Phase of V_d With Respect to io,n in Each Phase: The small-signal DVR phase- to-power transfer function Tr,n (s)

$$T_{r,n}(s) = \left[\frac{\Delta p_n(s)}{\Delta \varnothing_n(s)}\right] = -v_{d,n}i_{o,n} \quad \ldots 4.26$$

Where Vd is the steady-state values of vd .

3) Phase Transformation Between β and φ in Each Phase: The transfer function Tpt,n (s) representing the transformation between β and φ is

$$T_{pt,n} = \left[\frac{\Delta \varnothing_n}{\Delta \beta_n}\right] = \frac{v_{s,n}}{v_{d,n}} \frac{v_{s,n} - v_{o,n}\cos\beta}{\sqrt{v_{o,n}^2 + v_{s,n}^2 - 2v_{o,n}v_{s,n}\cos\beta}}$$

...4.27

Where Vs , Vo , and B are the steady-state values of vs , vo , and β, respectively.

4) Phase Transformation Between β and vdc in Inverter: The transfer function Tinv (s) of the inverter is as follows [19]–[22]:

$$T_{inv} = \left[\frac{\Delta v_{dc}(s)}{\Delta \beta(s)}\right] = -\frac{2}{sC_{dc}v_{dc}}\left\{v_{s,a}i_{o,a}\cos\alpha_a + v_{s,b}i_{o,b}\cos\alpha_b + v_{s,c}i_{o,c}\cos\alpha_c\right\}$$

...4.28

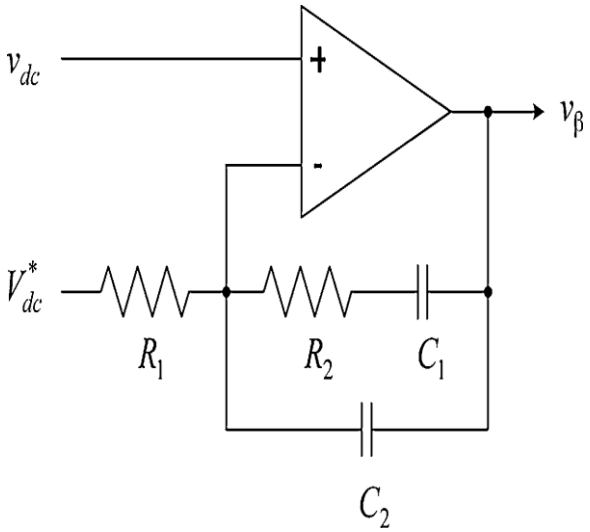


Fig.4.6. Circuit schematic of the power-flow controller

5) PLL: The PLL consists of three components, including the phase detector (PD), loop filter (LF), and the voltage controlled oscillator (VCO) [27].Based on the small-signal model of the PLL is as follows:

$$T_{PLL}(s) = \frac{\Delta\beta(s)}{\Delta v_\beta(s)} = \frac{T_{VCO}(s)F_C(s)}{1 - T_{VCO}(s)T_{pd}(s)F_L(s)} = A\frac{\omega_n^2}{s^2 + 2\xi\omega_n + \omega_n^2}$$

…4.29

Where $A = -(R_l / (R_c K_{pd}))$; $\xi = 0.5 (\sqrt{\tau K_{pd} K_l K_{vco}})$; $\omega_n = \sqrt{(K_{pd} K_l K_{vco}/\tau)}$ …4.30

K_{pd},K_1,K_{vco} are the constant gains of PD, LF and VCO, respectively.

1. Power-Flow Controller:

The function of the power-flow controller is to regulate vdc at the reference voltage V_{dc}, which is determined by the voltage ratings of the capacitor and the switches. Charging or discharging the capacitor Cdc is achieved by adjusting φn in three phases individually. The regulation action is performed by the error amplifier shown in Fig. 4.6. The transfer function TC (s) can be shown in (Eq.4.29-4.30), at the bottom of the page.

4.4. SIMPLIFIED DESIGN PROCEDURES:

The values of L, C, and Cdc in the inverter, R1 , R2 , C1 , and C2 in the power-flow controller are designed as follows.

A. Design of L and C in the Inverter:

The values of L and C in the output filters are determined by considering the maximum voltage drop across the inductor vL, D at the maximum line current Io, max, angular line frequency ω, maximum ripple current I ripple , and angular switching frequency ωsw . As most of the load current is designed to flow through L, the value of L is determined by considering that its voltage drop vL, D is small at the maximum line current Io, max.

Thus

$\omega L I_{o,max} < \upsilon_{L,D} = L < (\upsilon_{L,D}/\omega I_{o,max})$ …4.31a

As the inverter output consists of high-frequency harmonics, the fundamental component of the ripple current through the filter is designed to be less than I ripple. For the sake of simplicity In the calculation, the load impedance at the switching frequency is assumed to be infinite.

Thus

$$\frac{2v_{dc}}{\pi}\frac{1}{\omega_{sw}L-\left(\frac{1}{\omega_{sw}C}\right)} < I_{ripple} \;\&\; C > \frac{1}{\omega_{sw}\left(\omega_{sw}L-\left(\frac{2v_{dc}}{\pi I_{ripple}}\right)\right)}$$

…4.31(b)

The nominal switching frequency is chosen to be a few hundred times the line frequency. vL,D is chosen to be 1% of the line voltage, and Iripple is chosen to one half of the peak of the line current. As shown in Table I, ωsw = 300 ω, vL,D = 2 V, and Iripple = 2.6 A for the designed prototype. Based on (Eq.4.31) and stated criteria, the values of L and C in the output filters are determined.

B. Design of Cdc in the Inverter:

The value of C_{dc} is determined by

$$c_{dc} = \frac{4(v_{o,nor} - v_{s,min})(i_{o,a}\cos\theta_a + i_{o,b}\cos\theta_b + i_{o,c}\cos\theta_c)t_{res}}{v_{dc,ref}^2 - 8(v_{o,nor} - v_{s,min})^2}$$

…4.32

Where vo, nor and vs, min are nominal value of load voltage and minimum voltage of supply voltage in specification, respectively, tres is duration of restoration.

C. Design of R1 , R2 , C1 , and C2 in the Power-Flow Controller:

The pole and zeros are designed as follows:

$\log \omega_p = \text{Log } \omega_{z2} - (\psi/20)$ …4.33

Typically, ψ = 20 is chosen, and the ratio of ωz1 and ωz2 is chosen to be at least 100, in order to avoid overlapping in the two zeros.

Therefore

$\log \omega_z = \log \omega^2_z - 2$ …4.34

Based on Eq. (4.35)–(4.37), R1 , R2 , C1 , and C2 are designed by putting a value into one of them. The practical simulation model of DVR is shown in Fig 4.9. The loop gain TOL(s), it is based on the specifications and designed component values listed in Tables 4.2 and 4.3. The bode plot shows operation range, the frequency between ωcross, min, and ωcross, max within the stable regions. Based on Eq. (4.30), we have

$\omega_{z1} + \omega_{z1} = (1/R_2C2) + (1/R_2C_1) + (1/R_1C_2)$ …4.35

$\omega_{z1} * \omega_{z1} = (1/R_1\ R_2\ C_1\ C_2)$ …4.36

$\omega_P = (C_1 + C_2)/(C_1\ C_2\ R_1\ )$ …4.37

4.5 RESULT ANALYSIS OF A FAST DYNAMIC CONTROL SCHEME FOR CAPACITOR-SUPPORTED INTERLINE DYNAMIC VOLTAGE RESTORER

4.5.1. Harmonic Distortions:

When large amount of loads are added or removed at the load centre's a dip in voltage level will take place and that can abrupt performance of the customer's equipment. The above mentioned are two major power quality issues that existing in the power systems. Due these effects the total harmonic distortion that is transmitted in the line is 33.54% for one complete cycle of the waveform and the transmitted signals will affect the performance of the line as shown in the fig.4.7.

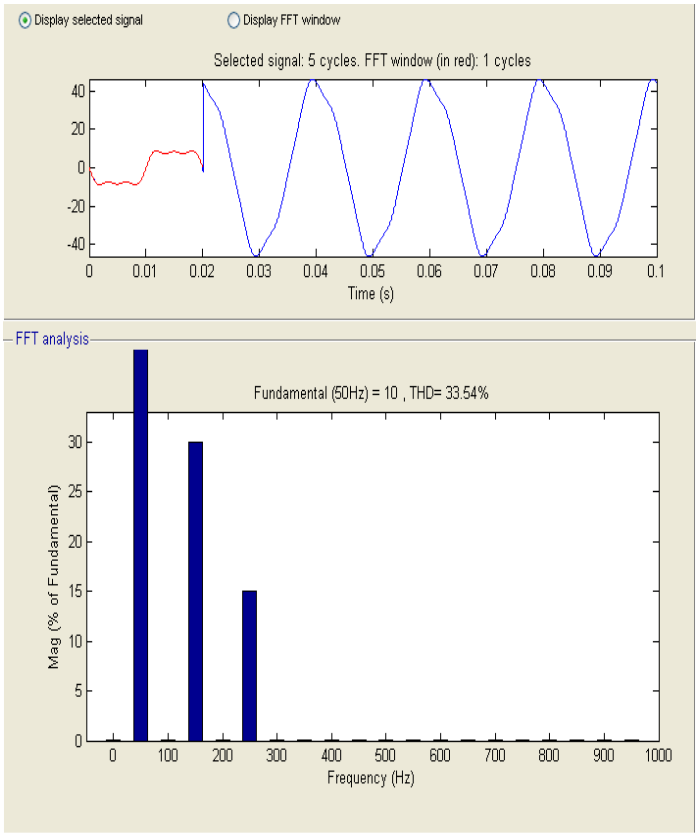


Fig. 4.7 The voltage and harmonic analysis of waveform without DVR

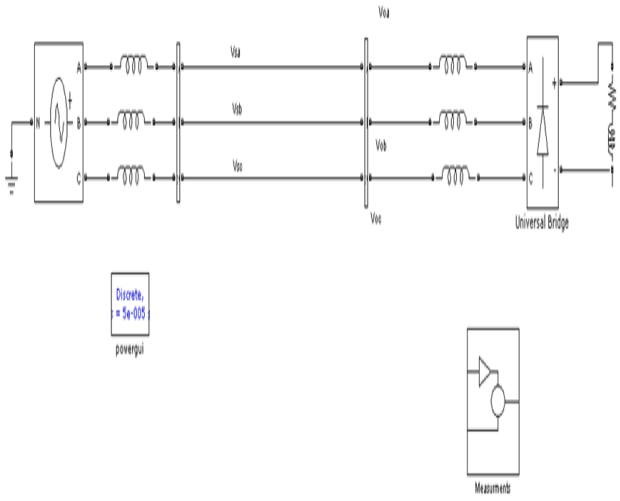


Fig.4.8 Simulation model without DVR

When large amount of loads are connected the dip in voltage will rise which can be reduced by using a dynamic voltage restorer. The sag that is reduced by using the DVR is shown in the below fig.4.9. The storage element in the DVR i.e. capacitor stored energy will be used to bounce back the sagged phases to nominal values and the total harmonic distortion can be reduce to1.37% from a value 33.54% as shown in fig 4.9.

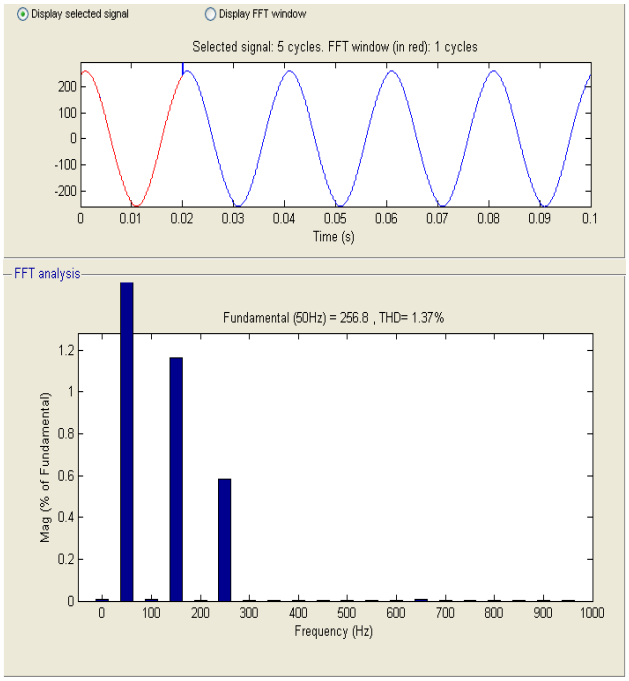


Fig.4.9 The voltage and harmonic analysis of waveform with DVR

The voltage sag and swell cases that are compensated by the dynamic voltage restorer are shown in the fig. (4.11-4.14)

4.5.1. Voltage Sag:

The voltage sag effected on single and three phase conditions are shown in the fig.4.11-4.12 where the supply voltage is reduced from a value of V_s=220V rms to 120V rms i.e. the percentage of sag that resulted is around 45%. When a sag occurs in the voltage then outer control loop and inner control loop will initiate to release the energy stored in the capacitor to restore the supply voltage to nominal value. The voltage sag is compensated with the transition time 250µsec to 180µsec.

4.5.2. Voltage Swell:

The voltage swell effected on single and three phase conditions are shown in the fig.4.13-4.14 where the supply voltage is increased from a value of Vs=220V rms to 260V rms i.e. the percentage of swell that resulted is around 19%. When a voltage swell occurs in the voltage then outer control loop and inner control loop will initiate to charge the capacitor to restore the supply voltage to nominal value. The voltage swell is compensated with the transition time of 180µsec.

The dynamic voltage restorer provides the compensation to the harmonics contents, voltage sag and voltage swell cases.

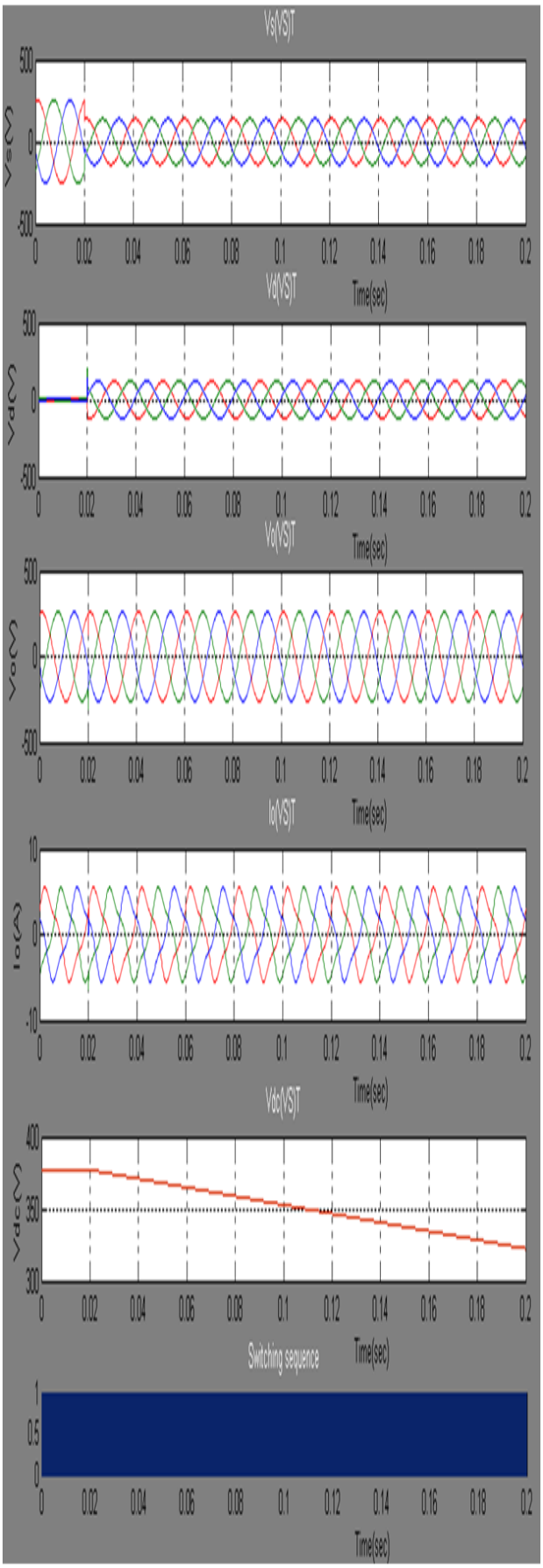


Fig.4.11 Waveforms at three sagged phases under condition. $V_{s,a}$, $V_{s,b}$, and $V_{s,c}$ are changed from 220 to 120 V_{rms} .

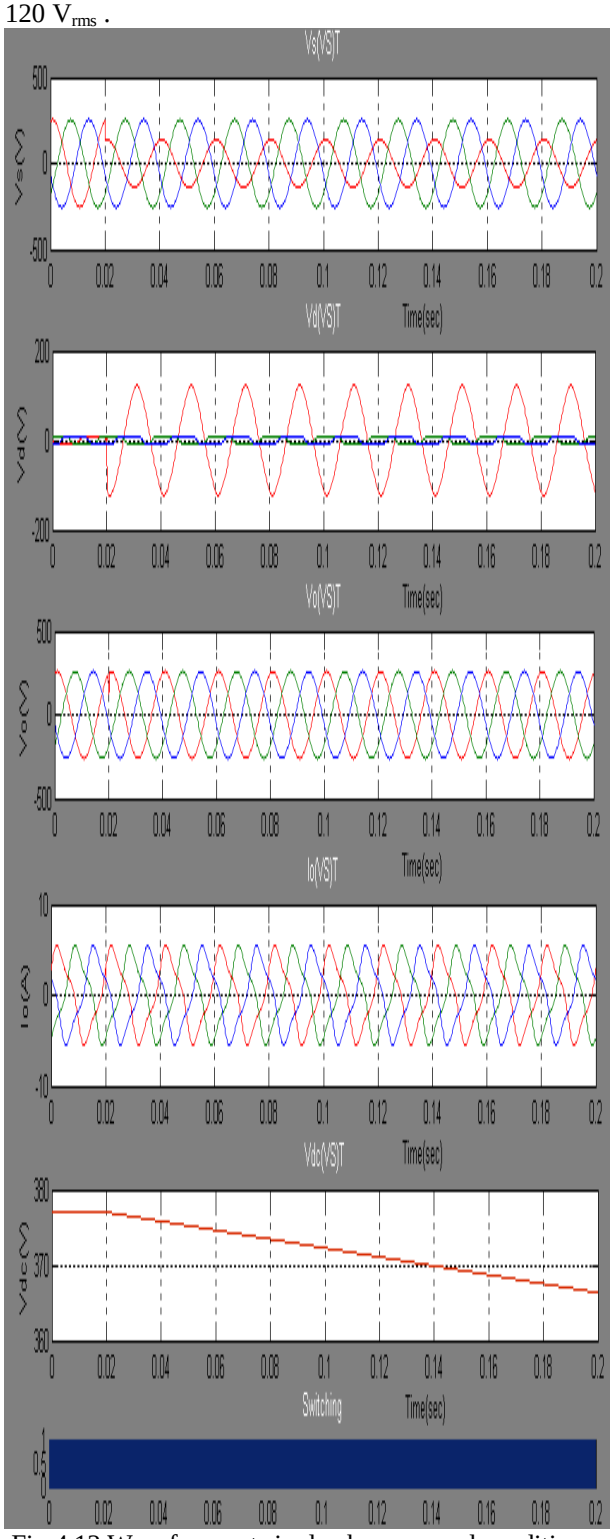


Fig.4.12 Waveforms at single phase sagged condition: $V_{s,a}$ is changed from $220V_{rms}$ to $120V_{rms}$.

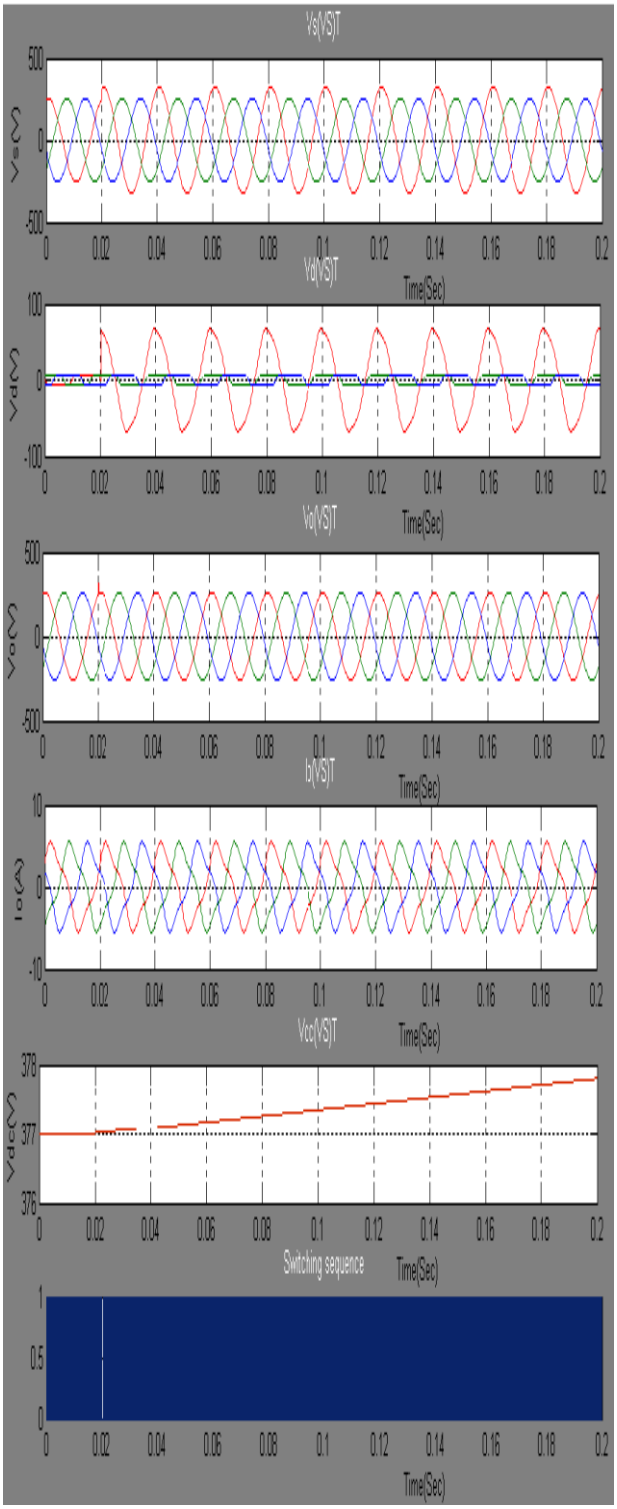


Fig.4.13 Waveforms at single phase swell condition. $V_{s,a}$ is changed from $220V_{rms}$ to $260V$ V_{rms}

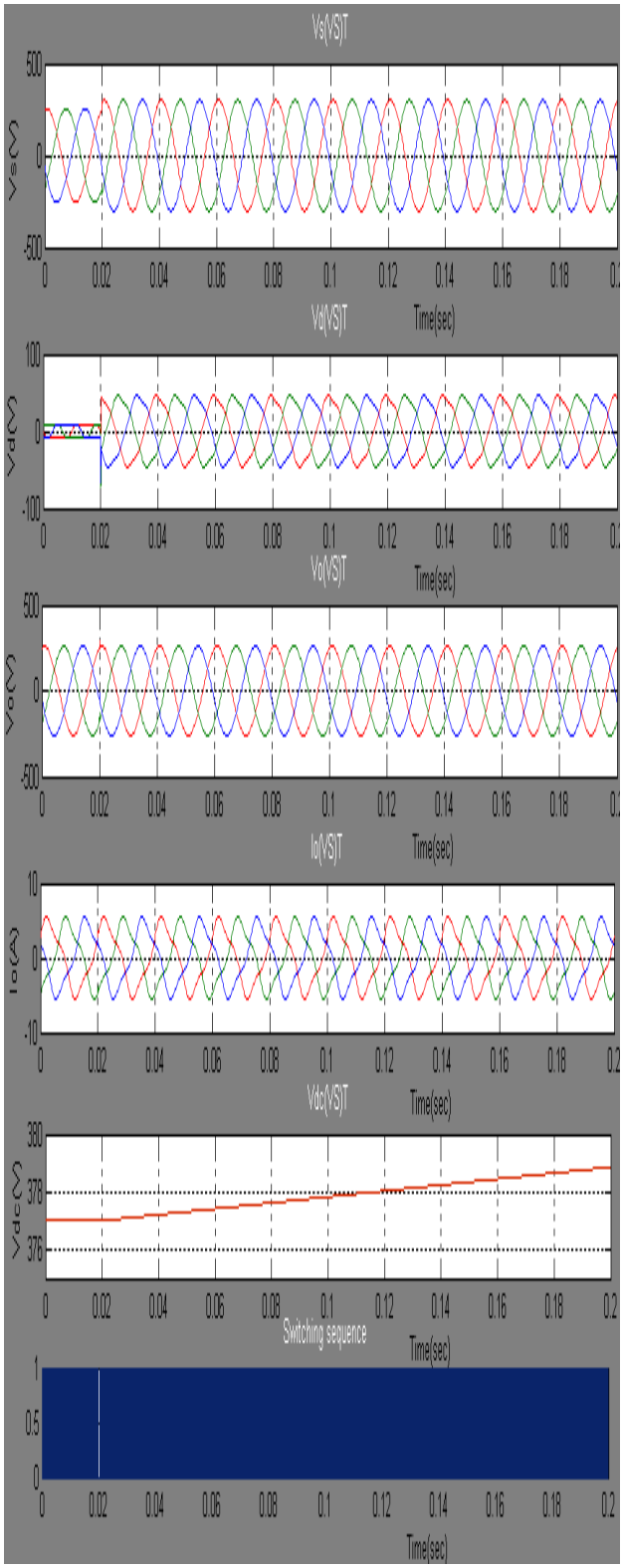


Fig.4.14 Waveforms at three swell conditions. (a) $V_{s,a}$, $V_{s,b}$, and $V_{s,c}$ are changed from $220V_{rms}$ to $260V_{rms}$.

4.6. COMPARISION OF RESULTS WITH AND WITHOUT DVR:

The effect of voltage sag and swell has a greater impact on the power that is transmitted from sending end to recieveing end. The real power that is transmitted gets varied due to the addition of more

non-linear loads or sudden shutdown of large rating loads. The voltage sag and swell cases cause customer appliances to get abrupt by reducing their life span. The power quality at the load centre are mostly electonic switched ones, so due to the switching actions of these non-linear loads the level of harmonics injected into the supply will be more and the cost of the capacitors required to compensate the harmonics will increase there by increasing the overall cost.

When an automatically controlled regulators are used then the chances of overcoming the voltage sag or swell cases can be aoided. The dynamic voltage restorer operates at desired levels to regulate voltages as well as eliminates the harmonics. The entire mechanism uses capacitor banks to restore the voltage to nominal values and the energy stored in the capacitor can be charged from the supply it self. Under normal operated conditions the MOSFET switches which operate at 10 KHz frequency nor inject nor charge the capacitor. When a voltage sag occur the stored enrgy restores the voltage to nominal value by discharging the energy. When a voltage swell occur in any of the phases, the capacitor uses the swelled phase to charge its energy to bounce to normal full capacity.

The total harmonic content that will be available when a power system is operated under sagged condition will be 33.54% i.e without using the DVR. When a DVR is used in to back up the sagged voltage to nominal value it also eliminates the total harmonic content to a lower value lessthan 6%.

VI. CONCLUSION

In this project simulation of various custom power devices i.e. DVR, DSTATCOM, for mitigation of voltage sags and swells are modeled and simulated in matlab/simulink. An industrial system test system with Induction motor and sensitive loads are simulated in PSACD/EMTDC and it shows that due to the presence of induction Motors in the system , the voltage at the sensitive load cannot reach its rated value instaneously after the fault is cleared. Starting of Induction motors causes voltage at the sensitive loads connected system , it can be eliminated by starting the induction the Induction motor wth starters. Faults are the main causes of the voltage sags . Custom power devices DVR, DSTATCOM which uses inverter topology are simulated for different sag and swell conditions and it has shown that DVR can mitigate up to 50% of sag for DC voltage(V_{DC} =5KV, 60% of sag for V_{DC} =7KV , 70% of sag for V_{DC} =10KV. A 12 pulse DVR generates less harmonics than a 6 pulse DVR and at the 12 pulse DVR can mitigate sags due to unbalanced faults. DSTATCOM can mitigate voltage sags up to 80% due to three phase faults with V_{DC} =50KV and voltage sags up to 30% due to Sudden load switching with V_{DC} =19KV. It is shown that for the same voltage sag compensation DVR requires less energy than DTATCOM.

A new Voltage sag mitigation topology called pwm switched auto transformer is modeled and simulated with peak and RMS voltage as a reference. This topology requires only one PWM switch per phase as compared to DVR or DSTATCOM requires two switches per phase. The PWM switched auto transformer does not require energy storage device for mitigation of voltage sag as compared to DVR and DSTATCOM requires energy storage elements..

Scope of Future Work

- Hardware Implementation of PWM Switched Auto Transformer for closed loop control for voltage sag/swell mitigation has to be done.

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