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Comparative Study of Different Types of Full Adder Circuits

Sansar Chand Sankhyan
Department of EECE ITMU, Gurgaon

ABSTRACT
The 1-bit full adder circuit is one of the most important components of any digital system applications. The power-delay product is a measurement of the energy expanded per operational cycle of an arithmetic circuit. In this we have discussed about the various types of full adders. Also reviewed about the average power and delay of various types of 1 bit full adders.and at last we concluded that which is the low power consuming and more speed giving I bit full adder design.
KEYWORDS: Full-adder, High performance, MUX, Low-power, PDP, XOR

I. INTRODUCTION

Full Adder

A **full adder** adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A,B, and C_{in}; A and B are the operands, and C_{in} is a bit carried in from the next less significant stage.[2] The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The circuit produces a two-bit output, output carry and sum typically represented by the signals C_{out} and S, where $\mathrm{sum} = 2 \times C_{out} + S$. The one-bit full adder's truth table is:

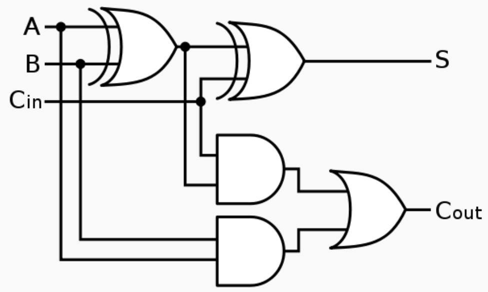

Fig 1: block dagram of 1 bit full adder

Input			Output	
C	B	A	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates. One example implementation is with $S = A \oplus B \oplus C_{in}$ and $C_{out} = (A \cdot B) + (C_{in} \cdot (A \oplus B))$.

II. DIFFERENT TYPES OF FULL ADDERS

2.1 2MB12T [4]

This full adder has been implemented using six multiplexers and 12 transistors. Each multiplexer is implemented by pass-transistor logic with two transistors. As shown in Fig. 1, there is no VDD or GND connection in this circuit and there are some paths containing three serried transistors. It causes to increase delay of producing SUM signal. The size of each transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP. Therefore, the area of the circuit is increased.

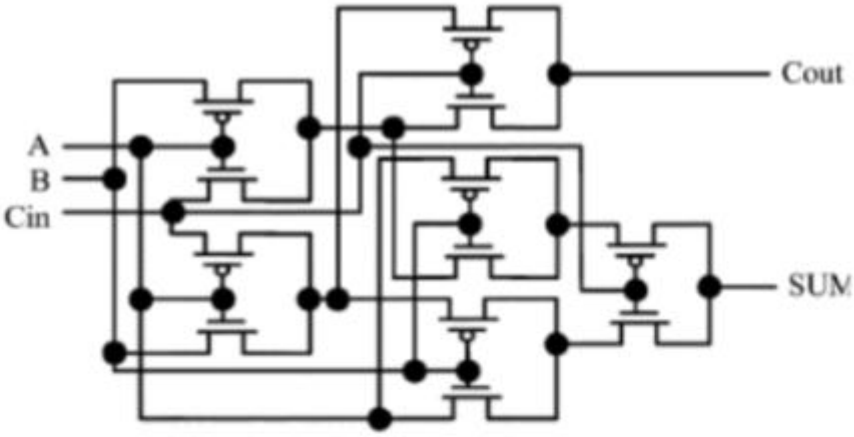

Fig 2.1 MB12T has been implemented using six multiplexers and 12 transistors[4]

2.2 Improved 14T full adder [6]

An improvement from 14T [6] has simultaneous XOR and XNOR signals. Feedback transistors provide rail-to-rail outputs in XOR-XNOR module.

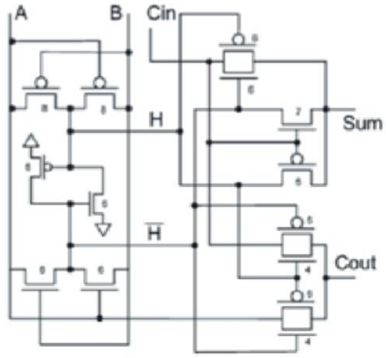

Fig 2.2 An improvement from 14T [6]

2.3 16T full adder [7]

It shows another improved version from 14T, which is called 16T [7]. It is the same as New-14T in terms of the output modules. However, the XOR-XNOR module has been modified to reduce delay and power consumption. The XOR-XNOR modules does not have full-swing outputs thus, the transistors which have been connected to this module are turned on or off slowly.

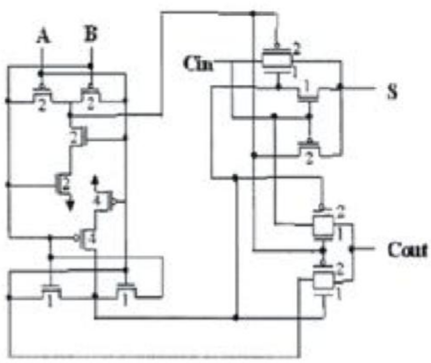

Fig 3 : 16T[7] 1 bit full adder Full adder

2.4 10T bit full adder [3]

A full adder in form of centralized structure is made by ten-transistor-10T [3] is shown in Fig. 4. As shown in Fig.4 SUM and COUT are generated using two double transistors multiplexers. 3T XOR and XNOR consume high energy due to short circuit current in ratio logic. Maximum serried transistors here are two transistors while in MB12T are three transistors

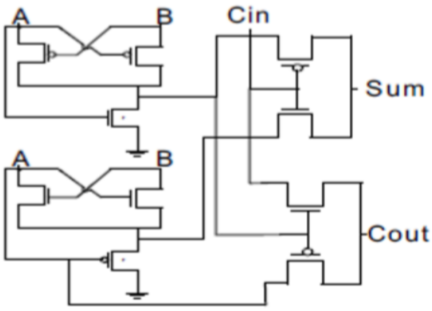

Fig 4.4 10T 1 bit full adder [3]

2.5 8T full adder [5]

The design of proposed full adder is based on three transistor XOR gate and 2-to-1 multiplexer with 8 transistors in total. It acquires least silicon area. The design of 3T XOR gate is shown in Fig.8. The heart of the design is based on a modified version of a CMOS inverter and a PMOS pass transistor. With this design a significant improvement in delay.

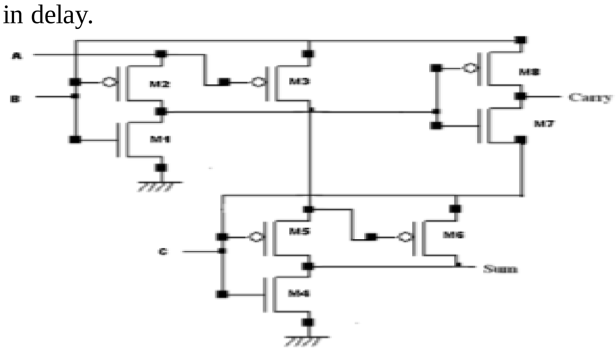

Fig 5.5 Schematic Model of 1-bit Full-adder cell using 8- Transistor [5]

III. DESIGN SIMULATION AND SIMULATION RESULTS

Table 2 : Comparison of different 1 bit full adders in terms of power , delay and area

Types of adder	Technology (nm)	Average Power (μW)	Delay (ps)	PDP (10-18J)	Area (μm2)
2 8T[1]	180	3.87	48.472	187.586	7.3
16T[7]	180	2.33	39.412	91.82	4.3
12T[4]	180	5.19	27.372	142.06	3.9
10T[3]	180	1.3	40.481	52.625	3.5
8T[5]	180	1.129	11.512	12.997	2.9

IV. TECHNOLOGY USED

Cadence virtuso is used for all the simulation work

V. CONCLUSION

All types of design parameters for full adder circuit are studied. But 8t full adder is best among all. The 8T 1 bit full adder is found to give better performance in power delay product parameter among all the adders mentioned in the comparison done. In This circuit design buffering circuit is added in the basic full adder design which results in the lesser use of transistors and due to which the area consumption reduces. Here in 8T full adder design the driving capability is improved that leads to operating capability at lower voltages and offers faster operating speed as the delay is reduced. So it is concluded here that 8T full adder design is best suited for the applications where lesser chip area, less power consumption and higher speed is needed.

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