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Embedded Multi-Resolution Signal Tracing For Amba Ahb With Real Time Lossless Compression

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ABSTRACT
AHB Bus Tracer is a significant infrastructure that is needed to monitor the on chip-bus signals, which is vital for debugging and performance analysis and also optimizing the SOC. Basically on chip signals are difficult to observe since they are deeply embedded in a SoC and no sufficient I/O pins are required to access those signals. Therefore, we embed a bus tracer in SoC to capture the bus signals and store them.
In this paper a multiresolution AHB On-Chip bus tracer is proposed for system-on-chip (SoC) debugging and monitoring which is capable of capturing the bus trace with different resolutions and efficient built-in compression mechanisms. Subsequently compression of the trace without any loss of the actual trace which when reconstructed at the analyzer will remain the same. The trace data will be decompressed on the host for further observation and debugging. The experimental results show that the proposed approach was designed successfully; the RTL simulations were performed successfully along with successful synthesis using Xilinx ISE.
Keywords: AMBA, AHB Bus Tracer, Real Time Compression**,** multi-resolution, signal tracing.

I. INTRODUCTION

The AMBA-AHB defines a point to point interface between two communicating entities such as IP cores and bus interface modules. One entity acts as a master of the AMBA-AHB instance, and the other as a slave. Only the master can present commands and is the controlling entity. The slave responds to commands presented to it, either by accepting data from the Master, or presenting data to the master.

In the System-on-a-Chip (SoC) era, it is a challenge to verify and debug system chip efficiently and rapidly. For design verification and debugging at system level and chip level, not only external I/O signals observation, but also internal signals tracing can help designer to efficiently analyze and verify the design such as the software program, hardware protocol, and system performance. SoC bus signal tracing can be accomplished with either software or hardware approaches. The software approach trace only program address, and the cost of hardware implementation of software approaches would be high. On the other hand, the hardware approach can trace signals at the target system directly. However, the main problem with hardware-based tracing techniques is that the cycle based traces size is usually extremely large.

Therefore, in order to reduce the trace size the compression of the trace is necessary. In order to achieve high trace compression ratio the bus tracer adopts trace compression mechanisms. It supports multi resolution tracing by capturing traces at different timing and signal abstraction levels. It also provides the dynamic mode change feature to allow users to switch the resolution on-the-fly for different portions of the trace to match specific debugging/analysis needs. This feature provides a more flexible tracing to focus on the interesting points.

II. RELATEDWORK

The spirit of a hardware tracer is its data reduction or Compression technique. There are hardware approaches to compress the trace, which can be divided in lossy and lossless categories. Some appropriate compressing methods have been available for different types and parts of bus signals. Branch/target filtering is one common technique for program address compression. This approach has been used in some commercial processors, such as TriCore and ARM's Embedded Trace Macrocell.Thehardware overhead of these works is small since the filtering mechanism is simple to implement in hardware. However, the effectiveness of these techniques is mainly limited by the average basic block size, which is roughly around four or five instructions per basic block, as reported in and for data address and value tracing, the most popular method is used the differential approach based on subtraction. Some researches have shown that using the differential method can reduce the data address and data values traces by about 40 percent and 14 percent respectively. Besides the address and data bus, there are several control signals on system bus

that need to be traced. Some FPGA boards have built-in signal trace tools, such as the Altera Signal Tap and Xilinx Chip- Scope.

FS2 AMBA Navigator supports bus clock mode and bus transfer mode to trace bus signals on every clock and bus transfer respectively. Trace buffer stores bus cycles or bus transfers based on local internal memory size. Although these approaches support multiple trace modes such as tracing at cycle by-cycle or at signal transaction, only one mode can use during a tracing
process. This paper presents the multi-resolution approach that can use different trace modes during a bus signal tracing process.

III. AMBA BUS TRACER ARCHITECTURE

This section presents the architecture of our bus tracer. Shown in Fig.1 is the bus tracer overview. It mainly contains four parts 1)Event Generation Module 2)Abstraction Module 3)Compression Modules and 4) Packing Module. The Event Generation Module controls the start/stop time, the trace mode, and the trace depth of traces. The signal Abstraction module traces the corresponding AHB signals at proper time according to user configuration. The trace compression module compresses the trace data in accordance with signal characteristics. Finally, in the data packing module, the trace data is arranged compactly for output to the internal on-chip trace memory or external off-chip storage. When the onchip trace memory is full, it sends an interrupt to the microprocessor then this processor reads the data from the trace memory and transfers the trace data to off-chip storage through AMBA.

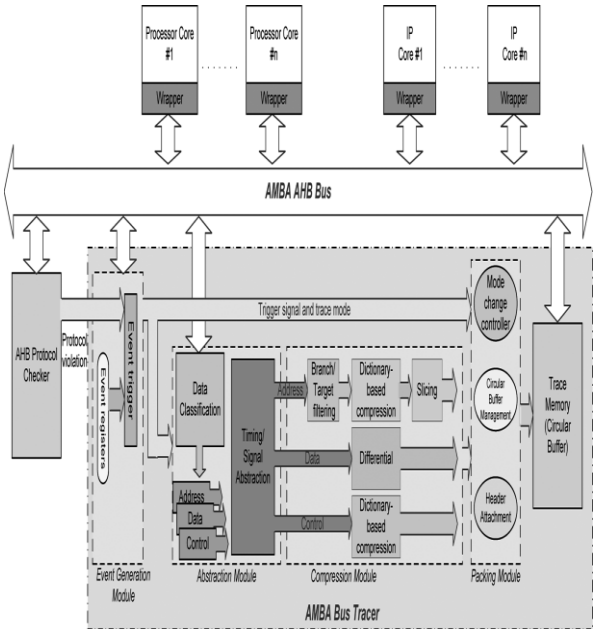


Fig.1.Multiresolution Bus Tracer Block Diagram

The transaction-level debugging provides software and hardware designers a common abstraction level to diagnose bugs. The abstraction level is in two dimensions timing abstraction and signal abstraction. The timing dimension has two abstraction levels which are the cycle level and transaction. level. The cycle level captures the signals at every cycle. The transaction level records the signals only when their value changes.

The signal dimension involves grouping of AHB bus signals into four categories: program address, data address/value, access control signals (ACS), and protocol control signals (PCS). Then, we define three abstraction levels for those signals. They are full signal level, bus state level, and master operation level. The full signal level captures all bus signals. The bus state level further abstracts the PCS by encoding them as states according to the bus-state-machine (BSM).The states represent bus handshaking activities within a bus transaction. The master state level further abstracts the bus state level by only recording the transfer activities of bus masters and ignoring the handshaking activities within transactions. This level also ignores the signals when the bus state is IDLE, WAIT, and BUSY. The BSM is designed based on the AMBA AHB 2.0 protocol to represent the key bus handshaking activities within a transaction. The transitions between BSM states follow the AMBA protocol control signals. Combining the abstraction levels in the timing dimension and the signal dimension.

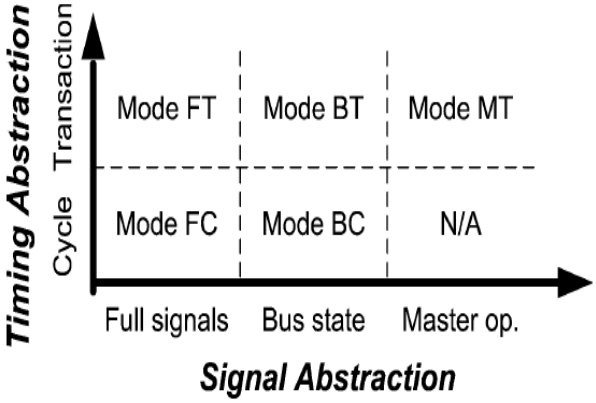


Fig.3. Debugging/monitoring process with DMC

1. Event Generation Module: The Event Generation Module decides the starting and stopping of a trace and its trace mode. The module has configurable event registers which specify the triggering events on the bus and a corresponding matching circuit to compare the bus activity with the events specified event registers. Event register contains four parameters: the trigger conditions, the trace mode, the trace direction, and the trace depth. The trigger conditions can be any combination of the address value, the data value, and the control signal values

32 bits					
Address					
Address Mask					
Data					
Data Mask					
Control					
Control Mask					
Trace Depth					
Trace Mode(4bits)	Direction	Enable	AHB Bus	Checker Event	Event Numbers (24 bits)
Event Numbers(21 bits)					[10:0] zeros

Fig. 3. Event register

2. Abstraction Module: The Abstraction Module monitors the AMBA bus and selects/filters signals based on the abstraction mode.

In abstraction mode we provide five modes in different granularities. They are Mode FC (full signal, cycle level), Mode FT (full signal, transaction level), Mode BC (bus state, cycle level), Mode BT (bus state, transaction level), and Mode MT (master state, transaction level).

At Mode FC, the tracer traces all bus signals step by step so the detailed bus activities can be observed. At Mode FT, the tracer traces all signals only when their values are differed.

At Mode BC, the tracer uses the Bus State Machine, such as NORMAL, IDLE, ERROR, and so on, to represent bus transfer activities in cycle changing level. Comparing to mode FC designers can observe the bus handshaking states without analyzing the detail signals.

At Mode BT, the tracer uses bus state to represent bus transfer activities in transaction level Our bus tracer also supports dynamic mode change (DMC) feature which allows designers to change the trace mode dynamically in real-time.

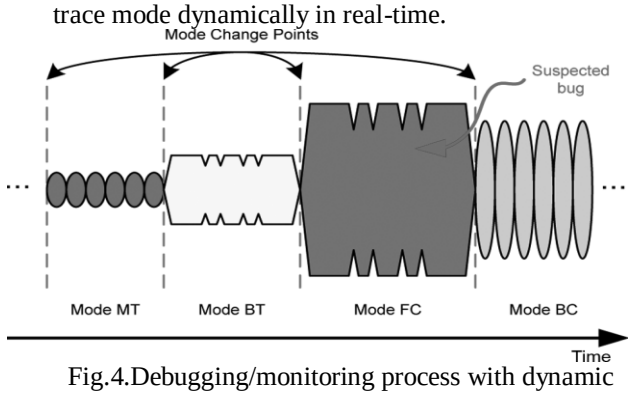


Fig.4.Debugging/monitoring process with dynamic mode change

3. Compression Module: The purpose of Compression Module is to reduce the trace size. It accepts the signals from the abstraction module. To achieve real time compression, the Compression Module is pipelined to increase the performance.

4) Packing Module: The Packing Module is the last phase. It receives the compressed data from the compression module, processes them, and writes them to the trace memory.

Fig.5.Concatenation of mode-change packet for abstraction mode switch

IV. AHB Protocol checker (HP checker)

Checker is an external module from where we can trace data other than AHB bus.

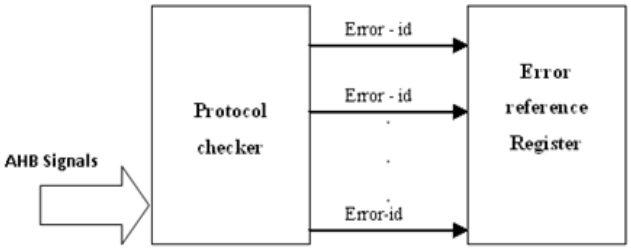


Fig. 5: Protocol Checker

HB Protocol Checker (HP Checker) architecture, contains two main function blocks: Protocol Checker, ERROR Reference.

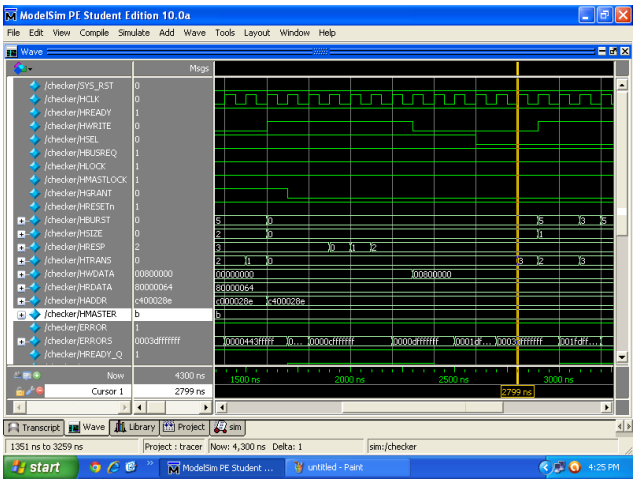
Protocol Checker is the main core of HP Checker, the inputs are all AHB bus signals, and the outputs are ERROR signals and corresponding master and slave IDs. Every rule has its own corresponded bit because every cycle maybe occur more than one error.

HP Checker is a rule-based protocol checker, thus how to establish a set of well-defined rules is very important.

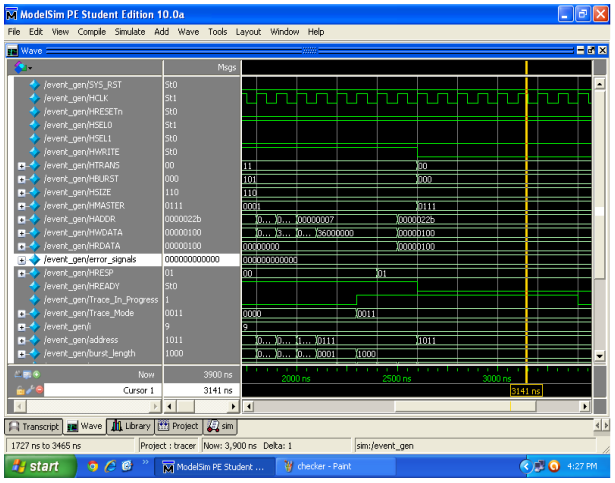
V. EXPERIMENTAL RESULTS

By simulation and synthesis the following results are obtained for each cycle at different abstraction levels. Here Modelsim tool is used in order to simulate the design and Xilinx tool for Synthesis process and the netlist generation.

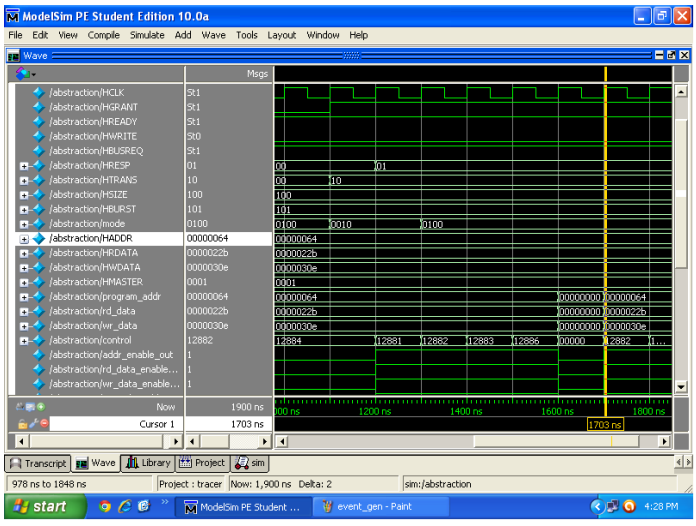
Checker Result:-



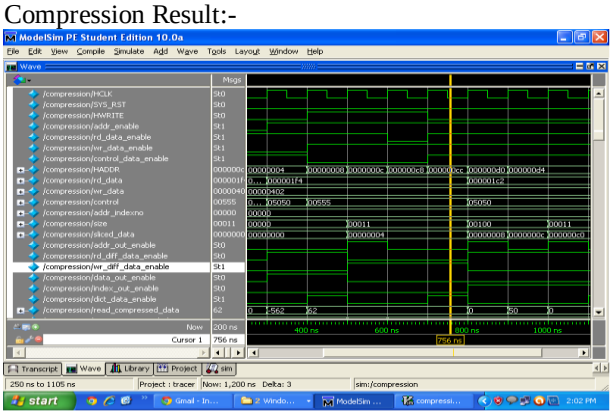
Event Generator Result:-



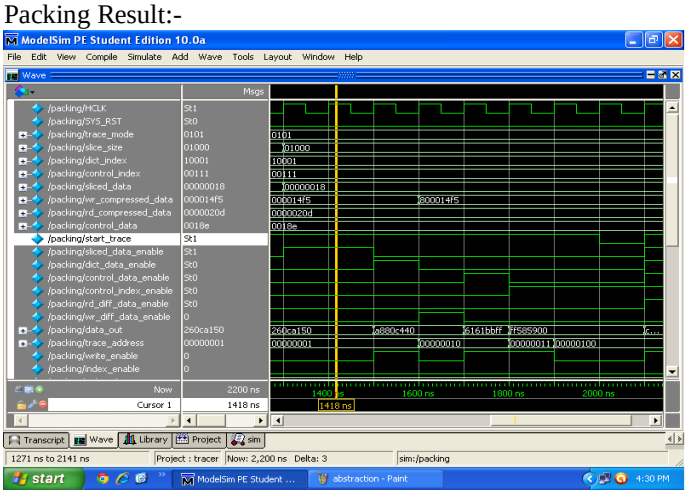
Abstraction Result:-



Compression Result:-

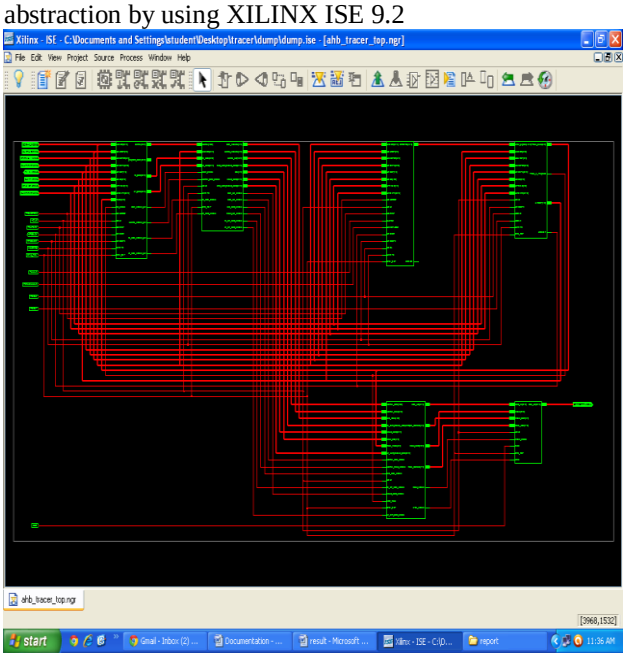


Packing Result:-



Synthesis Result:

We synthesized this code by using XILINX ISE 9.2 verification, and implementation of digital logic chips at the Register transfer level (RTL) level of abstraction by using XILINX ISE 9.2



DESIGN SUMMARY RESULT:-

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	8	1,920	1%
Number of 4 input LUTs	40	1,920	2%
Logic Distribution			
Number of occupied Slices	21	960	2%
Number of Slices containing only related logic	21	21	100%
Number of Slices containing unrelated logic	0	21	0%
Total Number of 4 input LUTs	40	1,920	2%
Number of bonded IOBs	43	66	65%
Number of GCLKs	1	24	4%
Total equivalent gate count for design	325		
Additional JTAG gate count for IOBs	2,064		

Timing Summary:-
Minimum period: 5.654ns (Maximum Frequency: 176.864MHz)
Minimum input arrival time before clock: 7.141ns
Maximum output required time after clock: 6.978ns
Maximum combinational path delay: 8.227ns

VI. CONCLUSION

AHB bus is capable of achieving high performance with a maximum frequency of 176.864MHz.The bus traces with 5 modes of resolution and the design is verified for all cases of 5 modes. With the aforementioned features, SYS-HMRBT supports a diverse range of design/debugging/ monitoring activities, including module development, chip integration, hardware/software integration and debugging, system behavior monitoring, system performance/power analysis and optimization, etc. The users are allowed to tradeoff between trace granularity and trace depth in order to make the most use of the on-chip trace memory or I/O pins.

VII. FUTURE SCOPE

In the future, we would extend this work to more advanced buses/connects such as AXI or OCP. In addition, with its real time abstraction capability, we would like to explore the possibility of bridging our bus tracer with ESL design methodology for advanced hardware/software co development/debugging/ monitoring/analysis

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