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Design and Synthesis of Bus Invert Encoding and Decoding Technique Using Reversible Logic

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ABSTRACT

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. This paper presents a bus invert coding on reversible logic using Feynman, Feynman double gate, BJN, Sayem and SCG gates. The proposed Bus-Invert method of coding the I/O which lowers the bus activity and thus decreases the I/O peak power dissipation by 50% and the I/O average power dissipation by up to 25%. Proposed circuits have been simulated using Xilinx Isim simulator and implemented using Xilinx Spartan3 FPGA platform.

Keywords **–** Reversible Logic, Circuit Design using Reversible Gates, Reversible Logic Gates, Bus invert coding**.**

I. INTRODUCTION

The Landauer [1] proposed that, for a single bit of information loss kTln2 joules of energy will dissipates, where K is the Boltzmann's constant and T is the absolute temperature at which the bit loss operation has been performed. Hence the amount of energy lost is having direct relationship to the number of bits erased during computation involving classical logic gates. Bennett [2] showed that circuits built using reversible logic gates dissipate no energy as they have theoretically zero internal power. According to Gordon Moore, the performance of integrated circuit continues to improve at an exponential rate and doubles every 18 months, hence generating a lot of heat and reducing the life of the circuit. Therefore it is impossible to design Quantum circuits without reversible gates. The classical computer consists of conventional logic gates for processing large amount of data. In conventional gates only the NOT gate is reversible gate, i.e. in which input and output are uniquely retrievable from each other.

Bus-Invert method is the one used to coding and decoding the I/O which lowers the bus activity and thus decreases the I/O peak power dissipation by 50% and the I/O average power dissipation by up to 25%. The method is general but applies best for dealing with buses. This is fortunate because buses are indeed most likely to have very large capacitances associated with them and consequently dissipate a lot of power. In previous systems the design of bus invert coding and decoding can be done using conventional logic gates. We can understood that the systems with conventional logic gates causes power dissipation and energy loss in the system [1] in order to overcome these we have to use reversible logic in the system i.e. we have to design the system with reversible logic gates. This paper will presents the bus invert coding and decoding design with reversible logic gates.

II. REVERSIBLE LOGIC GATES

For a reversible logic gate will be having a $m \times n$ function, where m = number of inputs, and n = number of outputs and it is said to be reversible if and only if m = n i.e. equal number of inputs and equal number of outputs.

A Reversible Gate will be having following requirements:

- The input vector can be uniquely determined by the output vector
- There is a one-to-one correspondence between the input and the output assignments
- There should not be a fan-out of more than one.
- Feedback is not allowed in reversible logic circuits.

In reversible logic gates, the output which is not used as a primary output or is not an input to another gate is known as a garbage output [3]. The inputs on the other hand having fixed values are known as constant inputs [4]. Hence for an optimized reversible circuit, the number of garbage outputs, the number of constant inputs and the number of reversible gates used should be a

minimum. Reversible circuits used in the domain of low power CMOS design [5], optical computing [6], quantum computing [8] and nanotechnology [7].

An m ×n reversible gate is represented using two vectors:

$I_V = (I_1, I_2, I_3.....I_m)$ and $O_V = (O_1, O_2, O_3.....O_n)$

Where I_V and O_V are the input and output vectors respectively. If m=n then the gate is reversible. There exist several reversible gates in the literature we will discuss few preferable gates required for our design.

Feynman Gate:

Feynman gate [9] is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q=A ⊕ B. It has Quantum cost one. The Feynman gate is shown in Fig. 1.

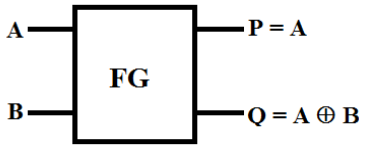

Fig. 1. 2*2 Feynman Gate

Feynman Double Gate (F2G):

Feynman double Gate (F2G) [10] is a 3*3 gate. It has A, B and C input vector and output vector as P = A, Q = A ⊕ B, and R = A ⊕ C. Quantum cost is equal to 2.The Feynman double gate is shown in Fig. 2.

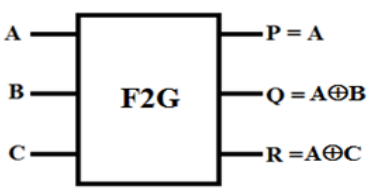

Fig.2. 3*3 Feynman Double Gate (F2G)

Sayem Gate (SG):

Sayem gate (SG) [11] is a 4*4 reversible gate. The input (A, B, C, D) and outputs P=A, Q=A'B ⊕ AC, R=A'B ⊕ AC ⊕ D and S=AB ⊕ A'C ⊕ D. Quantum cost is equal to 6.The Sayem gate is shown in Fig. 3.

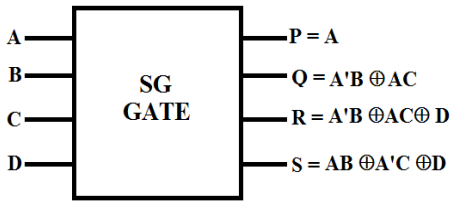

Fig.3. 4*4 Sayem Gate (SG)

BJN Gate:

BJN Gate [14] is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=B and R= (A+B) ⊕ C. Quantum cost is equal to 1. The BJN gate is shown in Fig. 4.

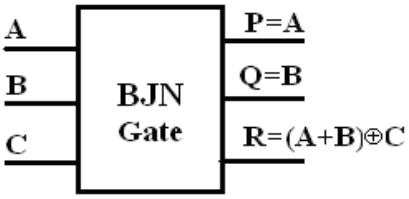

Fig. 4. 3*3 BJN gate

Modified HNG Gate:

MHNG Gate [13] is a 4*4 gate with inputs (A, B, C, D) and outputs P=A, Q=D, R=A ⊕ B ⊕ C and S=(A ⊕ B)C ⊕ AB ⊕ D. Quantum cost is equal to 5. The MHNG gate is shown in Fig. 5.

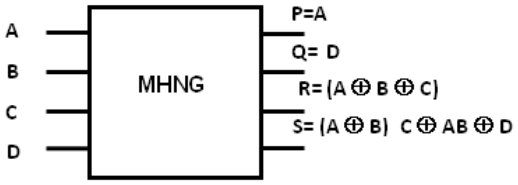

Fig. 5. 4*4 MHNG Gate

Six-correction logic Gate (SCL):

SCL [14] is a 4*4 reversible gate. The input (A, B, C, D) and outputs P=A, Q=B, R=C and S=A(B+C) ⊕ D. Quantum cost is equal to 1.The SCL gate is shown in Fig. 6

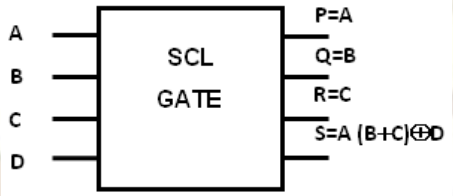

Fig. 6. 4*4 SCL Gate

III. BUS INVERT CODING

Bus-Invert method is used to coding and decoding the I/O which lowers the bus activity and thus decreases the I/O peak power dissipation by 50% and the I/O average power dissipation by up to 25% [15]. The method is general but applies best for dealing with buses. This is fortunate because buses are indeed most likely to have very large capacitances associated with them and consequently dissipate a lot of power.

Let's denote as the data value (Pd) the piece of information that has to be transmitted over the bus in a given time-slot. Then the bus value (Din) will denote the coded value (the actual value on the bus). Typically a code needs extra control bits. The Bus-Invert method proposed here uses one extra control bit called invert. By convention then invert = 0 the bus value will equal the data value. When invert = 1 the bus value will be the inverted data value.

The peak power dissipation can then be decreased by half by coding the I/O as follows (Bus-Invert method):

1) Compute the Hamming distance (the number of bits in which they differ) between the present bus value (also counting the present invert line) and the next data value by using the majority voter logic circuit.
2) If the Hamming distance is larger than n/2, set invert = 1 and make the next bus value equal to the inverted next data value.
3) Otherwise let invert = 0 and let the next bus value equal to the next data value.
4) At the receiver side the contents of the bus must be conditionally inverted according to the invert line, unless the data is not stored encoded as it is (e.g., in a RAM).

The Fig. 7, Fig. 8 and Fig. 9 shows the Bus invert encoder and decoder and majority voter logic circuits using Reversible logic gates.

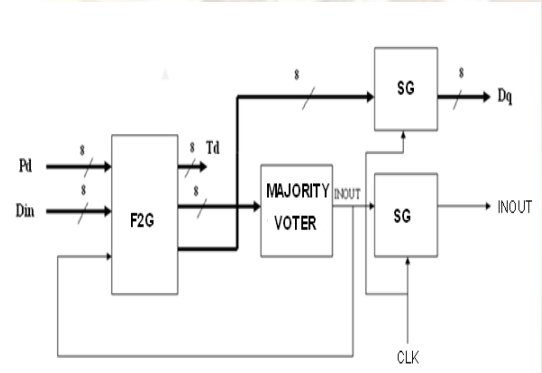

Fig. 7. Bus Invert Encoder using Reversible Logic Gates

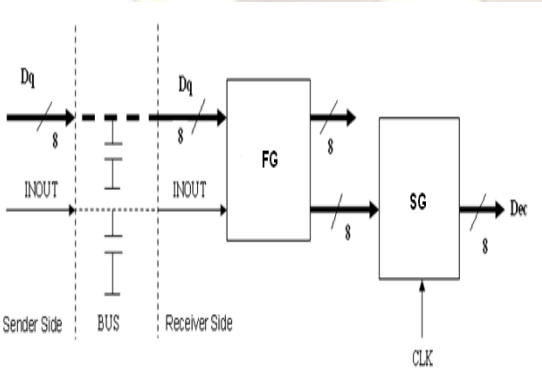

Fig. 8. Bus Invert Decoder using Reversible Logic Gates

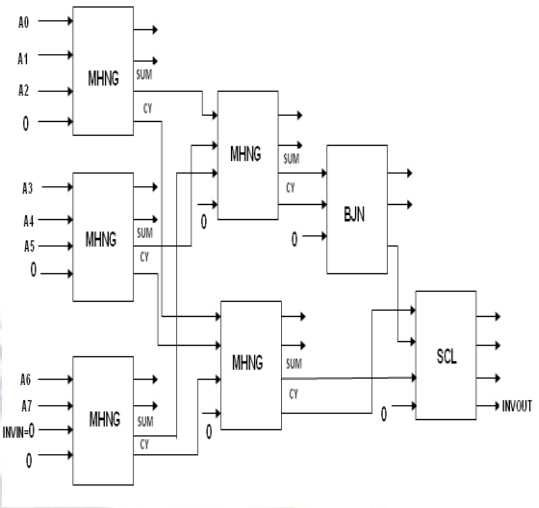

Fig. 9. Majority Voter logic circuit using Reversible Logic Gates

IV. SIMULATION RESULTS

The entire architecture is programmed using Verilog. The coding is done on Xilinx ISE12.2i on Spartan 3 using target device: XC3S50-PQ208 at speed grade of -5. Simulation can be done using Xilinx ISim simulator.

For the design of Reversible Bus Invert Encoder and Decoder we must use reversible gates such as 2*2 Feynman Gate, 3*3 Feynman double Gate , 4*4 SC Gate, 3*3 BJN Gate, 4*4 Sayem Gate and 4*4 Six-correction logic gate. The Fig. 10 Shows simulation results of Bus invert coding circuit using reversible gates.

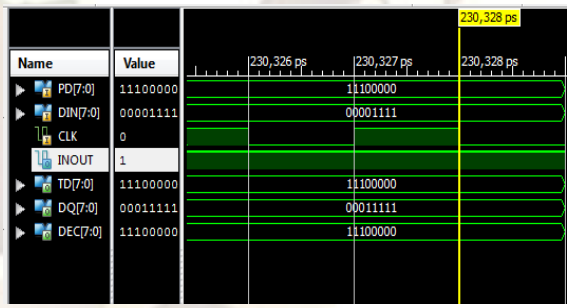

Fig. 10. Simulation result of Bus invert coding using Reversible gates

V. CONLUSION AND FUTURE WORK

Reversible logic is becoming the modern way of digital circuit designing. Here in this paper we have tried to attain bus invert coding circuit by using some of the basic reversible gates. This design can be employed in low power logical design applications. Although the Bus Invert method was explained in the particular setting of dynamic I/O power dissipation the same methods can be applied in any case where large capacitances are involved. Furthermore it is likely that the method will also

reduce the total I/O overlap current. Both the driver and the receiver on the bus must use the bus invert method in order to code and decode correctly the information on the bus.

In the future we plan to apply coding in the particular bus invert method in some practical application. We also plan to further study the theory of limited weight codes and in particular their relationship to error correcting codes. As a last comment, it is interesting to mention that the bus invert method decreases the total power dissipation although both the total number of transition and the total capacitance.

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