

## **Design of an Implicit Pulse Triggered Flip-Flop Using PTL Based and Logic for Space Applications.**

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### **ABSTRACT**

In this paper, a novel low-power pulse-triggered flip-flop (FF) design for space applications is presented. In this the clock generation circuitry an AND function is removed and is replaced with a Pass-Transistor logic based AND gate. Since in the PTL-style AND gate the n-mos transistors are in parallel they consume less power and provides a faster discharge of the pulse resulting in miniaturization and power consumption reduction in satellites. A software package called the TANNER EDA tools utilizing MOSIS 90nm technology is used for the study.

**Keywords** - Flip-flop, low power, pulse-triggered.

### **I. INTRODUCTION**

Flip-flops are critical timing elements in digital circuits which have a large impact on the circuit speed and power consumption. The performance of flip-flop is an important element to determine the efficiency of the whole synchronous circuit. Miniaturization of digital circuits used in satellites and in other space based systems is a rapidly growing research area. In an attempt to reduce power consumption in flip-flops a pulse enhancement method is presented. An implicit type pulse triggered flip-flop is designed using conditional pulse enhancement scheme. The pulse generation logic use two input AND gate at its discharge path which reduces the circuit complexity and hence the overall power is reduced. Pulses that trigger discharging are generated only when there is a need, so unwanted circuit activity due to glitches can be avoided which reduces the overall power consumption. Pulse discharge can be made faster. The delay inverters which consume more power for stretching the pulse width are replaced by the PMOS transistors which enhances the pull down strength when there is a longer discharge path. Transistor sizes are also reduced to provide area and power saving. Hiroshi Kawaguchi and Takayasu Sakurai In [2] has proposed a reduced clock-swing flip-flop (RCSFF) which is composed of a reduced swing clock driver and a special flip-flop which embodies the leak current cutoff mechanism. The RCSFF can reduce the clock system power of a VLSI system down to one-third compared to the conventional flip-flop. The RCSFF is composed of a true single-phase master-latch and a cross-coupled NAND slave-latch.

The master-latch is a current-latch-type sense-amplifier. The salient feature of the RCSFF is that it can accept a reduced voltage swing due to the single-phase nature of the flip-flop. The literatures surveyed can be summarized as follows. Bai-Sun Kong, Sam-Soo Kim, and Young-Hyun Jun in [3] describes a family of novel low- power flip-flops, collectively called conditional-capture flip-flops (CCFFs). They achieve statistical power reduction by eliminating redundant transitions of internal nodes. These flip-flops also have negative setup time and thus provide small data-to-output latency and attribute of soft-clock edge for overcoming clock skew-related cycle time loss. The sense amplifier based flip-flop described here operates much faster than the conventional flip-flops. Peiyi Zhao, Tarek K. Darwis and Magdy A. Bayoumi in [5] proposed a new flip-flop the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output. It uses a pulse generator which is suitable for double-edge sampling. The flip-flop is made up of two stages. Stage one is responsible for capturing the LOW-to-HIGH transition. Stage 2 captures the HIGH-to-LOW input transition. Antonio G. M. Strollo, Davide De Caro, Ettore Napoli, and Nicola Petra in [6] proposed a new sense-amplifier-based flip-flop. The proposed flip-flop provides ratioless design, reduced short-circuit power dissipation, and glitch-free operation. The new circuit has been successfully employed in a high-speed direct digital frequency synthesizer chip, the proposed circuit is able to keep the fast operation of the Kim SAFF while avoiding its drawbacks. Ying-Haw Shu, Shing Tenqchen, Ming-Chang Sun, and Wu-Shiung Feng in [7] described XNOR-Based Double-Edge-Triggered Flip-Flop. The XNOR-based approaches are difficult to reach the speed demand due to the delay of the XNOR-based clock generator. Here a new designed DET-FF based on an alternative XNOR gate is done, by utilizing the sensitivity to the driving capacity of the previous stage, using this simplified XNOR gate as a pulse-generator. A modified transparent latch following the pulse-generator acts as an XNOR-based DET-FF, which accomplishes almost same speed and less power dissipation as compared with the conventional DET-FFs. The XNOR-based DET-FF has been also implemented in a two-phase-pipeline system. Chen

Kong Teh, Mototsugu Hamada, Tetsuya Fujita, Hiroyuki Hara, Nobuyuki Ikumi, and Yukihito Oowaki in [8] introduced a new family of low-power and high-performance flip-flops, namely conditional data mapping flip-flops (CDMFFs), which reduce the dynamic power by mapping the inputs to a configuration that eliminates redundant internal transitions. Here two CDMFFs, with differential and single-ended structures have been proposed and their comparison with the conventional flip-flops is also done. Hamid Mahmoodi, Vishy Tirumalashetty, Matthew Cooke, and Kaushik Roy in [9] proposed four novel energy recovery clocked flip-flops that enable energy recovery from the clock network, resulting in significant energy savings. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency. A sinusoidal clock signal for energy recovery is used here for clock gating. Peiyi Zhao, Jason McNeely, Weidong Kuang, Nan Wang, and Zhongfeng Wang in [10], here various design techniques for a low power clocking system are surveyed. Among them is an effective way to reduce capacity of the clock load by minimizing number of clocked transistors. To approach this, a novel clocked pair shared flip-flop is proposed which reduces the number of local clocked transistors. In addition, low swing and double edge clocking, can be easily incorporated into the new flip-flop to build clocking systems. Saranya. L, Prof. S. Arumugam in [11] proposed a Low-Power Pulse-Triggered flip-flop. Here three kind of conventional pulse-triggered flip-flop are designed. First, the implicit Pulsed Data-Close to output (ip-DCO) pulse-triggered flip-flop. Second, the Modified Version of Hybrid latch flip-flop (MHLFF) and third is the Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop. Also the comparison of low power pulse triggered flip-flops between SAL, SVL logics are carried out. James Tschanz, Siva Narendra, Zhanping Chen, Shekhar Borkar, Manoj Sachdev, and Vivek De in [12] compared several styles of single edge-triggered flip-flops, including semi-dynamic and static with both implicit and explicit pulse generation. Also an implicit-pulsed, semi-dynamic flip-flop (ip-DCO) which has the fastest delay of any flip-flop considered. Tania Gupta, Rajesh Mehra in [13] proposed an explicit pulsed double edge triggered sense amplifier flip-flop for the low power and low delay. Redundant transitions are eliminated by using the conditional technique named conditional discharge technique. By using the fast improved version of the nickolic latch along with the sense amplifier approach a circuit with a low delay factor was designed. R. Nithyalakshmi, P. Sivasankar Rajamani in [14] presented a pulse enhancement technique for the reduction in power consumption of the flip-flop. An implicit type pulse triggered flip-flop was designed and also have designed a Johnson counter using the proposed flip-flop which provides a

glitch free decoding. Yin-Tsung Hwang, Jin-Fa Lin, and Ming-Hwa Sheu in [1] proposed a novel low power pulse triggered flip-flop. Here an implicit type pulse triggered flip-flop with conditional pulse enhancement scheme has been presented which uses a pass transistor logic (PTL) based AND gate in the discharging path which facilitates the discharge only when needed. In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. In this the clock generation circuitry an AND function is removed and is replaced with a Pass-Transistor logic based AND gate. Since in the PTL-style AND gate the n-mos transistors are in parallel they consume less power and provides a faster discharge of the pulse. A software package called the TANNER EDA tools utilizing MOSIS 90nm technology is used for the study.

## **II. IMPLICIT TYPE PULSE TRIGGERED FLIP-FLOP**

In implicit type flip-flops the clock distribution circuit is a built in logic and there is no need for an external circuitry for the clock division and distribution. Implicit type flip-flops consist of two parts, a clock distribution network or clock tree and a latch for data storage. Several low power techniques are available which can be applied to the pulse flip-flops they are conditional enhancement, conditional capture and conditional data mapping. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch.

## **III. IMPLICIT TYPE P-FF WITH PULSE CONTROL SCHEME**

Three conventional implicit pulse flip-flops are discussed in this section.

### **3.1 IP-DCO (IMPLICIT PULSED-DATA CLOSE TO OUTPUT)**

The ip-DCO is an efficient design, is given in Fig1. The pulse generator is AND based logic and a semi-dynamic structured latch design which can interface both dynamic and static structures. Implementing logic designs are easy and delay penalty is small. It occupies small area and also it uses single phase clocking. It has Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The complementary of the clock signal is taken and it is delay skewed and applied as the input to the pulse generator to generate

a transparent window equal in size to the delay by inverters I1-I3. There are two disadvantages. It has larger switching power and there is a larger capacitance load which causes speed and performance degradation.

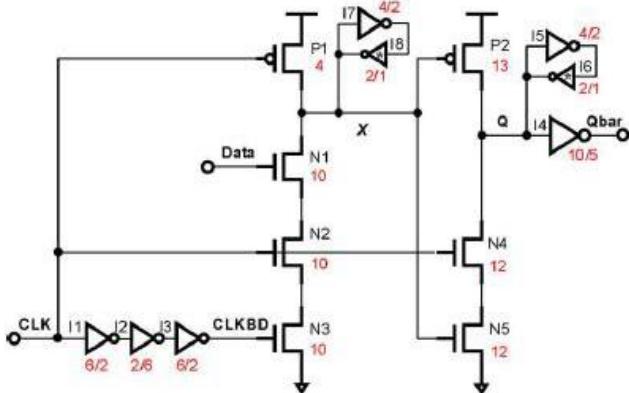


Figure 1 ip-DCO

### 3.2 MHLLF (MODIFIED HYBRID LATCH FLIP-FLOP)

Static latch structure is employed. Precharging of the node reduces the delay, but the power consumption is increased. Here the periodical precharging of node by the clock signal does not take place. When Q is low, the node is maintained high with the help of a weak pull-up transistor P1 which is controlled by the FF output signal Q. The unnecessary discharging problem at node is eliminated by using this design. But during the "0" to "1" transition, there is a longer Data-to-Q. This is mainly because node is not pre-discharged. The area consumption is high because we need larger transistors to enhance the discharging capability. When D=Q=1 there is extra power consumption because of the floating nodes.

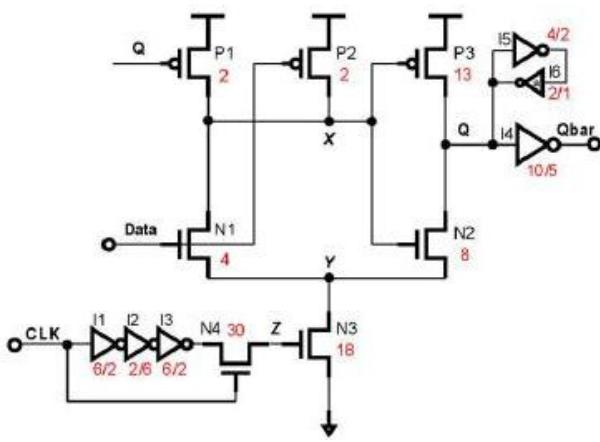


Figure 2. MHLLF

### 3.3 SCCER (SINGLE ENDED CONDITIONAL CAPTURE ENERGY RECOVERY)

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paragraphs should have SCCER is a design which is a modification over the ip-DCO design. It uses a conditional discharged technique in which the discharge path is controlled by eliminating the switching activity when the input stays in stable HIGH. In this design, the back to back inverters which is used instead of pull up and pull down resistors is replaced by a weak pull up transistor P1 and inverter I2 to reduce the load capacitance of node. The series connection of two nMOS transistors N1 and N2 is used in the discharge path. An extra nMOS transistor N3 is used to eliminate the unwanted switching activity. The Q\_fdbk is used to control N3, so if D=1 there is no discharge. The discharge path is long when the input data is "1".

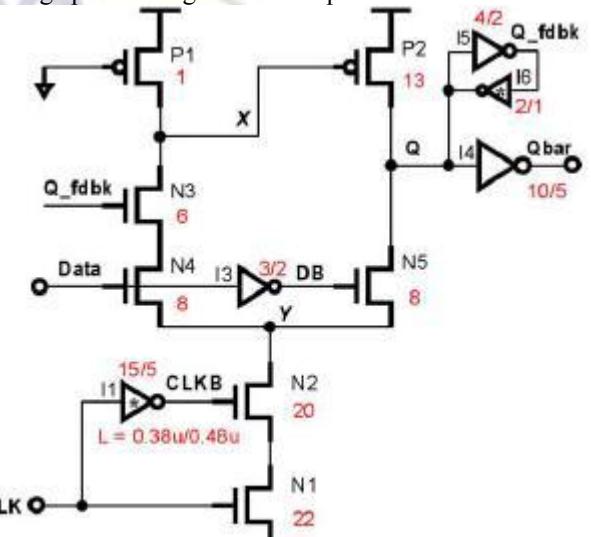


Figure 3. SCCER

### 3.4 PROPOSED MODEL

The proposed model is a implicit type pulse triggered flip-flop with a conditional pulse enhancement scheme.

There are two measures employed to overcome the draw backs in the conventional designs. Due to the presence of the large number of transistors in the discharging path the delay is high and also large power is consumed in power-up of the transistors. So, the number of nMOS transistors in the discharging path should be reduced. Also there is a need to increase the pull down strength when the input data=1. So there is a need to conditionally enhance the pull down strength when input data is "1." This design inherits the upper part of the SCCER design. Transistor stacking design of ip-DCO in Figure 4.4 and SCCER in Figure 4.6, is replaced by removing the transistor N2 from the discharging path. Transistor N2 and N3 are connected in parallel to form a two-input pass transistor logic (PTL)-based AND. It controls the discharge of transistor N1. The input to the AND logic is always complementary to each other. As a result, the output node is kept at zero

most of the time. There is a floating node when both input signals equal to "0". But it doesn't provide any harm to the circuit performance. The critical circumstance occurs only when there is rising edges at the clock pulse. Transistors N2 and N3 are turned ON together in this case to pass a weak logic high to node. This weak pulse strength is enhanced by switching ON the transistor N1 by a time span equal to the delay provided by inverter I1. The switching power at node can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. On designing the flip-flop in this way, the number of transistors in the discharging path can be reduced. This speeds up the pulse generation and hence delay is reduced. The area overhead is also reduced. The flip-flop using the conditional enhancement scheme is given in the Figure 4.

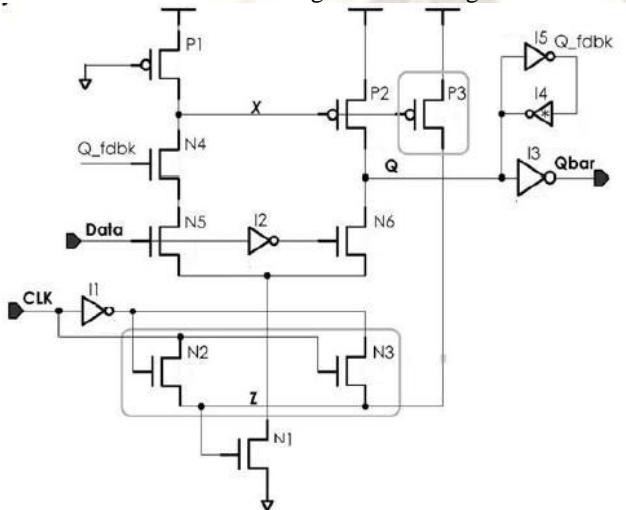


Figure 4. Proposed Model

Pulses that trigger discharging are generated only when there is a need, so unwanted circuit activity due to glitches can be avoided which reduces the overall power consumption. Pulse discharge can be made faster. The delay inverters which consume more power for stretching the pulse width are replaced by the PMOS transistors which enhances the pull down strength when there is a longer discharge path. Transistor sizes are also reduced to provide area and power saving.

#### IV. RESULTS

All the conventional pulse-triggered flip flop mentioned in fig 1 and the proposed model described in 4 were analyzed using the TANNER EDA utilizing the MOSIS 90nm. The waveforms of the MHLLF and the proposed model of the conditional pulse enhancement based pulse flip-flop were simulated and the output shows that the conditional

pulse enhancement based flip-flop has taller pulses at the node x.

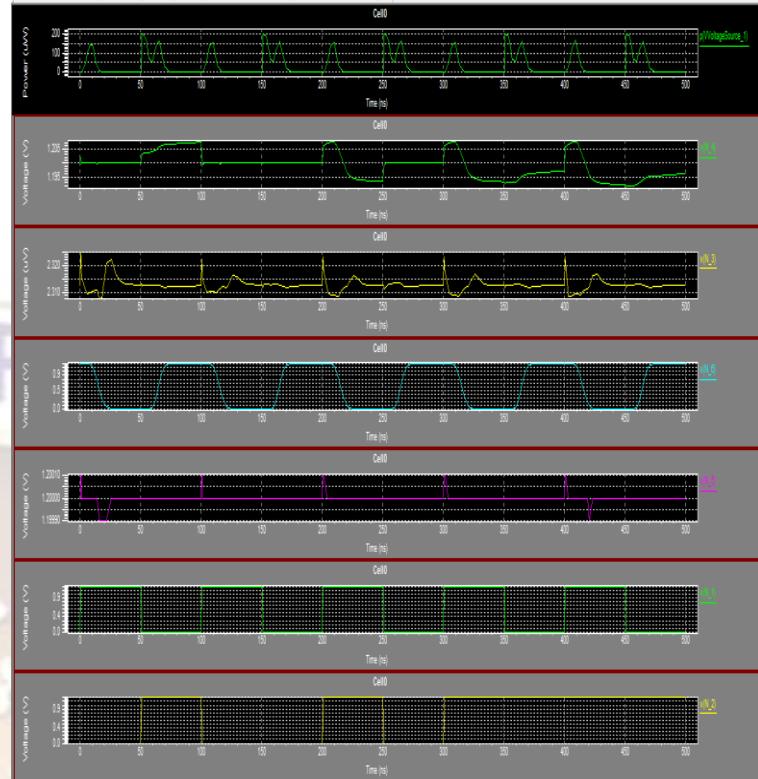


Figure 5. Simulation Waveform of MHLLF

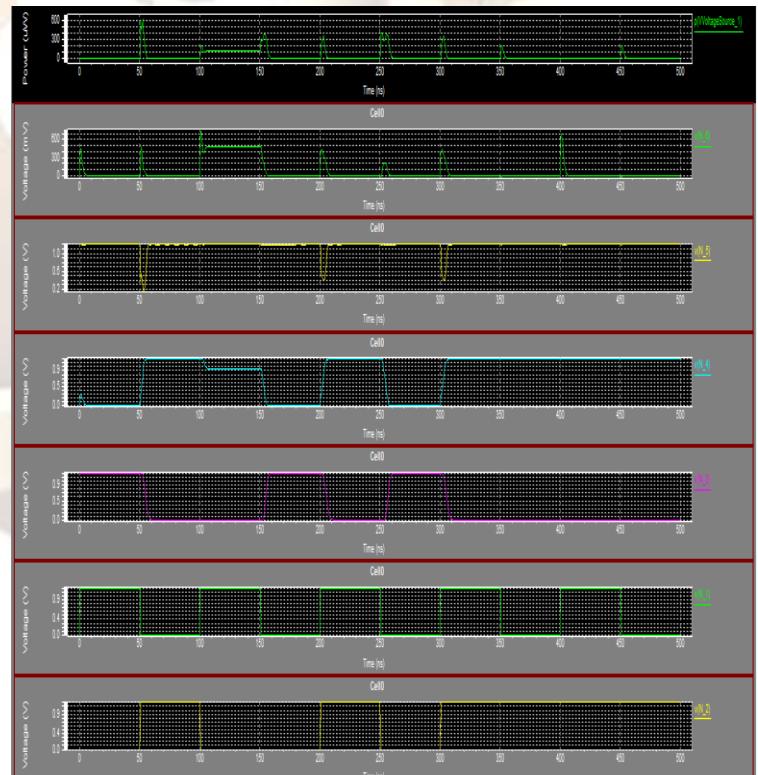


Figure 6. Simulation Waveform of the Proposed Model

The graphs are in the order Average power consumption spectrum, the output at the node X, output at the node Z of the flip-flop, the output Q of the flip-flop, the complement of the output, the input clock signal and the input data

## V. CONCLUSION

In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. In this the clock generation circuitry an AND function is removed and is replaced with a Pass-Transistor logic based AND gate. Since in the PTL-style AND gate the n-mos transistors are in parallel they consume less power and provides a faster discharge of the pulse. A software package called the TANNER EDA tools utilizing MOSIS 90nm technology is used for the study. The comparison of the Number of transistors used and the Average power consumed for 100% activity, 50% activity and 0% activity are done. The power consumed is for five cycles of operation. The power consumption shows a decreasing trend as the switching activities are reduced. From the above results it is clear that this type of design approach can be implemented in real space systems to increase the efficiency as well as to minimize the power consumption.

## REFERENCES

- [1] Yin-Tsung Hwang, Jin-Fa Lin, and Ming-Hwa Sheu, 2012, "Low-Power Pulse-Triggered Flip-Flop Design With Conditional Pulse-Enhancement Scheme," Proc IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 2, pp. 361-366.
- [2] Hiroshi Kawaguchi and Takayasu Sakurai, 1998, "A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction," IEEE Journal of Solid-State Circuits, Vol.33, No.5, pp. 807-811.
- [3] Bai-Sun Kong, Sam-Soo Kim, and Young-Hyun Jun, 2001, "Conditional-Capture Flip-Flop for Statistical Power Reduction," Proc. IEEE Journal of Solid-State Circuits, Vol. 36, NO. 8, pp. 1263- 1271.
- [4] Samuel D.Naffziger, Glenn Colon-Bonet, Timothy Fischer, Reid Riedlinger, Thomas J. Sullivan, and Tom Grutkowski, 2002, "The Implementation of the Itanium 2 Microprocessor," IEEE Journal of Solid-State Circuits, Vol.37, No.11, pp. 1448-1460.
- [5] Peiyi Zhao, Tarek K. Darwish, and Magdy A. Bayoumi, 2004, "High-Performance and Low-Power Conditional Discharge Flip-Flop", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 5, No. 5, pp. 477-484.
- [6] Antonio G. M. Strollo, Davide De Caro, Ettore Napoli, and Nicola Petra, 2006, "A Novel High-Speed Sense-Amplifier-Based Flip-Flop" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 13, No. 11, pp. 1266-1274
- [7] Ying-Haw Shu, Shing Tenqchen, Ming-Chang Sun, and Wu-Shiung Feng, 2006, "XNOR-Based Double-Edge-Triggered Flip-Flop for Two-Phase Pipelines", IEEE Transactions On Circuits and Systems—II, Express Briefs, VOL. 53, NO. 2, pp. 138-142.
- [8] Chen Kong Teh, Mototsugu Hamada, Tetsuya Fujita, Hiroyuki Hara, Nobuyuki Ikumi, and Yukihito Oowaki, 2006, "Conditional Data Mapping Flip-Flops for Low-Power and High-Performance Systems", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 12, pp. 1379-1383.
- [9] Hamid Mahmoodi, Vishy Tirumalashetty, Matthew Cooke, and Kaushik Roy, 2009 "Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating," Proc IEEE Transactions on Very Large Scale Integration(VLSI) Systems, Vol. 17, No. 1, pp. 33-44.
- [10] Peiyi Zhao, Jason McNeely, Weidong Kuang, Nan Wang, and Zhongfeng Wang, 2011, "Design of Sequential Elements for Low Power Clocking System," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 5, pp. 914-918.
- [11] Saranya. L, Prof. S. Arumugam, 2013, "Optimization Of Power For Sequential Elements In Pulse-Triggered Flip-Flop Using Low Power Topologies," International Journal of Scientific & Technology Research Volume 2, Issue 3.
- [12] James Tschanz, Siva Narendra, Zhanping Chen, Shekhar Borkar, Manoj Sachdev, and Vivek De, "Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High-Performance Microprocessors," Microprocessor Research Labs, Intel Corporation 5350 N.E. Elam Young Parkway, Hillsboro, OR 97124, USA.
- [13] Tania Gupta, Rajesh Mehra, 2012, "Low Power Explicit Pulsed Conditional Discharge Double Edge-Triggered Flip-Flop," International Journal of Scientific & Technology Research Volume 3, Issue 11.
- [14] R.Nithyalakshmi, P.Sivasankar Rajamani, "Power Efficient Counter Design Using Conditional Pulse-Enhancement Flip-Flop", 2013, International Journal of Engineering Science and Innovative Technology, Volume 2, Issue 2.