

Analysis of Total Voltage Source Power Dissipation in 6t Cntfet Sram and Force Stacking Cntfet Sram at Low Supply Voltage

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ABSTRACT

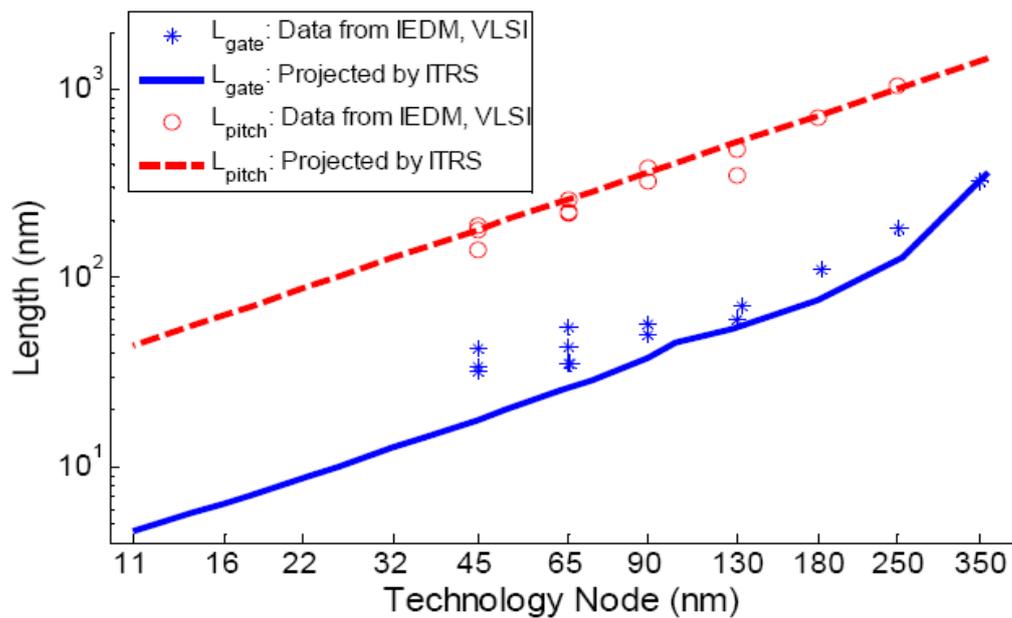
As scales down technology reaches to 90nm and below, the bulk CMOS will approach the scaling limit due to the increased short-channel effects and leakage power dissipation, severe process variations, high power density and so on. To overcome this scaling limit, different types of materials have been experimented and used. Si-MOSFET-like Carbon nanotube FET (CNFET) devices have been evaluated as one of the promising and reliable replacements in the future nanoscale electronics. CNFET has higher sub-threshold slope and lower short-channel effect than Si-MOSFET. It has been observed that the stacking of two off devices rather than one off device has smaller leakage current. This paper propose a SRAM that uses forced stack technique to reduce power dissipation. Circuit is simulated using HSPICE with Stanford CNFET model at 32nm. The simulation result shows that the proposed forced stack CNTFET SRAM reduces the power dissipation in every decreasing

low supply voltage compare to CNTFET SRAM without Force stacking.

Keywords - CNTFET SRAM, Force Stacking, HSPICE, Low supply voltage, Power dissipation.

I. INTRODUCTION

Ever since the 0.35 μm node, the gate length of MOSFET has entered the deepsubmicron region. 65 nm technology becomes the mainstream since 2006, and 45 nm technology has been announced in 2007. As CMOS continues to scale deeper into the nanoscale, various device non-idealities cause the I-V characteristics to be substantially different from well-tempered MOSFETs. It becomes more difficult to further improve device/circuit performance by reducing the physical gate length. The discrepancy between the fabricated physical gate length and the ITRS [1] projected gate length becomes larger as the technology advances, as shown in Figure 1.1. On the other hand, as the major driving force for the semiconductor industry, the device contacted gate pitch (Lpitch) is scaled down by a factor of 0.7 every technology node. Reasonable questions to ask are: Will the MOSFET scaling be stopped? Is there a way to extend the silicontechnology roadmap? After silicon technology, or as a complement to silicon technology, is there any potential technology that may be used?



According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. According to Moore's law, the dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years. This scaling down of devices has been the driving force in technological advances since late 20th century. However, as noted by ITRS 2009 edition, further scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range [1]. The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping. Carbon nanotubes (CNT) are very promising in respect of overcoming the serious limits faced by the Si CMOS Technology, because of their exceptional structural, electronic, and optical properties [2]. In particular, they exhibit ballistic transport over length scales of several hundred nanometers. Nanotube devices can be integrated with existing silicon-based structures. A CNTFET refers to a FET that uses CNT as the channel instead of bulk silicon in the traditional MOSFET structure.

SRAM is one of the important building block in the digital circuit. SRAM is further building block built from inverter which occupies about 90% of the area of soc in 2013. so its important to design low power SRAM using CNTFETs.

Authors have proposed a new SRAM cell design using CNTFETs. while there are circuit level solutions to reduce leakage in processors. Force stacking technique is used in leakage reduction and

reducing power dissipation authors have already published their paper in IJERA before but non of authors have compared power dissipation at different low supply voltage. this paper proposes and analyze power dissipation in CNTFET based SRAM and force stacking CNTFET SRAM at low supply voltage.

II. THE CARBON NANOTUBE FET

A carbon nanotube field-effect transistor (CNTFET) refers to a [field-effect transistor](#) that utilizes a single [carbon nanotube](#) or an array of carbon nanotubes as the channel material instead of bulk [silicon](#) in the traditional [MOSFET](#) structure. First demonstrated in 1998, there have been major developments in CNTFETs. According to [Moore's law](#), the dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years. This scaling down of devices has been the driving force in technological advances since late 20th century.

However, as noted by ITRS 2009 edition, further scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range. The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping. These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk MOSFET structure with a single carbon nanotube or an array of carbon nanotubes

The exceptional electrical properties of carbon nanotubes arise from the unique electronic structure of graphene itself that can roll up and form

a hollow cylinder. The circumference of such carbon nanotube can be expressed in terms of a chiral vector: $\hat{C}_h = n\hat{a}_1 + m\hat{a}_2$ which connects two crystallographically equivalent sites of the two-dimensional graphene sheet. Here n and m are integers and \hat{a}_1 and \hat{a}_2 are the unit vectors of the hexagonal honeycomb lattice. Therefore, the structure of any carbon nanotube can be described by an index with a pair of integers (n,m) that define its chiral vector. In terms of the integers (n,m) , the nanotube diameter d_t and the chiral angle θ are given by (1) and (2).

$$d_t = \frac{\sqrt{3}a_{C-C}\sqrt{m^2 + mn + n^2}}{\pi} \dots\dots\dots(1)$$

$$\theta = \tan^{-1} \left(\frac{\sqrt{3}n}{2m + n} \right) \dots\dots\dots(2)$$

1. GEOMETRY DEPENDENT CNTFET

- a. Back-gate CNTFET
- b. Top gate CNTFET

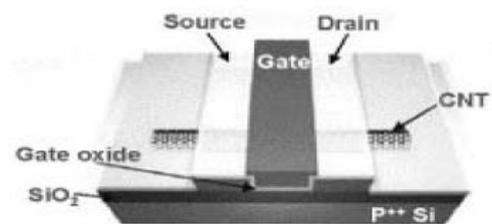
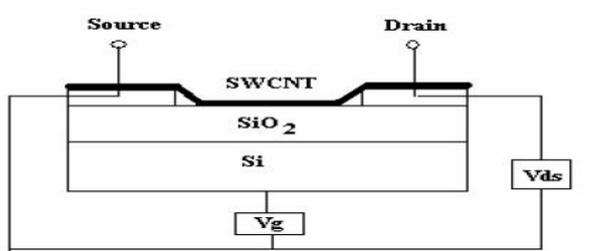


Fig : 1.7 (a) Back-gate CNTFET, 1.7(b) Top-gate CNTFET

2. ELECTRODE DEPENDENT CNTFET

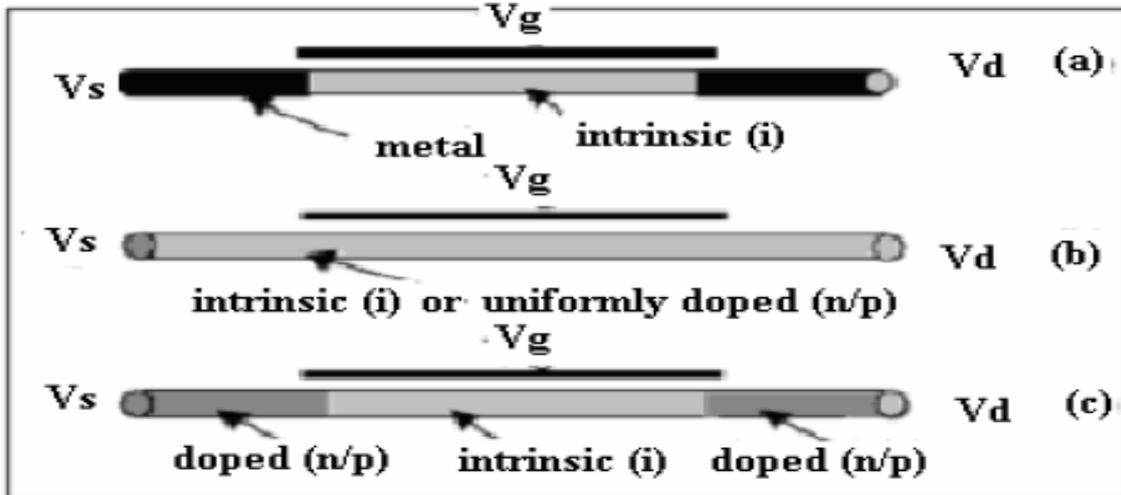


Fig : 1.8 (a) metal gate CNTFET 1.8 (b) uniform doped CNTFET 1.8 (c) Intrinsic gate and doped (n/p)

3. CNTFET TECHNOLOGY

Carbon nanotube (CNT) consists of a graphene sheet that rolled into a cylindrical structure. CNTs can be classified into two groups,

- 1. SWCNT

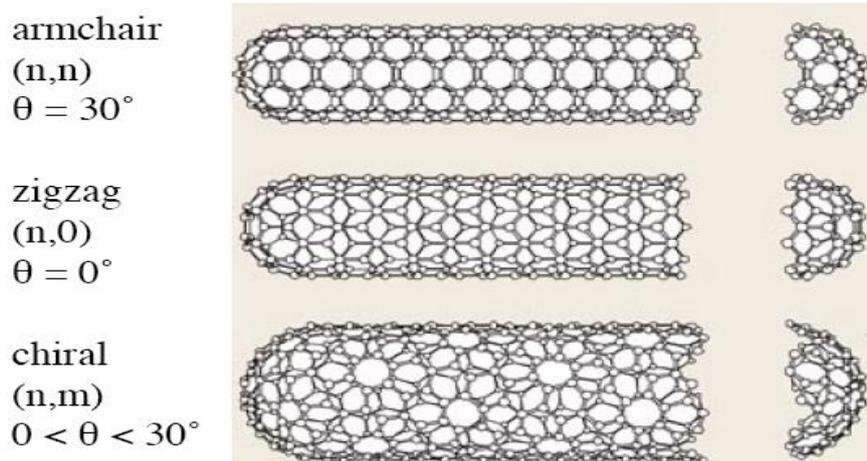


Fig :1.9 single walled CNT

2.MWCNT.

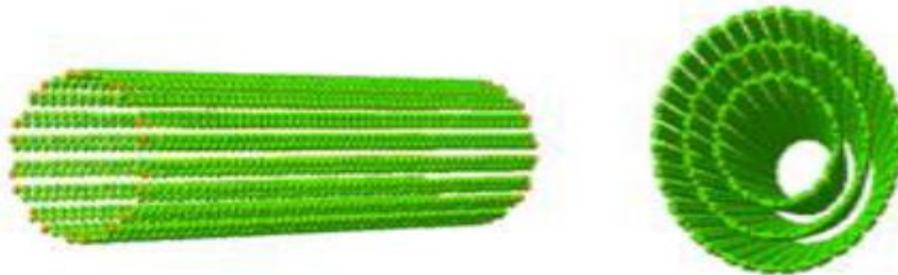


Fig 1.1.0 single walled CNT and multiwalled CNT

The first one has only one cylinder and the former has multi cylinders . Each SWCNT has a two dimensional vector

$$(n_1, n_2) = (n_1 a_1, n_2 a_2)$$

called chiral vector that specifies its electrical properties . The SWCNT has the zigzag structure when $n_1=0$ or $n_2=0$, and if $n_1= n_2$, the SWCNT has the armchair structure. Chiral vector defines whether a SWCNT is semiconducting or metal.

If

$$|n_1 - n_2| = 3k (k \in \mathbb{Z})$$

K is an any integer.....1,2,3,4,5,6,7,8,9.

the SWCNT is metallic and conducting, otherwise it is semiconducting. For determining the diameter of a SWCNT, we can draw a carbon molecule as a regular hexagon in a circle as shown.

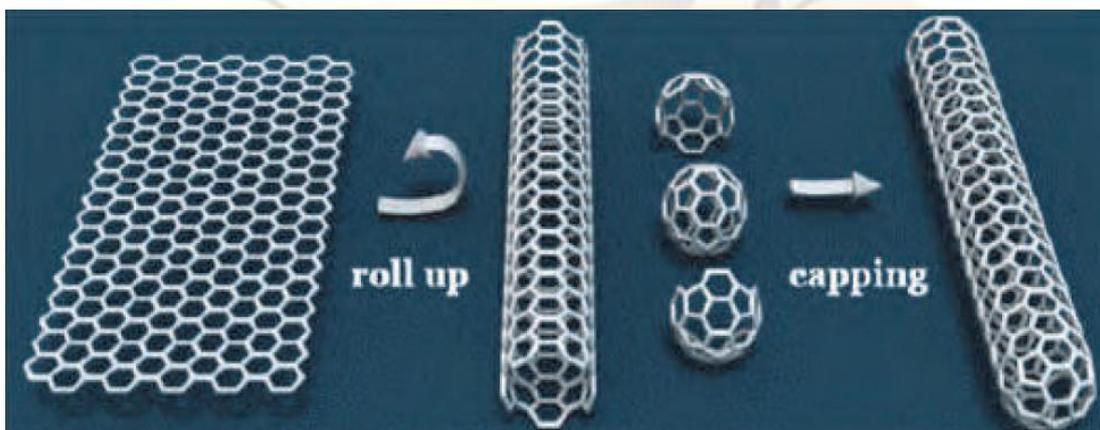


Fig 1.1.1: SWCNT roll up and capping

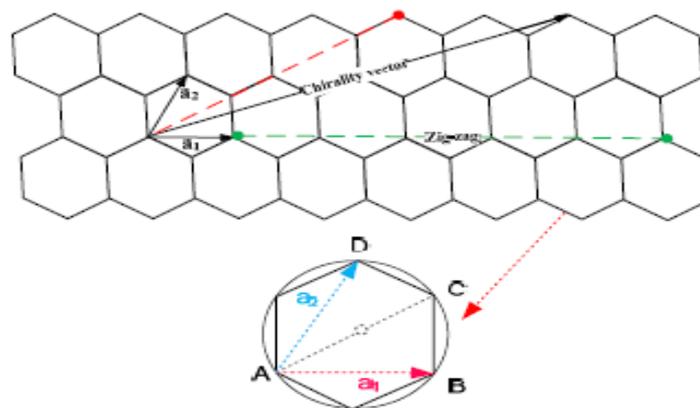


Fig 1.1.2 Chiral vector illustration

In this figure triangular ABD is isosceles, so $a_1 = a_2$. By considering the rectangular triangle ABC and by means of triangular relationship $|a_1|$ and $|a_2|$ is determined as:

The chiral vector is calculated as:

$$a_1 = a_2 = 2a_0 \sin(60^\circ) = \sqrt{3}a_0$$

$$Ch^2 = a_1^2 n_1^2 + a_2^2 n_2^2 + 2a_1 a_2 n_1 n_2 \cos(60^\circ) \quad (4)$$

$$Ch = \sqrt{3} a_0 \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (5)$$

$a_0 = 2.49 \text{ \AA}$ nearest bond distance

CNT diameter

$$D_{CNT} = \frac{\sqrt{3} a_0 \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \quad (6)$$

Threshold voltage

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3} a_0 V_\pi}{3 e D_{CNT}} \approx \frac{0.43}{D_{CNT}(\text{nm})} \quad (7)$$

III. FORCED STACK BAICS

Stacking transistor can reduce sub-threshold leakage. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power. The effect of stacking on reducing leakage can be understood from the Fig. 2.

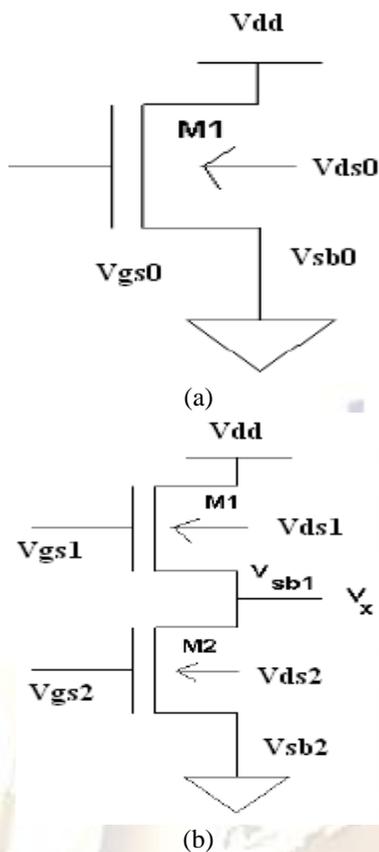


Fig. 2: (a) Single Transistor (b) Forced Stack Transistor

If the input is '0', then both transistor M1 and M2 are turned off. Here V_x is the intermediate node voltage between M1 and M2. Transistor M2 has its internal resistance. Due to this resistance V_x is greater than the ground potential. This positive V_x results in a negative gate-source (V_{gs}) for the M1 transistor and the negative source-base voltage (V_{sb}) for M1. Here M1 also has a reduced drain-source voltage (V_{ds}), which lower the drain induced barrier lowering (DIBL) effect. These three effects together reduced the the leakage power. The Figure 3 also illustrates the concept of Stacking effect.

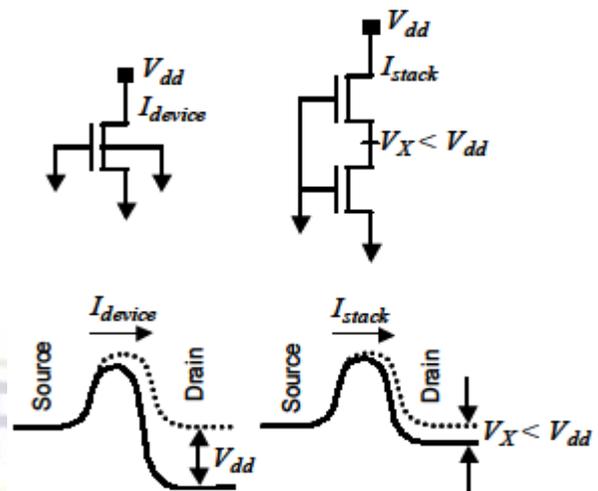


Fig. 3: Leakage current difference between a single OFF device and a stack of two OFF devices.

IV. CNTFET SRAM

Static Random Access Memory (SRAM) is a type of semiconductor memory. SRAMs are a major component of digital systems such as Embedded systems, microprocessors, reconfigurable International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4, December 2011 170 hardware, field programmable gate arrays just to name a few. Fast memory access times and design for density have been two of the most important target design criteria for many years, however with device scaling to achieve even faster designs; power supply voltages and device threshold voltages have scaled as well leading to degradation of standby power and static noise margins of memories. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote "0" and "1". Two additional access transistors help controlling the access to the cross coupled unit formed by the inverters during read and write operations. So typically it takes six transistors to store one memory bit. The design of a basic SRAM cell is shown in Figure 2. Access to the cell is enabled by the word line (WL) which controls the two access transistors M5 and M6 which allow the access of the memory cell to the bit lines: 'BL' and 'BLbar'. They are used to transfer data for both read and write operations. The presence of dual bit lines i.e. 'BL' and 'BLbar' improves noise margins over a single bit line. The symmetric circuit structure allows for accessing a memory location much faster than in a DRAM. Also the faster operation of an SRAM over DRAM can be attributed to the fact that it accepts all address bits at a time where as DRAMs typically have the address multiplexed in two halves, i.e. higher bits followed by lower bits. The SRAM is operated in one of the three modes namely WRITE, READ and IDLE operations. The start of a write

cycle begins by applying the value to be written and its complement to the bit lines. In order to write a '0', we would apply a '0' to the bit line 'BL' and its complement '1' to the 'BLbar'. A '1' is written by inverting the values of the bit lines i.e by setting 'BL' to '1' and 'BLbar' to '0'. 'WL' is then made high and the value that is to be stored is latched in. The inputdrivers of the bit lines are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Proper operation of an SRAM cell however needs careful sizing of the transistors in the unit. The read cycle is started by asserting the word line 'WL', enabling both the access transistors M5 and M6. The second step occurs when the values stored in 'Q' and 'Qbar' are transferred to the bit lines 'BL' and 'BLbar' through M1 and M6. On the BL side, the transistors M4 and M5 pull the bit line towards VDD (when a

"1" is stored at Q). If the content of the memory was a 0, the reverse would happen and 'BLbar' would be pulled towards 1 and 'BL' towards 0. For the idle state, the word line is not asserted and the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters INV1 and INV2 formed by M1, M2 and M3 M4 will continue to reinforce each other as long as they are disconnected from any external circuits. The operation of CNFETs based memories is very similar to that of CMOS except for minor differences in device orientation. One such difference being that the source and drain terminals of a CNFET are not interchangeable as is the case with MOSFET devices. Care must therefore be taken to orient the transistors in a memory cell in a manner that will ensure correct transmission of logic levels.

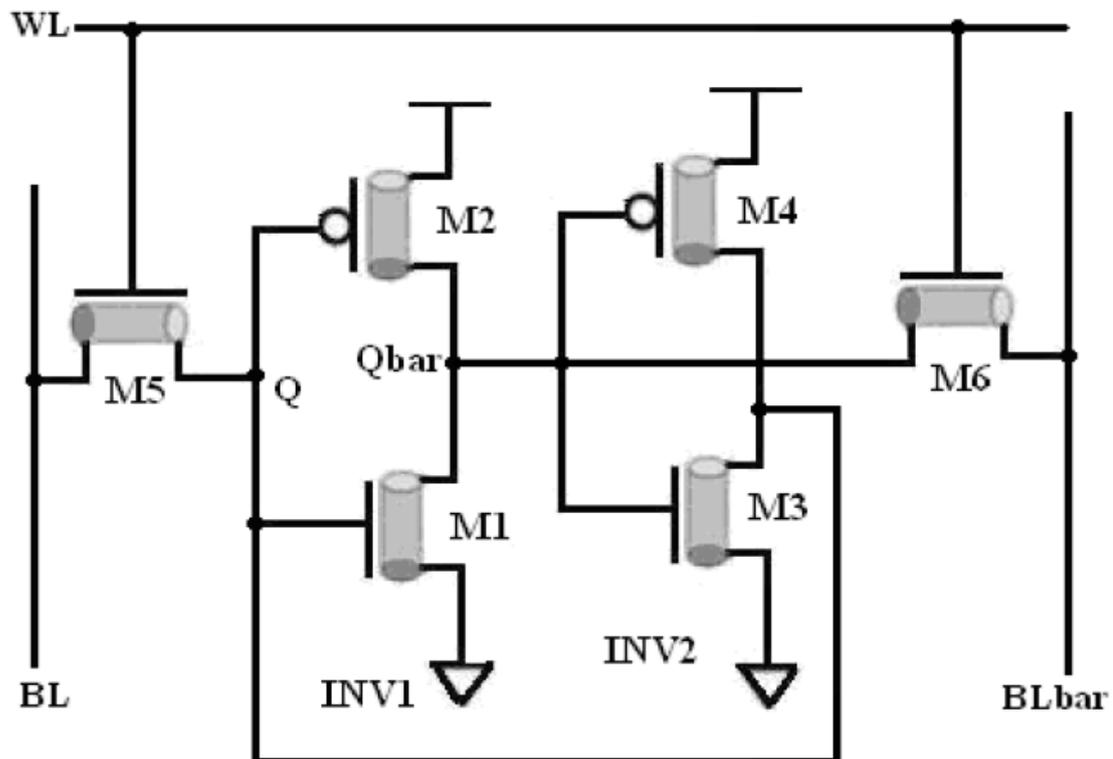


Figure 3.1. The basic 6T CNTFET SRAM Cell

V. SIMULATION RESULTS

The proposed inverter cell based on CNTFETs is designed and simulated using the Synopsis HSPICE. Simulations performed with Stanford CNTFET model at 32nm feature size with supply voltage VDD of 0.9V, 0.8 and 0.7. The following technology parameters are used for simulation of 6T SRAM and force stacking SRAM cells using CNTFET Technology :

- Physical channel length ($L_{channel}$) = 32.0nm.
- The length of doped CNT source/drain extension region (L_{sd}) = 32.0nm.

- Fermi level of the doped S/D tube (E_{fo}) = 0.6 eV.
- The thickness of high-k top gate dielectric material (T_{ox}) = 4.0nm.
- Chirality of tube (m,n) = (19,0).
- CNT Pitch = 10nm.
- Flatband voltage for n-CNTFET and p-CNTFET (V_{fbn} and V_{fbp}) = 0.0eV and 0.0eV.
- The mean free path in intrinsic CNT (L_{ceff}) = 200.0nm.

- The mean free path in p+/n+ doped CNT = 15.0nm.
- The work function of Source/Drain metal contact = 4.6eV.
- CNT work function = 4.5eV.

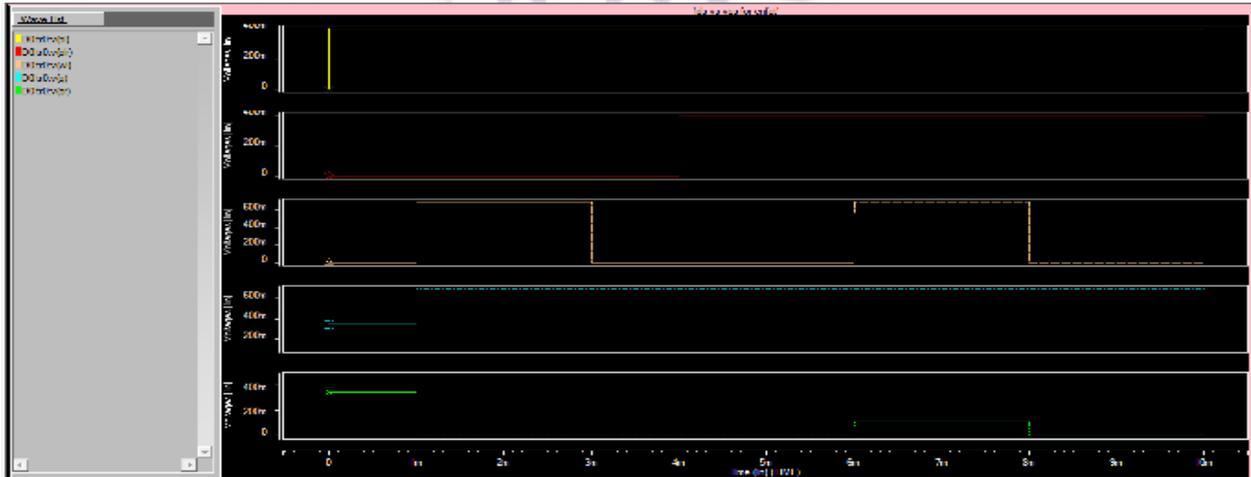
cell without forced stack Transistors are summarized in table 1 and table 2.

**CNFET SRAM WITHOUT FORCE STACKING
TABLE 1**

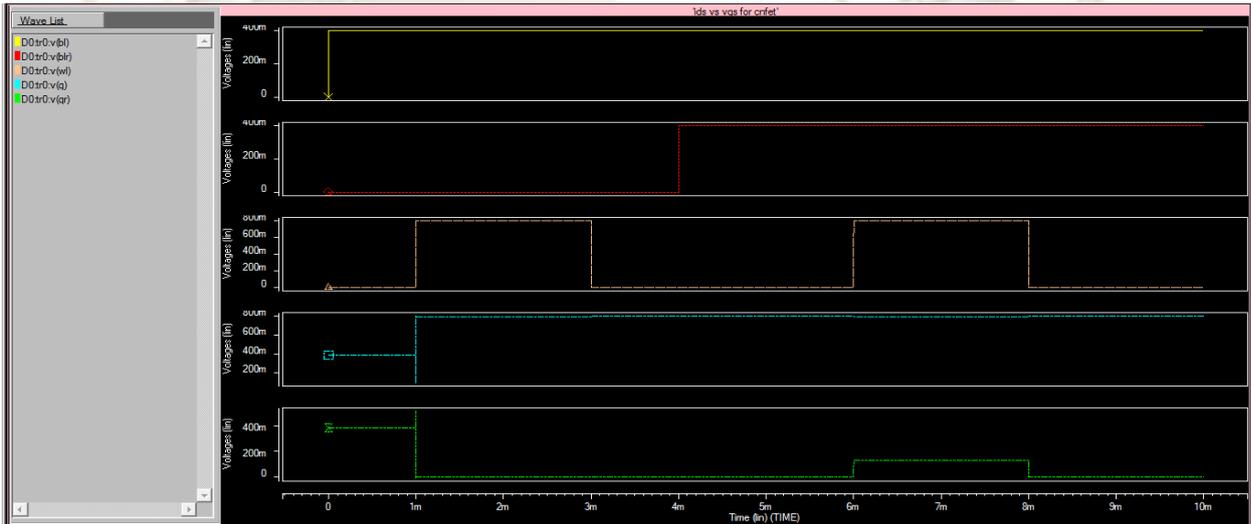
Supply voltage for SRAM	Power dissipation
0.9 v	1.433 E-05 watts
0.8v	8.753E-06 watts
0.7v	4.692E-06 watts
0.6v	2.039E-06 watts

The HSPICE avanwaves is used for displaying and measuring simulation parameters. power adissipation of both CNTFET SRAM Cell with Forced stack Transistors and CNTFET SRAM

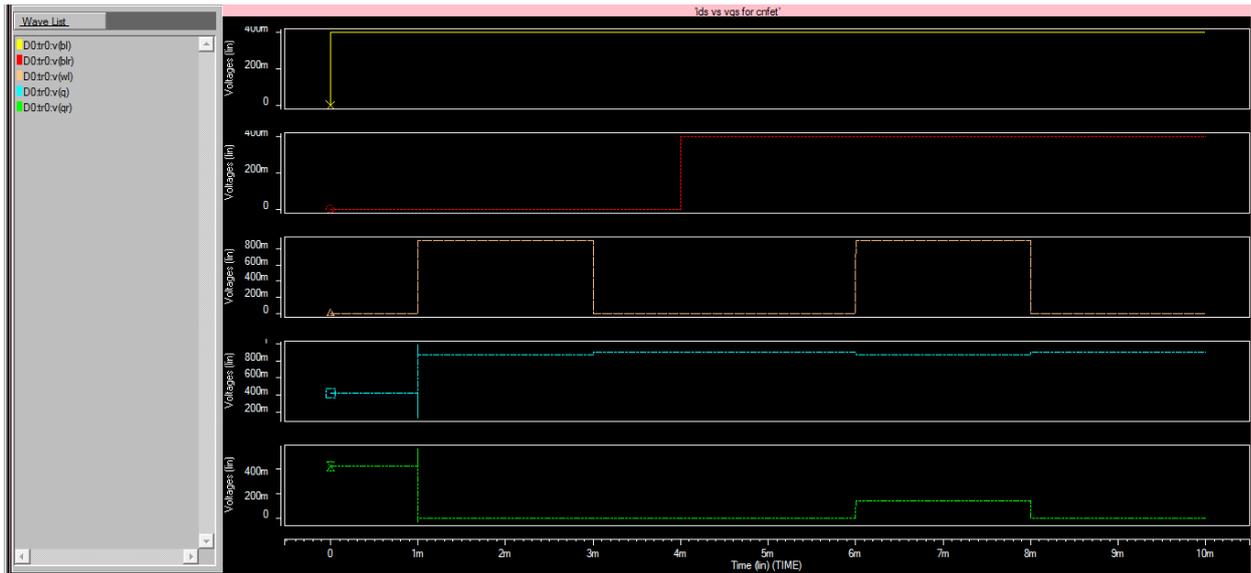
TRANSIANT ANALYSIS OF 6T SRAM AT DIFFERENT VOLTAGE AT VDD 0.7



AT VDD 0.8



AT VDD 0.9



CNFET SRAM WITH FORCE STACKING

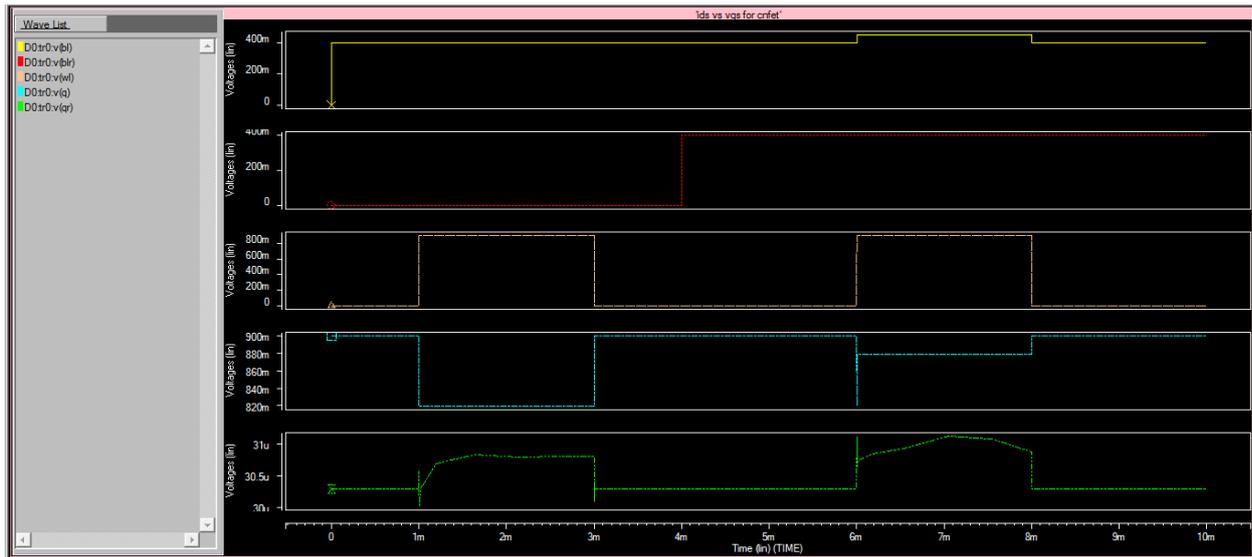
TABLE 2

Supply voltage for SRAM	Power dissipation
0.9 v	3.754E-09 watts
0.8 v	2.242E-06 watts
0.7v	9.906E-07 watts
0.6v	3.364E-7 watts

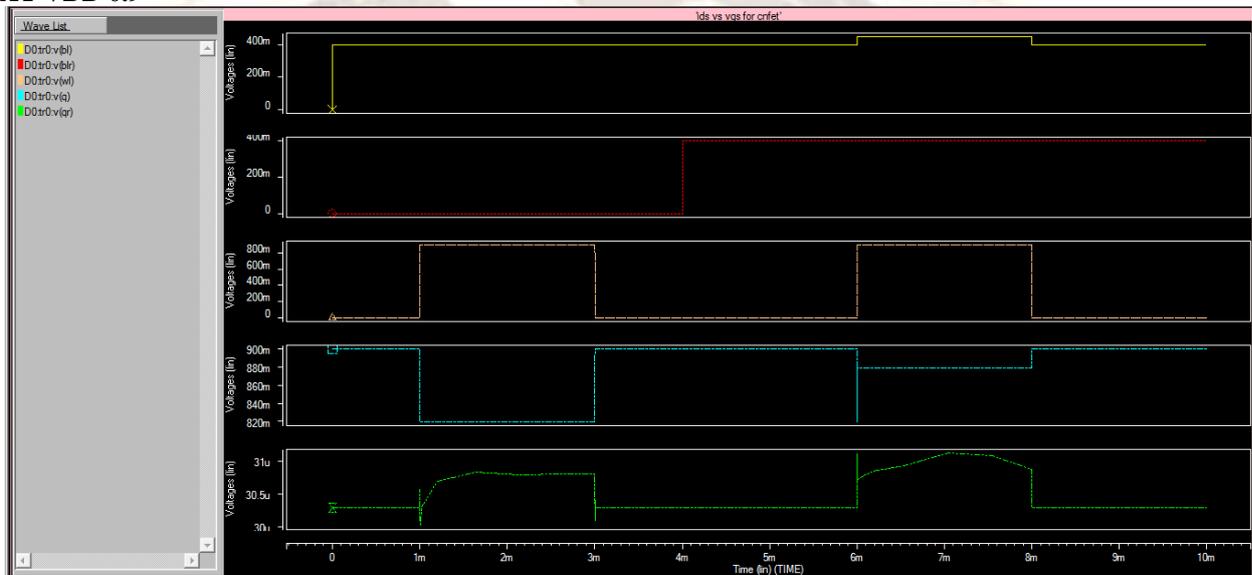
TRANSIANT ANALYSIS OF FORCE STACKING SRAM AT DIFFERENT VOLTAGE AT VDD 0.7



AT VDD 0.8



AT VDD 0.9



VI. CONCLUSION

Carbon nanotube electronics remains a very promising route to solve future down-scaling problems of conventional silicon technology. In this paper a CNTFET inverter using Forced Stack technique and without force stack technique is designed and simulated using HSPICE with Stanford CNFET Model at 32nm Technology at low supply voltage. The results shows that this proposed Forced Stack CNTFET SRAM cell reduces POWER dissipation to the significant effect compared to CNTFET SRAM without force stack technique. Table 1 and Table 2 shows that power dissipation reduce while lowering the supply voltage in CNTFET SRAM without force stacking , and force stacking technique SRAM but reduce much lower while lowering the supply voltage in force stacking CNTFET SRAM . This data shows that force stack

technique SRAM proposed design is better in low power dissipation than CNTFET SRAM without forced stacking.

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