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Reduction Of Power Consumption And Area Occupation By Using Deterministic Test Pattern Technique

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Abstract

Deterministic Test Pattern Technique. Which is used to reduce the number of test Patterns to find out the faults and hence power consumption will be reduced and 100% fault coverage. Partial matching pattern allows the reduction of the number of patterns used for detecting the random pattern resistant faults. A Multiple control Sequence is used to guide the linear feedback shift register (LFSR) to generate these patterns at application time. The patterns generated by the LFSR reduce 25% of power consumption when compared to those patterns produced by a conventional LFSR. The main advantages of this method are reduction of the test data volume, require less time to test the application and its reusability for logic cores on a system-on-chip (SOC).

Index Terms—-Built in self-test (BIST), Linear feedback shift register (LFSR), random-pattern-resistant (RPR) faults, system-on-chips (SOCs).

I. Introduction

Design integration can be increased by making the ICs small size and power should be low. The requirements for small size and low-power ICs have caused a significant increase in design integration. the integration several designs (cores) into a single monolithic IC which results in a system-on-chip (SOC). The number of cores integrated in a SOC is rapidly increasing, resulting in large amount of test data. To achieve the good test quality for the complex SOC by using the finite number of I/Os is a very difficult task. The amount of time required for this type of test application is high, it is also a big problem to overcome all these drawbacks and for testing embedded core based system chips is to use a built-in self-test (BIST). The advantages of built-in cell-test (BIST) are simplicity, flexibility and low overhead. The test pattern generator for the BIST is pseudorandom (PR) test pattern generator for its on-chip test pattern generation.

Pseudorandom test pattern generation (PRPG) can be implemented by using a linear feedback shift register. LFSR has several advantages. They are low overhead, scalability and reuse capability. Faults that are difficult to detect by pseudorandom pattern generation (PRPG) are called random-pattern-resistant (RPR) faults. To increase the probability of detecting the RPR faults by following the three categories. But these three categories have drawbacks

- The modification of circuit under test
- The use of weighted random pattern generation.
- The mixed mode approach.

The first category improves fault coverage by redesigning or inserting test points. It is not always possible because of performance restriction or intellectual property (IP) reasons. The second category is also to increase the probability for test patterns to detect RPR faults, but it is not efficient the third category consists of two phases: In the first phase, PR patterns are applied to detect the faults here fault coverage is done by 60% to 80% only. In the second phase, deterministic test patterns are injected to find the remaining faults. The deterministic patterns are generated by the LFSR[1] by reseeding are Appling a control signal that matches the output of the LFSR to the desired deterministic patterns.

A new technique for the generation of the test patterns for RPR faults by controlling the LFSR at the time of test application. This technique is called partial pattern matching. Select a BIST[2] using a controllable LFSR with multiple scan chains to generate deterministic patterns. In this approach, the system integrator is able to develop the core's tests without knowing the actual implementation of the core because providing deterministic test patterns and the S-matrix by the core provider. Hence, the method promotes design and test reuse without changing or revealing IP information.

Partial-matching technique along with multiple scan chains the BIST greater using a controllable LFSR, the goals such are

- To reduce the test data volume
- To shorten the test application time
- Reusability for logic cores

These three major goals can be achieved by mixed mode BIST. When comparing this method mixed-mode BIST environment to other mixed-mode approaches. In
Most mixed modes, the test flow is outlined in Fig. 1(a).
Our methodology is shown in Fig. 1(b): First, a deterministic ATPG is used. The patterns are then

partially matched. The remaining patterns are generated by applying a control sequence to the LFSR[1]. In our architecture shown in Fig. 2: It consists of controllable LFSR and phase shifter and scan chains and it is connected to the multi input signature register(MISR) from this it is connected to embedded memory from this it is connected to BIST[2] controller.

In many of the mixed modes, first the test flow is done by using a PR pattern, fault simulation is performed, and the RPR faults are identified. Then, a deterministic automatic test pattern generation (ATPG) is used to generate patterns for RPR faults.

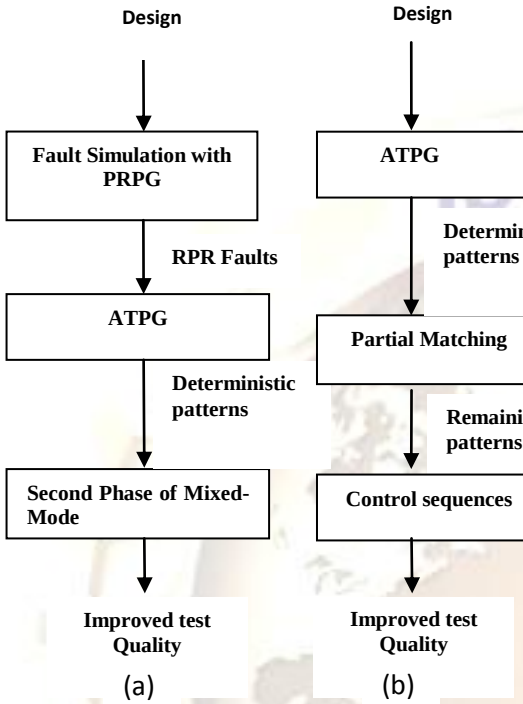


Fig. 1. Mixed-mode flow

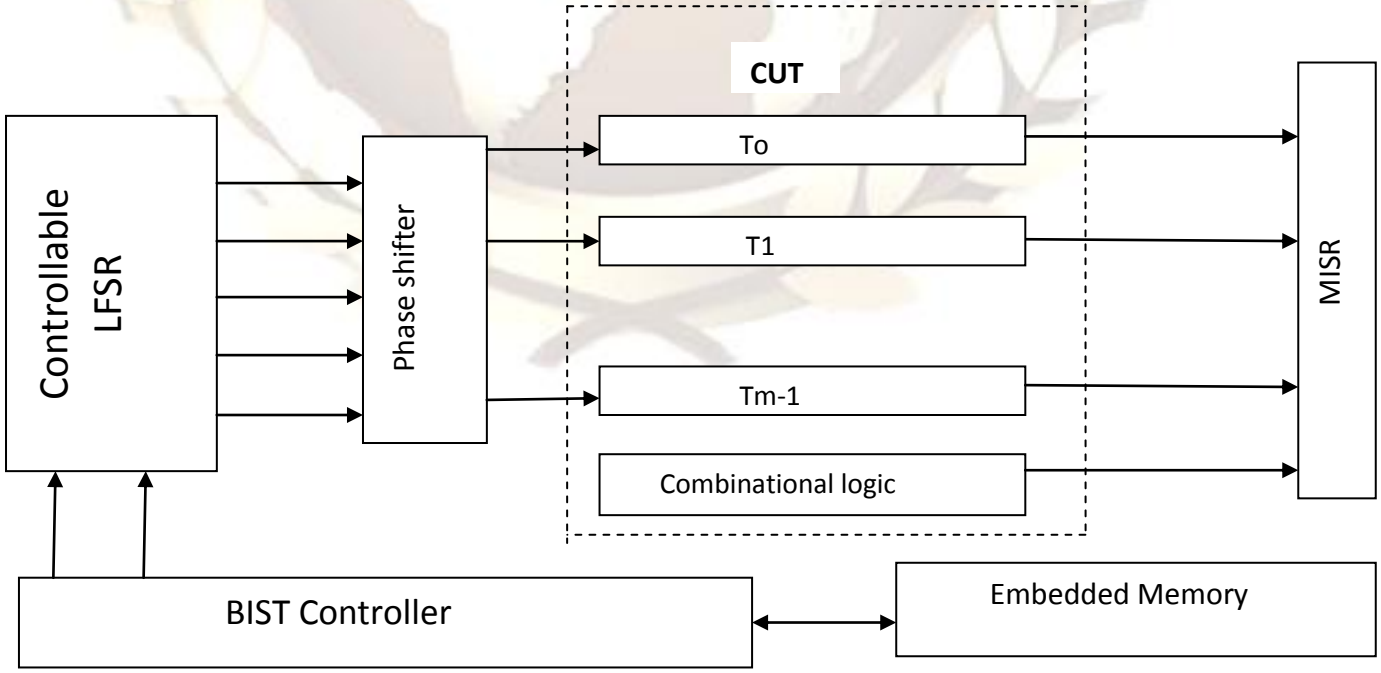


Fig. 2. Proposed testing architecture.

The second phase of the mixed-mode approach is then applied that is deterministic patterns are applied to target remaining faults. In our methodology first, a deterministic ATPG is used. The patterns are then partially matched. The remaining patterns are generated by applying control sequence to the LFSR. In our proposed method there are many advantages. First, fault simulation is eliminated but it is not in the case of other mixed modes. Second, the partial pattern matching increases the number of hits and hence leaves a fewer number of RPR patterns to require LFSR control signals. The shorter the control sequence, the smaller the storage needed on the chip. In section II, we describe the partial matching scheme. In section III, we describe the multiple-control sequence(MCS). Simulation results are presented in section IV, synthesis results are presented in section V, and in section VI, we present our results.

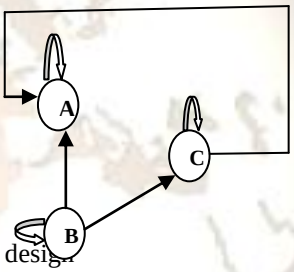
II. PARTIAL MATCHING

To maximize the fault coverage, all specified bits of the deterministic test patterns have to be fully matched by the PR patterns being produced by the LFSR. If there are many specified bits in the test pattern of a long scan chain, but it is difficult for PR pattern to hit any deterministic patterns with a full pattern match. This will result in huge number of test patterns that are not covered, this drawback can be eliminated in our new partial matching technique which analyzes the binary S-matrix. This binary S-matrix and utilizes the topology of the logic cones. This approach increases the possibility of patterns matching and hence reduces the size of the required control sequence.

Circuit Modeling

The binary S-matrix can be constructed from the S-graph [6] that is G = (V, E), where V is the set of vertices representing the scan cells in the circuit, E is the set of edges representing connectivity between the scan cells. The first step of the test preparation is to generate the binary S-matrix [6] for the cores. An entry S (i, j) =1 indicates that scan cell i is feeding into scan cell j. And S (I, j) =0 indicates that scan cell i is not feeding into scan cell j. Using the S-matrix confirms our approach with respect to testing without revealing IP information because the S-matrix is represented by the connectivity of scan cells without giving structure of the logic circuits.

In the similar way the scan chains can also be constricted, in such way that the scan cells in the same scan chain are independent of each other. The aim was to make the set of linear equations, which are necessary for the reseeding of an [illegible] words all the inputs of any logic cone [illegible] one scan chain but in our approac[illegible] of a logic cone can be in any scan chain.



	A	B	C
A	1	0	0
B	1	1	0
C	1	0	1

(c). Binary S-matrix of a design

Fig. 3 (b) S-graph of a design.

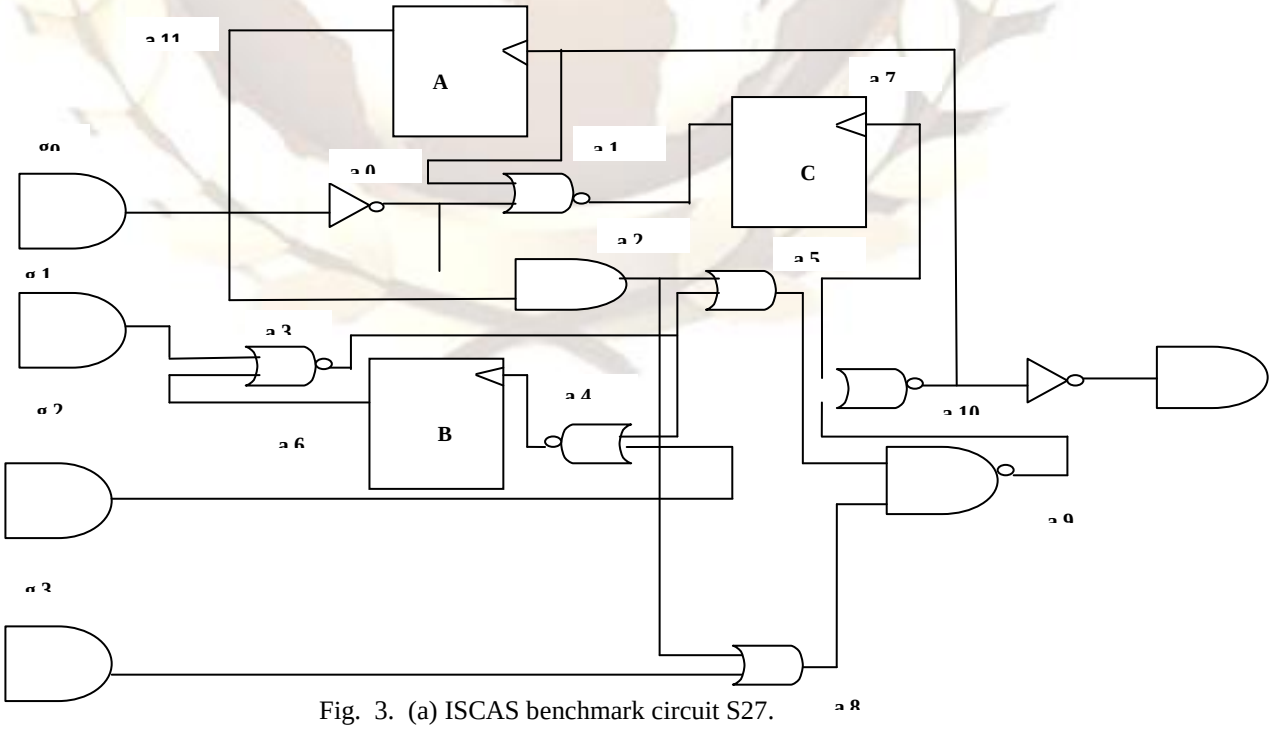


Fig. 3. (a) ISCAS benchmark circuit S27.

Using Logic Cones to Partition

A single deterministic test pattern generated by an ATPG usually detects more than one fault in the desire. When the pattern is captured by the flip-flops, the new input of any flip flop represents the response of pattern for faults within the combinational circuit cone converging at this flip flop. Logic cones are nothing but logic gates or simply combinational circuits each sub pattern corresponds to a logic cone of the design, which may contain multiple faults of the logic gates. For example deterministic test pattern expanded into three sub patterns each sub pattern detects faults in the corresponding logic cone sub patterns have more ”don’t care” bits than the original pattern. Hence, they are easier to match with the PR patterns then the original deterministic test pattern. Now a partial pattern matching technique is to be applied to the sub patterns as an enhancement to the full pattern matching technique, which has been applied to the original deterministic test patterns.

The partial matching technique consists of the following three steps.

- Form sub patterns for each deterministic pattern using a cone-masking approach.
- Generate the PR test patterns by simulating the LFSR and match them to sub patterns.
- Combine the remaining unmatched sub patterns that are related to the each original deterministic test pattern and update the final set of deterministic test patterns.

The original deterministic test patterns are split in to sub patterns for each deterministic test pattern the number of sub patterns is equal to the number of columns of the S-matrix that have at least one entry of a “1” . The value of bit i of sub pattern j is the same as the value of bit i of the deterministic test pattern if and only if S [i, j] is 1 otherwise it is unspecified bit(x).

In this method, there existing a phase shifter [4] and multiple scan chains. There are two test execution phases. During the first test phase, the LFSR is freely ran for a user specified number of N cycles to generate PR test patterns for easily detectable faults. The number of PR test patterns is the same as the used in all cores but with less test application time because of multiple scan chains. In the second test phase MCSs are used to direct the LFSR to generate the remaining patterns to detect the RPR faults.

Along with the phase shifter [4] and multiple scan chains there existing also a BIST controller. A pattern counter and a bit counter are part of the BIST controller. The bit counter keeps track of the number of test data bits being shifted into scan chains. The pattern counter counts the number of capture cycles that occur during each test execution phase.

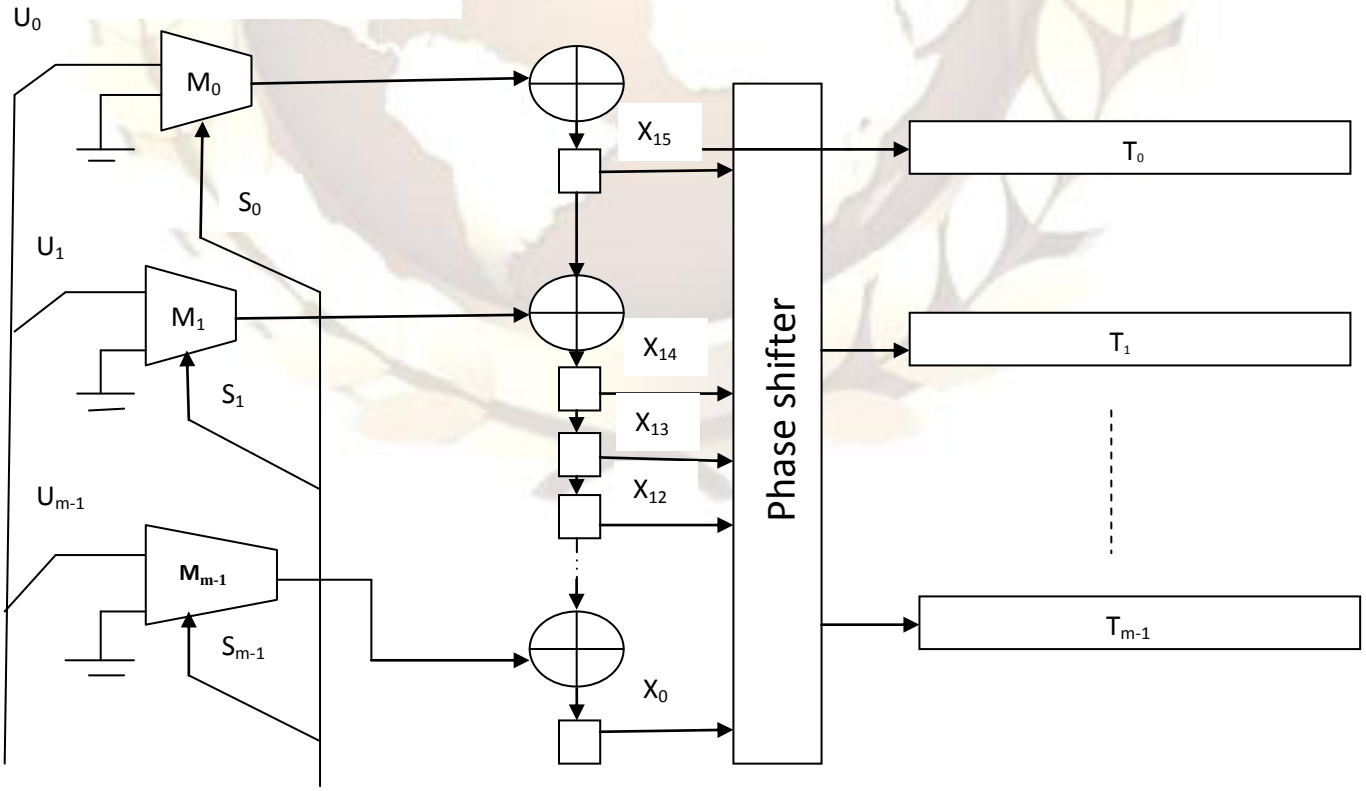


Fig. 4. Controlling the LFSR

TABLE I

Sub patterns for deterministic pattern

Deterministic Pattern A B C	Sub-Patterns A B C	Logic cone
0 1 1	0 x x	1
	x 1 x	2
	x x 1	3

The circuit shown in Fig. 3(a) is the ISCAS (International standard circuit and system) benchmark circuit S27. It can be represented by the S-graph shown in Fig. 3(b). The corresponding binary S-matrix is shown in Fig. 3(c). As per our methodology first Deterministic ATPG is used and it is found that as 011.This deterministic pattern is then split into three sub-patterns. Each sub pattern corresponds to a logic cone of the design. Number of logic for the circuit in Fig. 3(a), Table I shown deterministic test pattern (column 1) expanded into three sub patterns. In the circuit fault was injected at the a3 this fault is not identified by the random pattern and it is detected by deterministic pattern at the 011.once after finding the deterministic pattern and again the faults are injected at the a3, a4 and these faults are determined by random pattern and those faults which are not covered by random pattern are identified by deterministic pattern test generation. Thus all the faults will be determined by this method, by applying both random pattern test generation and deterministic pattern test generation, when s=0 the controllable LFSR [3] generate random test patterns and when s=1 it will generate the deterministic test patterns.

III. MULTICONTROL SEQUENCES

BIST controller allows the LFSR to freely run for a user defined number of capture cycles N it begins to control the LFSR.The method of deterministic bits presented a PRPG register to feed the LFSR seeds for generating the desired patterns in a multiple scan chain design For controlling the LFSR, using an MCS to direct it and to generate and apply the desired deterministic patterns in a multiple scan design. The MCS consists of two vectors U= (U_0, U_1, U_2…..U_{m-1}) and S= (S_0, S_1, S_2……S_{m-1}). The U vector was directly injected through multiplexers to scan chains. All multiplexers have been moved to the front of LFSR to improve both the test time and test data volume.

Phase shifters structure is based on the STUMPS architecture, one of the scan chains [5] is directly fed from the left most tap of the LFSR while other chains are fed from the phase shifter all the patterns supplied to each scan chains can be controlled. For example assume that four scan chain being controlled by four taps from the phase shifter deterministic test patterns indicated on These scan chains are (T_0, T_1, T_2, T_3) respectively. There are more advantages in using multi control to guide the LFSR to feed the target test data to the scan chains. In most of the cases only a few control sequences in some scan chains have to be specified while the remaining contents in the scan change are automatically matched to deterministic patterns. Therefore the rest of control sequences do not need to be specified. This further reduces the test data storage requirement.

The data format for the MCS consists of two and fields: a header and a body. The header specifies the logic values for the multiplexer selectors, body holds the MCSs U_0, U_1……U_{m-1}. If the deterministic pattern for the ith scans chain consists of only unspecified bits then the corresponding ith control sequence U_i is not needed to create the desires values of deterministic patterns. Therefore, Si is equal to zero, U_i can be skipped from the body field. However even If there is only one specified bit to be controlled in a deterministic pattern the corresponding control sequence U_i must be include in the body field S_i, and S_i is equal to one the advantage of MCS is to control any number of scan chain.

IV. Simulation results

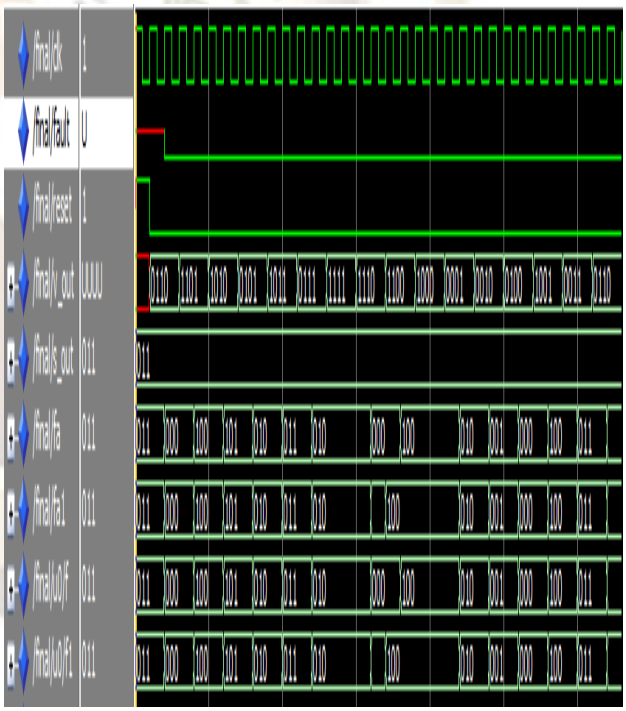


Fig. 5. Random pattern test generation.

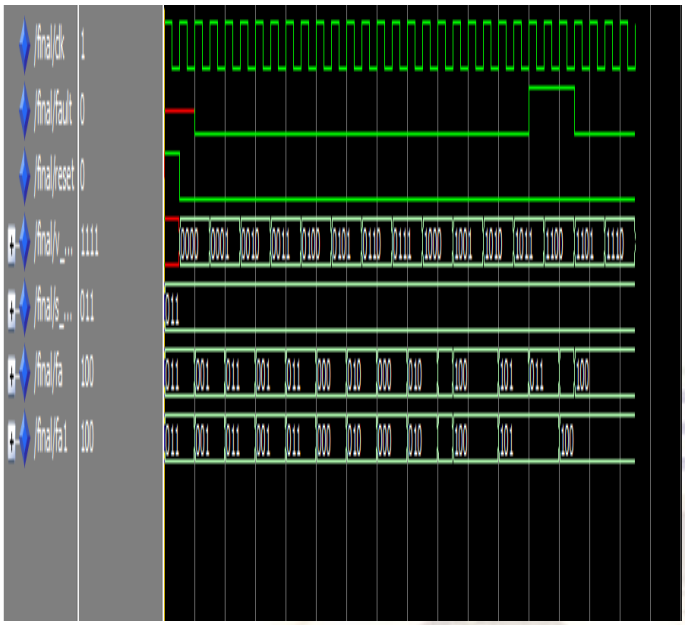


Fig. 6. Deterministic test pattern generation.

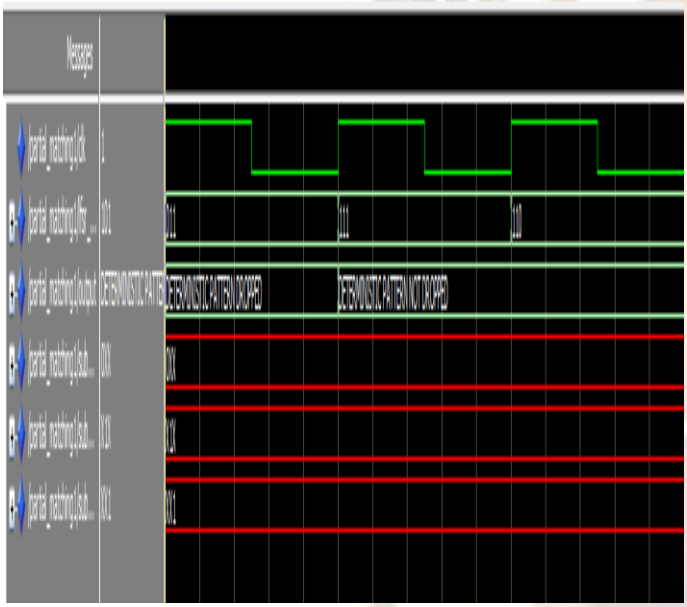


Fig. 7. S-graph and S-matrix.

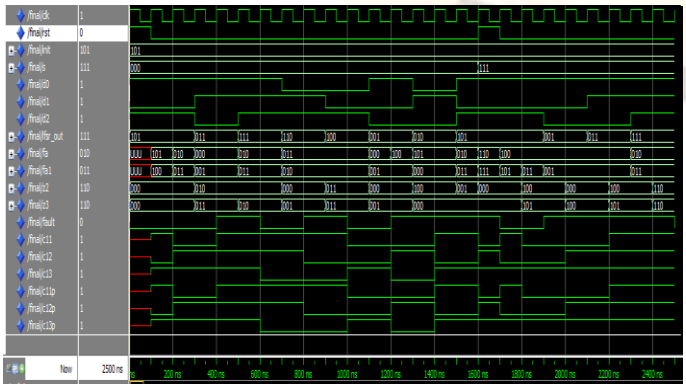
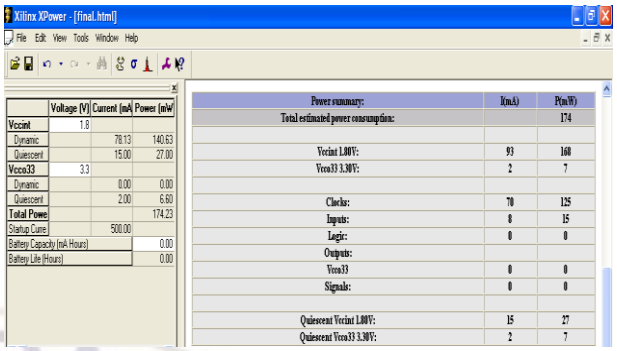


Fig. 8. ISCAS benchmark circuit S27.

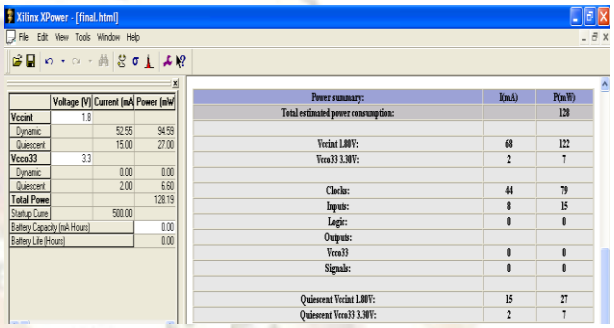
5. Synthesis result



Voltage	V	Current	mA	Power	mW
Vccint	1.8				
Dynamic			78.13		140.63
Quiescent			15.00		27.00
Vcco33	3.3				
Dynamic			0.00		0.00
Quiescent			2.00		6.60
Total Powe					174.23
Startup Curre			500.00		
Battery Capacity (mA Hours)					0.00
Battery Life (Hours)					0.00

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		174
Vccint 1.80V:	93	168
Vcco33 3.30V:	2	7
Clocks:	70	125
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig. 9. Power consumption using Random pattern test generation



Voltage	V	Current	mA	Power	mW
Vccint	1.8				
Dynamic			52.55		94.59
Quiescent			15.00		27.00
Vcco33	3.3				
Dynamic			0.00		0.00
Quiescent			2.00		6.60
Total Powe					128.19
Startup Curre			500.00		
Battery Capacity (mA Hours)					0.00
Battery Life (Hours)					0.00

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		128
Vccint 1.80V:	68	122
Vcco33 3.30V:	2	7
Clocks:	44	79
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig.10. Power consumption using Deterministic test pattern generation.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	49	9,312	1%	
Number of 4 input LUTs	30	9,312	1%	
Logic Distribution				
Number of occupied Slices	37	4,656	1%	
Number of Slices containing only related logic	37	37	100%	
Number of Slices containing unrelated logic	0	37	0%	
Total Number of 4 input LUTs	62	9,312	1%	
Number used as logic	30			
Number used as a route-thru	32			
Number of bonded IOBs	2	232	1%	
IOB Latches	1			
Number of GCLKs	1	24	4%	
Total equivalent gate count for design	793			
Additional JTAG gate count for IOBs	96			

Fig. 11. Area occupation using Random pattern Test Pattern Generation..

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	17	9,312	1%	
Number of 4 input LUTs	12	9,312	1%	
Logic Distribution				
Number of occupied Slices	11	4,656	1%	
Number of Slices containing only related logic	11	11	100%	
Number of Slices containing unrelated logic	0	11	0%	
Total Number of 4 input LUTs	15	9,312	1%	
Number used as logic	12			
Number used as a route-thru	3			
Number of bonded IOBs	2	232	1%	
Number of GCLKs	1	24	4%	
Total equivalent gate count for design	229			
Additional JTAG gate count for IOBs	96			

Fig. 12. Area occupation using Deterministic Test pattern Generation.

V. Conclusion

In conclusion, a new approach Deterministic test pattern technique to facilitate the generation of patterns for RPR faults. Using this method The test

application mode uses a controllable LFSR for a multiple-scan-chain configuration.

We have analyzed the design through the creation of a binary S-matrix and the identification of logic cones. Then, we have applied the partial pattern matching to filter the RPR faults. In addition, we have generated an MCS to guide the LFSR to generate the desired patterns instead of applying the whole deterministic test. the fault coverage as high as intended by the deterministic test, we have succeeded in reducing both the test data volume and the test application time. Moreover, in comparison with [22], both the test sequence length and the hardware overhead are much lower.

VI. Acknowledgment

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