

A High Speed Wide Range Frequency Synthesizer

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ABSTRACT

Present days the Frequency Synthesizer is used for the wireless communication in the GHz range to correct the phase and frequency error as well as to provide synchronization. As time passes the frequency of operation increases and the requirement of fast loop locking is required. This paper presents the design of a wide range voltage controlled oscillator, a wide range high speed fully programmable integer N prescaler, a phase frequency detector (PFD), an accurate charge pump and a loop filter which entails an entire 48MHz to 992MHz frequency synthesizer.

Keywords—Blind zone, CML Logic, Cycle Slip, Dead zone, Prescalar

I. Introduction

The Frequency synthesizer was first invented during the reduction of the noise in the radio received signal in the year 1932 and it was observed that the signal coming from the distance source is producing some noise if it is not properly tuned. Later it was observed that the noise is produced due to the mismatch of phase and frequency at the receiver input and a circuit was designed to reduce the phase and frequency error at the receiver side. When the time passes the frequency of operation increases and the requirement of fast loop locking is required.

Fig. 1 shows a generic PLL-based synthesizer. The Frequency synthesizer contains five block phase frequency detector (PFD), charge pump (CP), low pass loop filter (LPF), Voltage controlled oscillator (VCO) and frequency divider [1]-[2].

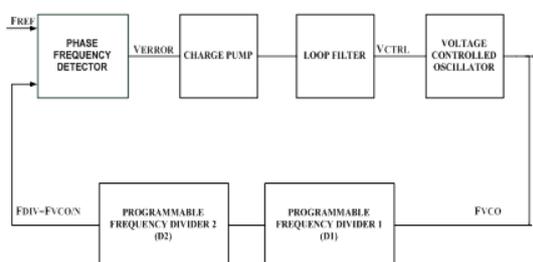


Fig. 1. Frequency Synthesizer

The operation of the PLL and the programmable counter in the feedback path allow generation of accurate high frequencies from a pure low frequency signal. The programmable divider D2 is preceded by a divider D1 that scales down the high output frequencies to a range at which standard

CMOS dividers can be implemented. The design of a Frequency synthesizer which operates for a wide frequency range with a good frequency precision and a very low locking time is really challenging.

II. Phase Detector

The three-state PFD circuit employs sequential logic to create three states and respond to falling edges of the two inputs, 'REF' and 'DIV' [2]. During State-0 falling edge of REF triggers the first DFF to which it is connected. Data (D) inputs of DFF's are connected to "1" thus UP switches to "1". Depending on the phase difference of REF and DIV, falling edge of DIV triggers the second DFF after a certain amount of time. Then DOWN (DN) switches from "0" to "1". At this point both inputs of the AND gate is "1" and its output turns to "1" which activates reset signal for DFF's. Reset signal generated by PFD resets the DFF's and outputs of both DFF's return to "0". The same sequence is valid if DIV is faster than REF but in the opposite direction.

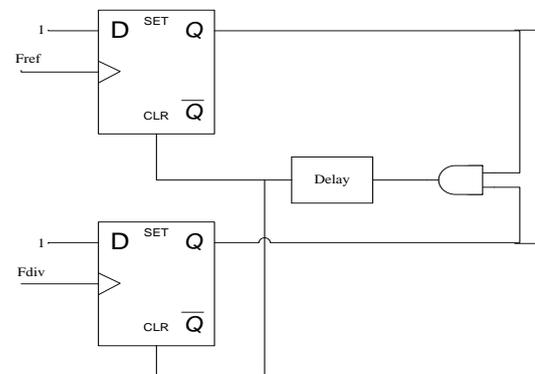


Fig. 2. Phase Frequency Detector

A dead zone [2] is a certain range of phase input difference to the PFD in which the PLL fails to lock. That means the VCO is allowed to accumulate as much random phase error proportional to the width of the dead zone while receiving no corrective feedback.

The dead zone exists because the charge pump switches are not ideal. They need a certain amount of time to turn on. So for example, when the UP signal pulse width is below 1 ns, the switch is still not closed properly because the pulse width is not enough to turn on the charge pump (to make its gate to source voltage greater than the threshold voltage) and thus, as a result, there will be no charging

current. Hence no corrective action. In other words, if the input phase difference, $\Delta\phi$ falls below a certain value ϕ_0 then the output voltage of phase frequency detector/charge pump/LPF combination is no longer a function of $\Delta\phi$. i.e. for $|\Delta\phi| < \phi_0$ the charge pump injects no current. The loop gain falls to zero and the output phase is not locked.

The dead zone vanishes if the width of error pulse is long enough to allow UP and DN to reach a valid logical level and turn on the switches in the charge pump. So we add delay blocks in the reset path. Thereby producing coincident pulses on UP and DN and eliminating the dead zone. The reset path should have much delay to properly switch the charge pump but it should not be much high leading to cycle slipping.

III. Charge Pump And Loop Filter

A charge pump is a three position electronic switch which is controlled by the three states of PFD. The three states are charging current ($+I_{cp}$), discharging current ($-I_{cn}$) and zero current [2]. When the VCO output frequency is lagging behind the reference frequency, the PFD will activate the UP signal and deactivate DN signal. Hence, switch S_1 will be closed and switch S_2 will be opened. Since switch S_1 is close, current I_{cp} will flow into the filter and increase the control voltage, V_{ctrl} . The increase in the control voltage, V_{ctrl} , will consequently increase the VCO output frequency. The same sequence is valid if VCO is faster than REF but in the opposite direction.

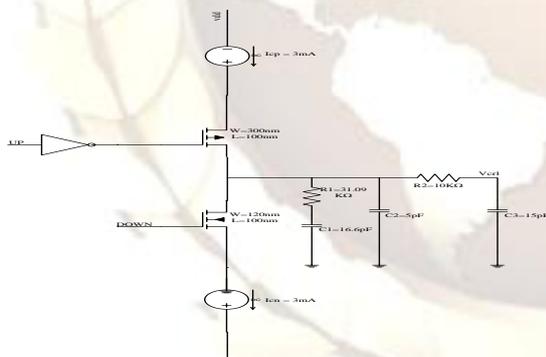


Fig. 3. Charge Pump and Loop Filter

The lock condition of the PLL is established when the VCO output frequency is the same as the reference frequency. During this period, the PFD will deactivate both UP and DN signals. Hence switches S_1 and S_2 will be opened until the VCO output frequency changes. Since switches are open, there is no current path formation, hence no current will flow into or out from the filter. Control voltage remains a constant.

IV. Voltage Controlled Oscillator

In order to vary the frequency of an LC oscillator [3], the resonance frequency of its tank(s) must be varied. Since it is difficult to vary the

inductance by means of a varactor, MOS varactors are more commonly used than pn junctions. The VCO using MOS varactor is shown in fig. 4. The varactor M_{V1} and M_{V2} appear in parallel with the tanks. The gates of the varactors are tied to the oscillator nodes and the source/drain/n-well terminals to V_{ctrl} . The oscillation frequency can thus be expressed as:

$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{var})}} \quad (1)$$

Where C_{var} denotes the average value of each varactors capacitance.

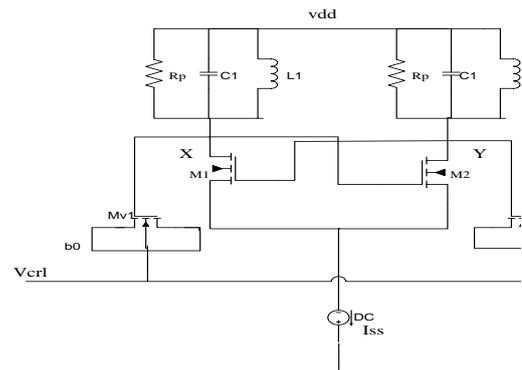


Fig. 4. VCO using MOS varactor.

In applications where a substantially wider tuning range is necessary discrete tuning may be added to the VCO so as to achieve a capacitance range well beyond C_{max}/C_{min} of varactors. Fig: 5 shows such an arrangement. The idea is to place a bank of small capacitors each having a value of C_u , in parallel with the tank and switch them in or out to adjust the resonant frequency.

The V_{ctrl} is known as fine control and the digital input to the capacitor bank is coarse control. The fine control provides a continuous but narrow range whereas the coarse control shifts the continuous characteristic. With ideal switches and unit capacitors, the lowest frequency is obtained if all of the capacitors are switched in and the varactor is at its maximum value, C_{max} :

$$\omega_{min} = \frac{1}{\sqrt{L_1(C_1 + C_{max} + nC_u)}} \quad (2)$$

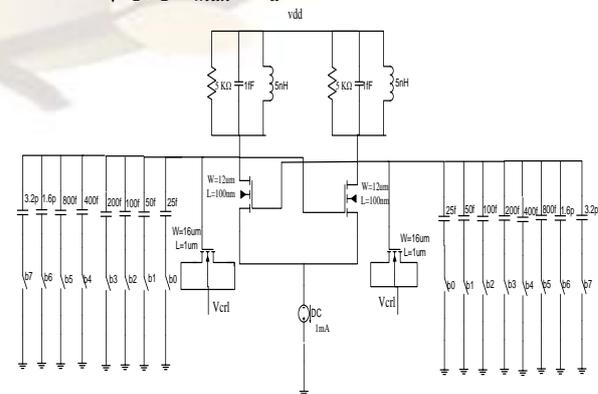


Fig. 5. Final LC VCO

The highest frequency occurs if the unit capacitors are switched out and the varactor is at its minimum value, C_{min} :

$$\omega_{max} = \frac{1}{\sqrt{L_1(C_1 + C_{min})}} \quad (3)$$

To avoid blind zones, each two consecutive tuning characteristics must have some overlap.

V. Programmable Prescaler

VCO output frequency ranges from 1GHz to 4GHz. So the programmable divider connecting to the output of the VCO should operate at high speed. Current mode logic is the choice for high speed mixed signal devices.

The divider configuration using CML [3] latches provides quadrature phases at X and Y only if CK and CKBAR are precisely complementary and the two latches match perfectly.

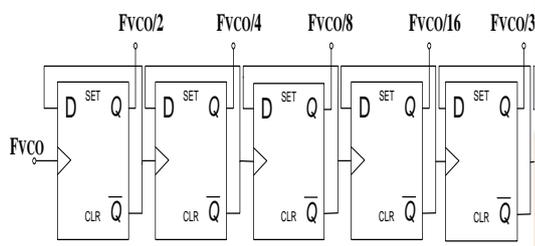


Fig. 6. Divider1

In the divider1(D1) we require divide by 4, divide by 16 and divide by 32. So a control logic is implemented with three selection bits C0, C1 and C2 to select the required frequency.

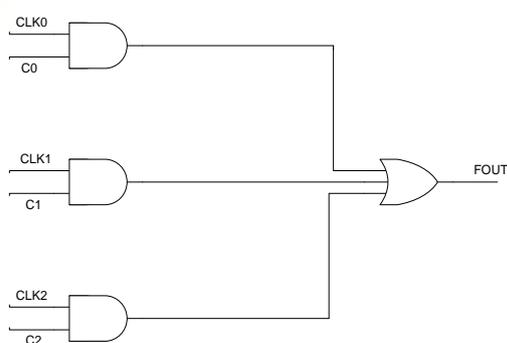


Fig. 7. Divider1 Control

CML buffers are used at the output of divider1 and the output from the buffer should be taken through inverter chain in order to shape and sharpen the waveform edges. In the output port of divider D1 also there must be inverter chain to shape and sharpen the output waveform edges and to produce rail to rail swing.

Divider 2 has to divide from 3 to 62 which is implemented with an up counter which count from 0 to 63.

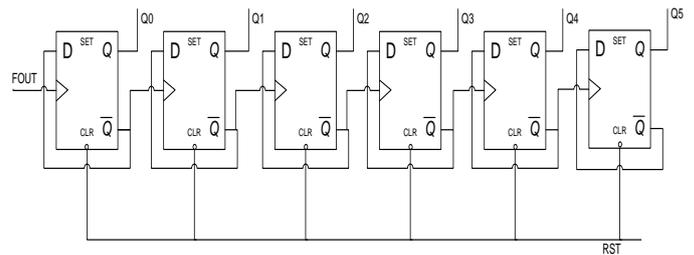


Fig. 8. Divider2

A control circuit is made with exor gates for comparing the selection bits (C3 to C8) and the output of the up counter. Whenever the selection bits are found equal to the output of the counter the up counter is reseted and thus the reset pulse will be divide by n of input clock fed to the up counter where n is the decimal equivalent of the selection

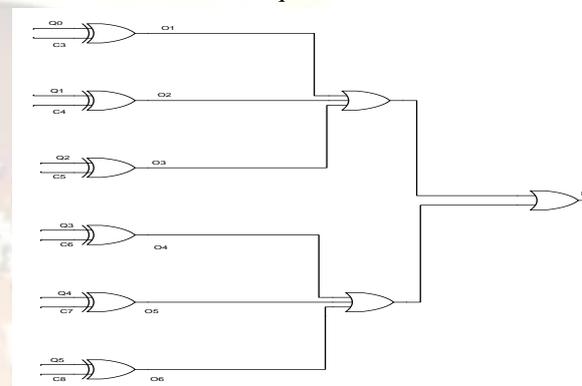


Fig. 9. Divider2 Control

Output of the divider2 counter is fed to the input of PFD. The whole divider circuit including the 2 dividers, inverter chains and buffers. The total delay of the circuit is found to be 106.35pS.

VI. Simulation Results

6.1 PFD Outputs

The output of the PFD when F_{ref} signal falling edge leads F_{div} signal falling edge and vice versa is shown in the Fig. 10 and Fig. 11 respectively.

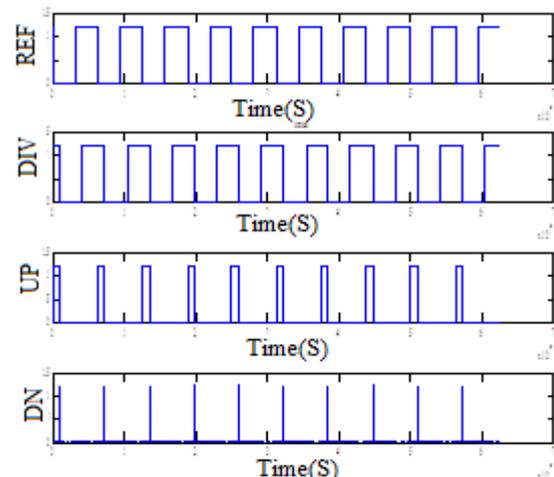


Fig. 10. When F_{ref} falling edge leads F_{div} rising edge

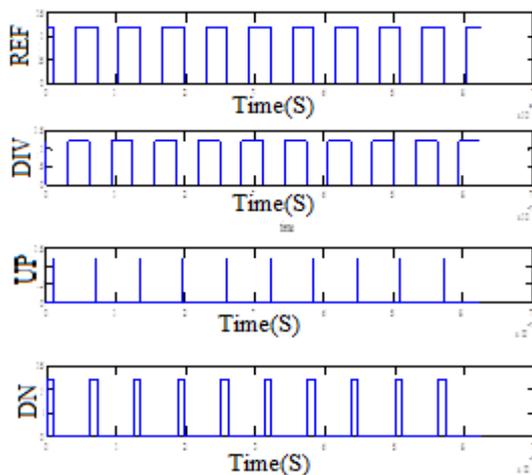


Fig. 11. When F_{ref} falling edge leads F_{div} rising edge

6.2 Loop Filter Outputs

The simulation result of the output of the loop filter circuit is shown in the Fig. 12 and Fig. 13.

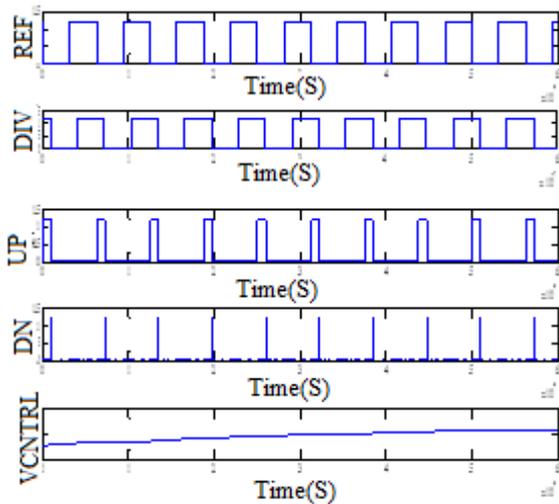


Fig. 12. When F_{ref} falling edge leads F_{div} rising edge

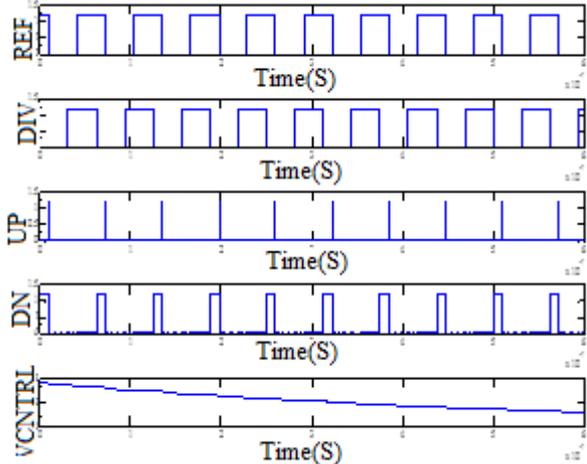


Fig. 13. When F_{ref} falling edge leads F_{div} rising edge

6.3 VCO Outputs

The heart of the PLL circuit is the voltage controlled oscillator. The circuit is designed to give a frequency of oscillation from 1 GHz to 4 GHz. The output signal of the VCO is shown in the Fig 14.

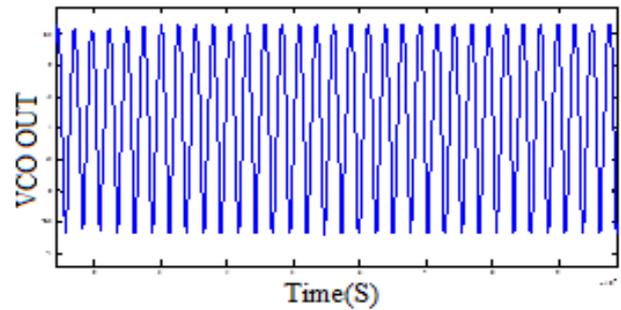


Fig. 14. VCO Output

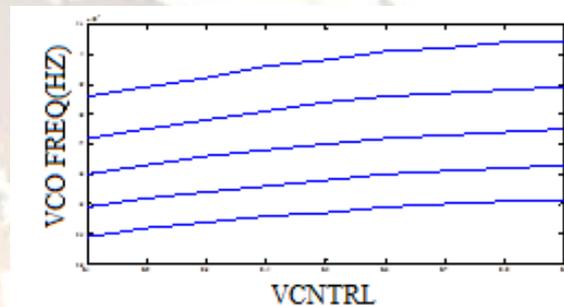


Fig. 15. VCO Characteristics

TABLE: 1 Phase noise measured.

Frequency(Hz)	Phase Noise, L(f) (dBc/Hz)
1000	-44.7276
10000	-71.99
100000	-100.324
1000000	-122.355

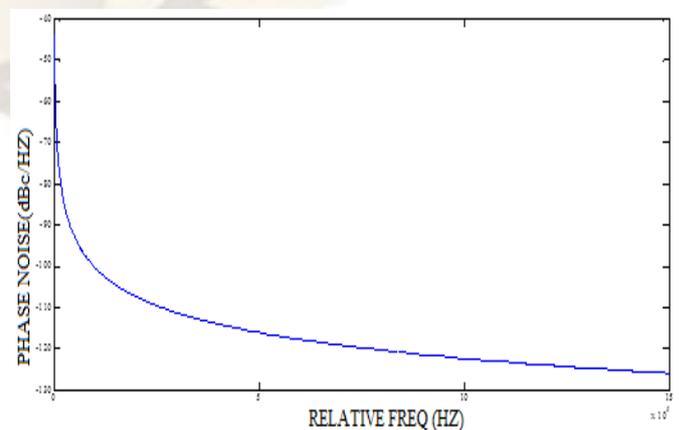


Fig. 16. VCO Phase Noise

RMS $J_{PER} = 8.1396$ pS at 3.86GHz [4].

6.4 Prescaler

The simulation result of the divider 1, divider2 are shown in Fig.17. The divider 1 divides the input by 4 and divider 2 is programmed as divide by 24 counter. Figure shows the whole divider circuit including the 2 dividers, inverter chains and buffers. The total delay of the circuit is found to be 106.35pS.

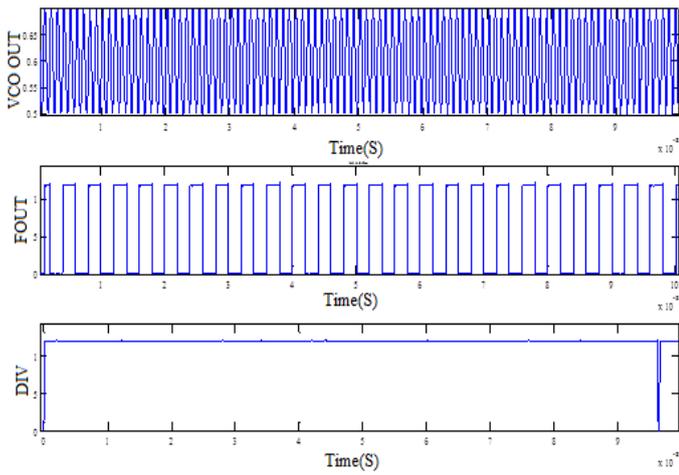


Fig. 17 Prescaler Output

6.5 Overall PLL Output

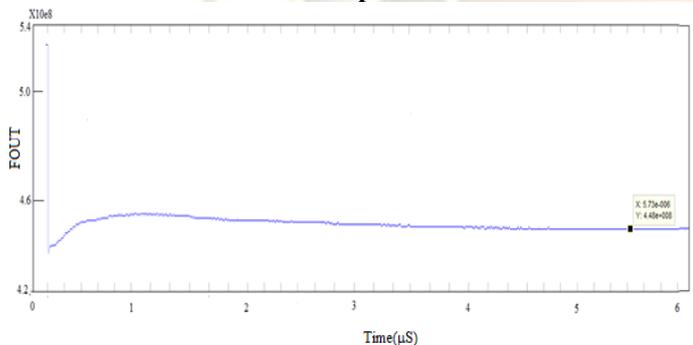


Fig. 18 PLL Output

The Fig: 17 shows the plot of output frequency versus time of the frequency synthesizer for an output frequency of 448MHz. From the figure it is clear that the output frequency (F_{OUT}) maintains constant after a time of $5\mu S$ which is the lock time of PLL.

VII. Conclusion

The phase frequency detector will decide the linearity and the pull-in range of the frequency synthesizer therefore the selection of PFD is very important in the design. The loop filter is very important for dynamic behaviour of the frequency synthesizer. Therefore the selection of proper value of resistor and capacitor will decide the speed and behaviour of the frequency synthesizer circuit. The

self-generated rms jitter of VCO at 3.86GHz, RMS $J_{PER} = 8.1396$ ps. The phase noise analysis results in some general design guidelines for the optimization of phase noise performance: The quality factor Q_L of the tank inductor should be as high as possible. The gain of the VCO has to be as small as possible in order to minimize flicker noise up-conversion. The flicker noise in the tail transistor is the main contributor to the close-in phase noise. For frequency synthesizers the design of divider circuit is very important and it will decide the range of frequency which can be applied in the frequency synthesizer. A wide range high speed programmable divider has been designed in 90nm GPDK technology. The design uses CML when necessary for high frequency operation. A 48 to 992MHz Frequency Synthesizer has been designed. The lock acquisition time is around $5\mu s$ for the system.

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