

Design, Implementation and Comparison of 8 Bit 100 Mhz Current Steering Dacs

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ABSTRACT

This paper presents the design, implementation and comparison of 8-bit current steering Digital-to-Analog Converters (DAC) architectures with 100MHz clock frequency. The circuit is designed in GPDK 90nm CMOS technology, with a supply voltage of 1.2V. The design is based on a differential current steering topology. The differential output of the DAC is loaded with two resistors and a full-scale differential voltage of 0.9Vpp is generated. Different current cell architectures are compared and Cascoding is selected for unit current cell design. One big advantage with this architecture is that almost all current goes through the output, and that makes this architecture power efficient. This type of converter is also superior when it comes to high-speed D/A converters. The reference current source is implemented using band gap reference circuit and verified the performance by varying temperature from -10°C to 70°C .

Keywords – Band gap reference, binary to thermometer decoder, cascode current source current steering, DAC architectures

I. INTRODUCTION

The world is getting digitized. The signal we perceive and retain is in analog form. In order to process the signal effectively we have to convert it into digital. Data Converters form the interface between analog world and digital world. Digital to Analog Converters (DAC's) represent the interface between digital processors and the real world. Wide varieties of DAC architectures are available, each having its own advantages. The most widely used design technique is the current steering type. It provides high speed operation and low power consumption compared to others. Most of the conventional current steering DAC's uses two dimensional current cell relocation techniques. Thereby many of the non-linearity errors can be reduced. A CMOS 8 bit 100MHz Current Steering DACs with band gap reference current circuit is presented in this paper. A unit current cell with ideal reference current source as Band Gap reference circuit is designed implemented and analyzed the circuit for supply voltage variation and temperature variation. This paper presents the design,

implementation and comparison of 8 bit 100MHz current steering DACs. Different current steering DAC architectures are described in section II. In section III we present the design of building blocks of the DAC architectures and the design of band gap reference current circuit. And we present the simulation results and comparison of DACs in sections IV and V.

II. DAC ARCHITECTURES

2.1 Binary weighted current steering DAC

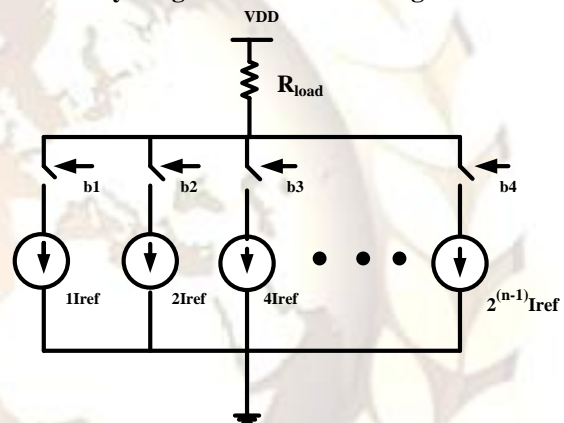


Fig 1 Current steering Binary DAC

The binary-weighted DAC is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision components are expensive, so this type of converter is usually limited to 8-bit resolution or less.

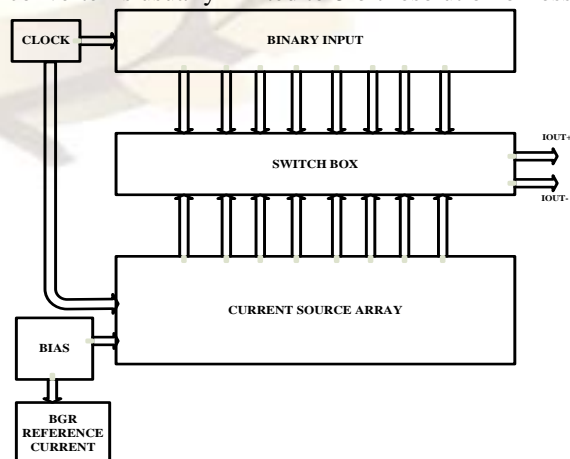


Fig 2 Block diagram of binary DAC

2.2 Thermometer coded current steering DAC

A current steering DAC consists of current sources, switching element and load resistor. For 8 bit DAC there are 255 current sources each with a MOS switch. These current sources are connected to the load resistor R_L via MOS switch. The switches are controlled by thermometer code. One dimensional architecture is difficult to implement. It requires a decoder with 8 input and 255 output binary to thermometer converter which is complex.

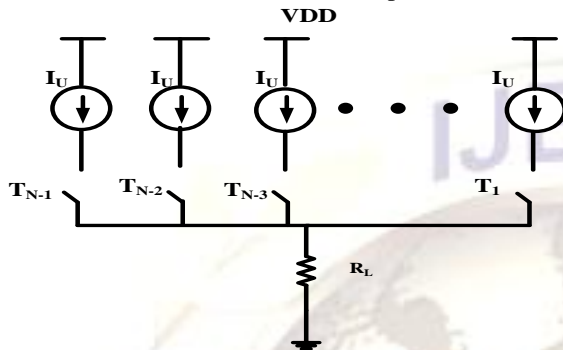


Fig 3 One dimensional current steering Thermometer coded DAC

To avoid the complexity of one dimensional architecture, we are using two dimensional architecture i.e., the 8 bit binary input is divided to two sets, 4bit LSB and 4bit MSB. Two decoder sets, one for row selection and other for column selection. The current cells are arranged as 16 x 16 array. The current cells contain analog part and digital part. Digital section turns on the current source according to the row and column input. The current sources are connected to the output node via MOS switches, which are controlled by the input code. Therefore, the output current of the DAC is proportional to the input code.

The circuit incorporates 4 bit binary to thermometer decoder, PMOS cascode current source with a digital logic for turning on the current source, a current mirror circuit for biasing the current source and transimpedance amplifier to convert the output current to voltage. In thermometer coded DACs, the digital input code is converted into a thermometer code, which controls the switches. The DAC is fully differential.

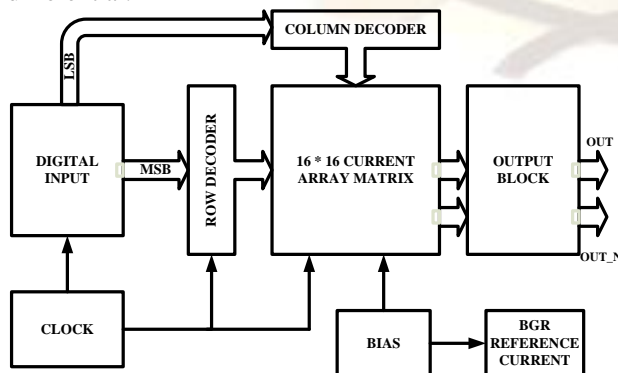


Fig 4 Two dimensional Current Steering DAC

2.3 Segmented architecture

To improve the performance of DAC segmented architecture is used. Usually this architecture is preferred for resolution greater than 8 bits. In this, two or more DACs may be combined in a single higher resolution DAC to give the required performance. These DACs may be of the same type or of different types and need not each have the same resolution.

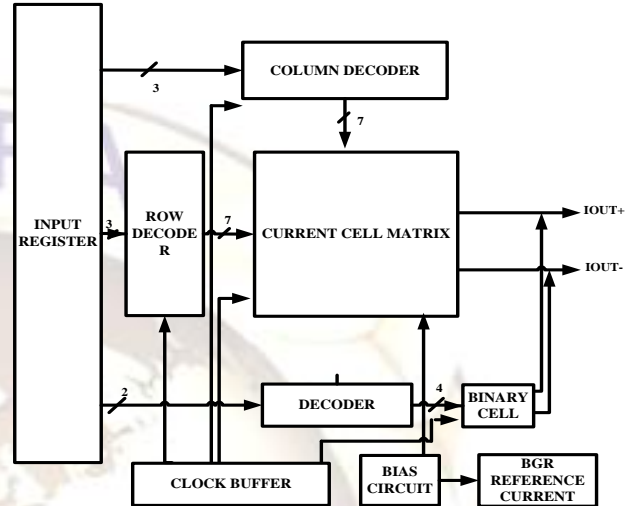


Fig 5 Segmented Current Steering DAC

In this architecture, one DAC handles the MSBs, another handles the LSBs, and their outputs are added in some way. The process is known as "segmentation," [2] and these more complex structures are called "segmented DACs".

The digital input is firstly clocked into the decoder. Column decoder receives the first 3-bit thermometer-code MSBs, and the row decoder receives the following 3-bit thermometer codes, the last two binary-weighted bits are sent to the decoder for the 2-bit LSBs. There are 64 cells in the main matrix and four smaller one in the small matrix.

III. BUILDING BLOCKS

3.1 Unit current Source

The unit current source has a large influence in the performance of current steering DACs. The main issues in high-speed, high-resolution DACs design are the mismatches in current source. The performance of the DACs is mainly limited by three factors: 1) output node voltage fluctuation of the current source due to improper switching of transistors 2) charge feed through 3) imperfect synchronization of the control signal of the current switching transistors. The unit current cell is most important factor of DAC, because the output impedance and dynamic performance of DAC is mainly affected by the current source matching.

The advantage of PMOS is that the output sources current and provides a signal which is above ground in a single-supply system. MOS act as current

source in saturation region. In order to provide high output impedance and high SFDR cascode PMOS current source is used. A cascode configuration is used to isolate the current source transistor from the voltage fluctuation at the common node. A small sized cascode transistor is used to shield the large current source transistor.

PMOS switches are used instead of NMOS, since when using PMOS switches the VGS value will not be altered due to the output node voltage changes. But this topology suffers from the charge feed through problem. The charge induced through the gate-drain capacitive coupling between the control signal node and the output of the DAC is translated in a voltage step at the output, which affects the dynamic performance of the DAC. To reduce the charge feed through problem a CFT transistor is connected between the switch and the output node. This will isolate the switches from the output node thereby reducing the charge feed through effect.

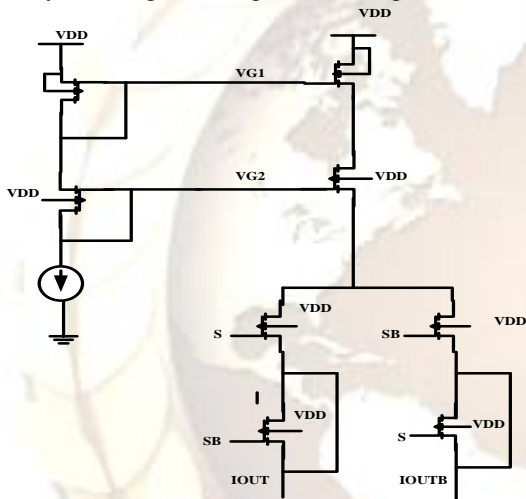


Fig 6: PMOS current cell with bias circuit

The current mirror circuit is connected to the PMOS current cell thereby producing required unit current. With the help of cascode transistors, the channel length modulation effect is eliminated in cascode current mirror and output impedance is large due to cascode transistor present in circuit.

3.2 Binary to thermometer decoder

Although the thermometer codes need much more bits than their counterparts, especially when bit is large, they have advantages in only changing one bit every time to avoid glitches. For example, when binary code switches from 0111 to 1000, four bits change simultaneously and this may cause glitches. While thermometer codes, switching from 000 0000 0111 1111 to 000 0000 1111 1111, only change one bit and avoid glitches effectively.

T1=B1+B2+B3+B4 (LSB)
 T2=B1+B2+B3
 T3=B1+B2+B3*B4
 T4=B1+B2

T5=B1+B2*(B3+B4)
 T6=B1+B2*B3
 T7=B1+B2*B3*B4
 T8=B1
 T9=B1*(B2+B3+B4)
 T10=B1*(B2+B3)
 T11=B1*(B2+B3*B4)
 T12=B1*B2
 T13=B1*B2*(B3+B4)
 T14=B1*B2*B3
 T15=B1*B2*B3*B4 (MSB)

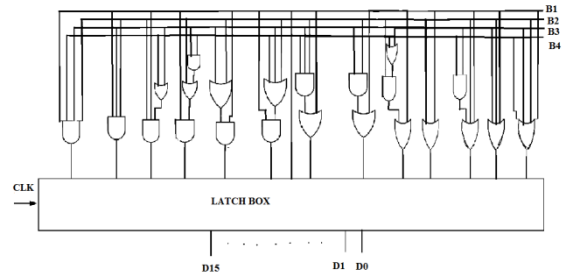


Fig 7 Four bit binary to thermometer decoder with latch

Output of decoder is applied to current cell matrix through latch block which consists of 15 latches in order to synchronize decoder outputs with the clock. This will improve the performance of DAC. The glitches or difference in arrival of outputs of decoder will affect the dynamic performance of DAC.

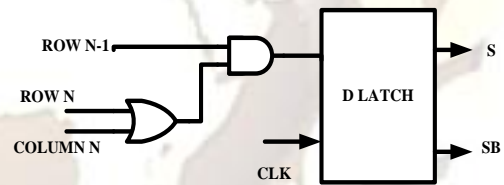


Fig 8 Digital decoding logic

Digital decoding logic will select the current source to be turned on corresponding to the thermometer code.

Design 3 bit binary to thermometer decoder for 6+2 segmented architecture.

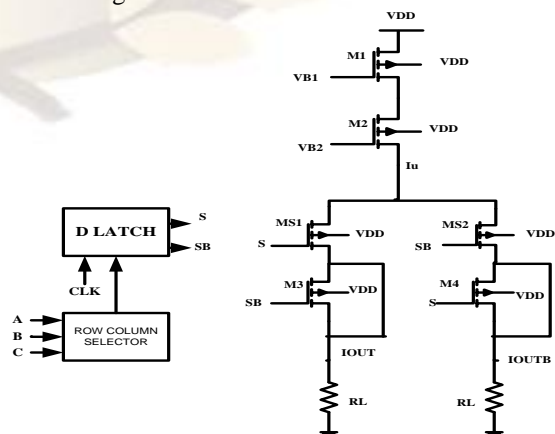


Fig 9 Current cell Schematic of thermometer DAC

3.3 Transimpedance amplifier

The output of current steering DAC is current. In order to convert current to corresponding voltage a transimpedance amplifier is used. This will act as an output buffer which will guarantee low impedance node at the output of the DAC. If no buffer is used, DAC will be sensitive to low output impedance. SNDR and SFDR depends on the conductance ratio of the current source. With an output buffer, load conductance becomes zero due to the virtual ground at the input of the amplifier.

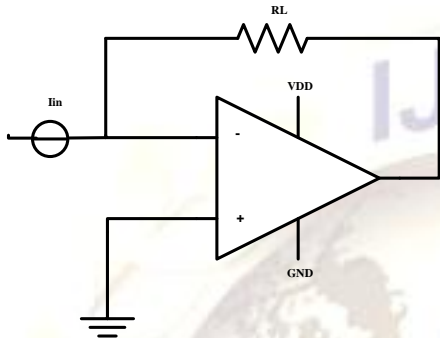


Fig 10 Transimpedance amplifier

$$V_{out} = I_{in} * R_L$$

Opamp: A single stage opamp is designed with a gain of 44dB. This opamp is used for implementing transimpedance amplifier which converts current to voltage.

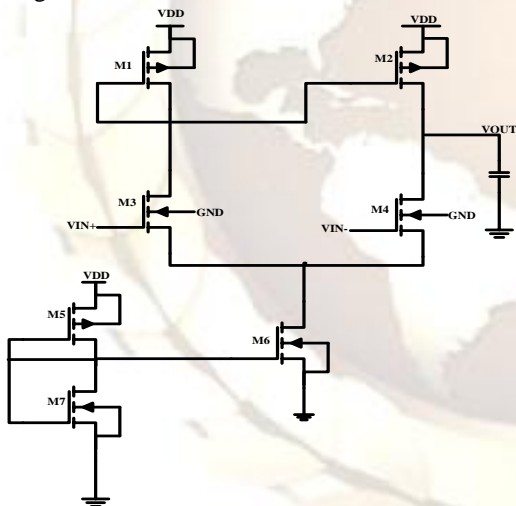


Fig 11 Single stage opamp

3.4 Band gap reference current circuit

Analog circuits incorporate a large number of references, current references as well as voltage references. Major objective of these types of circuit is to achieve dc voltages or dc current independent of temperature, supply voltage and process parameters variations. Designed a bandgap reference circuit for 78uA and analyzed the circuit for temperature variation from -10°C to 70°C. The variation in current is ±2.4uA.

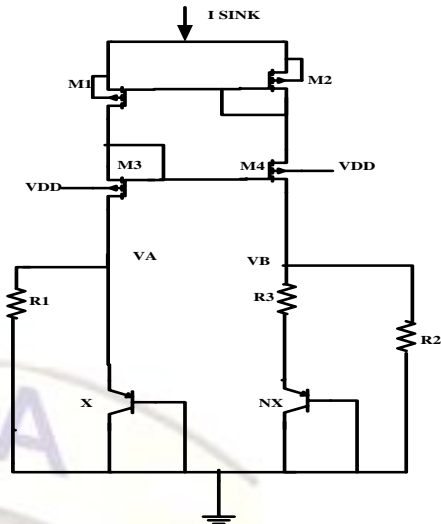


Fig 12 Band gap reference current circuit

IV. SIMULATION RESULTS

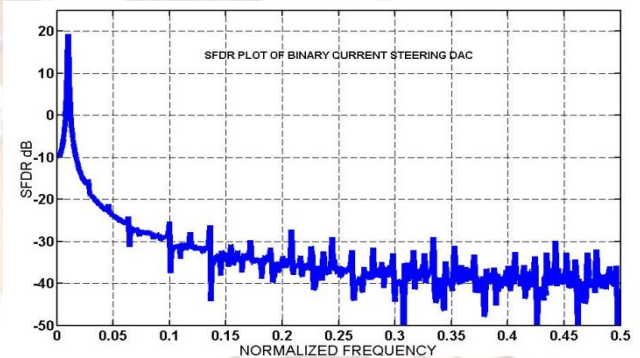


Fig 13 SFDR plot of 8 bit binary DAC

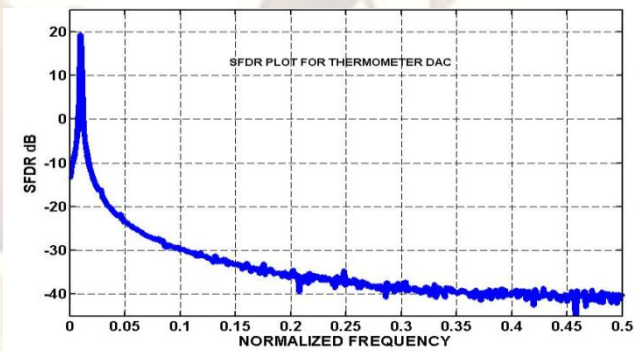


Fig 14 SFDR plot of 8 bit Thermometer DAC

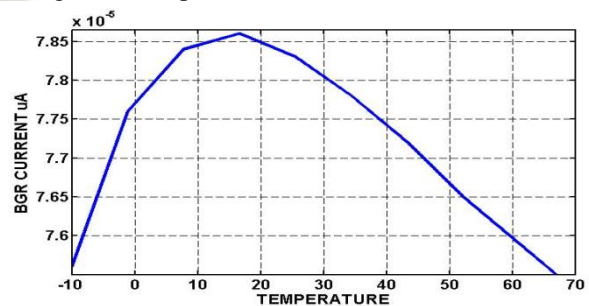


Fig 15 Band gap reference current variation with respect to temperature variation in Matlab

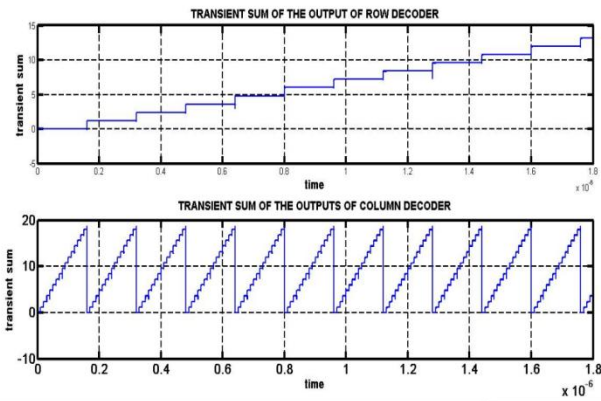


Fig 16 Transient sum of row and column decoder for ramp input

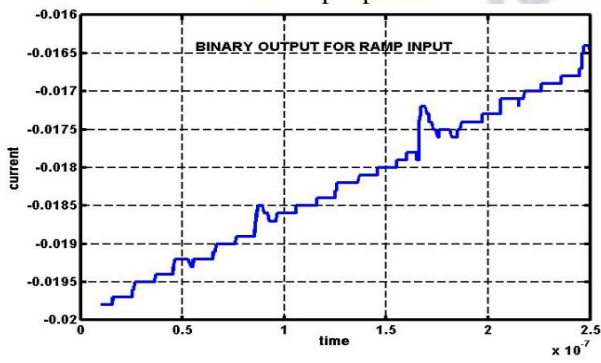


Fig 17 Binary output for ramp input

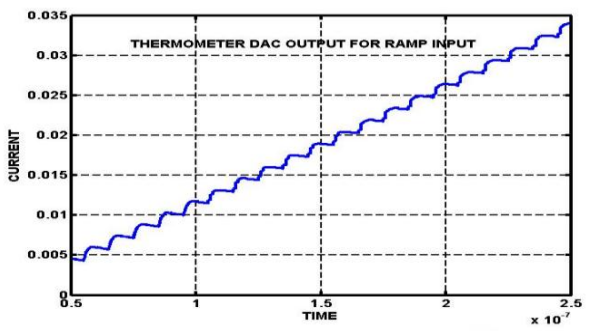


Fig 18 Thermometer output for ramp input

V. COMPARISON

	BINARY	THERMOME TER
PROCESS	90nm	90nm
RESOLUTION	8 BIT	8 BIT
SAMPLING FREQUENCY	100MHz	100MHz
VDD	1.2V	1.2V
Fin	0.9MHz	0.9MHz
INL	0.3 LSB	0.3 LSB
DNL	0.78LSB	0.23LSB
SFDR	46 dB	51 dB
settling time	4ns	4.2ns
Output swing (RL= 50Ω)	0.89Vpp	0.9Vpp

TABLE 1. Static and Dynamic performance of DACs

From the simulation results we can see that binary DAC output contains lots of glitches, in the case of thermometer coded DAC output has no glitches. Noise is more in binary DAC which effects the performance of DAC. DNL errors are much reduced and SFDR is improved in thermometer DAC. As input frequency increases with 100MHz as sampling frequency, the SFDR get attenuated. Binary DAC is faster than Thermometer DAC. The glitch energy is high at mid code transition of binary DAC.

VI. CONCLUSION

High-speed D/A converters use current steering architecture. It only involves the current steering rather than charge transfer or charging/discharging. Binary weighted current steering DAC is simple and fast, needs no decoding logic. Hence this architecture is compact and efficient. But the main problem faced by this architecture is large DNL error, less monotonic, can be used up to only 10 bits. Lots of glitches in the output which affect the performance of DAC. In binary weighted DACs due to the large ratio between the LSB and the MSB, it is difficult to synchronize the switching. The output can change by substantially more than 1LSB, which gives rise to a glitch. To improve the performance of DAC, a decoder for converting the binary code to the thermometer code is used. The thermometer code will control the switches of the current source according to the input code. This architecture utilizes a number of equal-size elements. Thereby glitches is completely reduced, hence improving the performance of DAC. SFDR, DNL of DAC is improved by using thermometer coded architecture. The main drawback of this architecture is can be used only for low resolution, less than 8. Otherwise the encoding circuit becomes too large. This lead to larger circuit complexity. Hence for high resolution DAC we c use combination of both architecture, Segmented. MSBs are implemented using thermometer DAC and LSB's using binary DAC. Latches are used to synchronize the circuit operation. The comparison of binary current steering DAC and Thermometer coded current steering DAC is explained in this paper. Here in binary DAC, instead of using different current sources for each bits we used a unit current source connected in parallel to achieve the required current value to avoid current source mismatches. Band gap reference current circuit is used instead of ideal current source hence area of the DAC is reduced. Analyzed the Band Gap circuit performance with respect to temperature variation. From the analysis, thermometer coded current steering DAC has more advantages than binary DAC. For high resolution, thermometer DAC is not feasible since the design is

complex. Hence for high resolution DAC, segmented DAC which is the combination of binary and thermometer architecture can be used.

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