

Design of Enhanced Power Gating Technique to Reduce Leakage Power and Ground Bounce Noise for CMOS Applications

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Abstract

In CMOS integrated circuit design there is a trade-off between static power consumption and technology scaling. Leakage power accounts for an increasingly larger portion of total power consumption in deep submicron technologies. Recently, the power density has increased due to combination of higher clock speeds, greater functional integration, and smaller process geometries. As a result static power consumption is becoming more dominant. This is a challenge for the circuit designers. However, the designers do have a few methods which they can use to reduce this static power consumption. But all of these methods have some drawbacks. In order to achieve lower static power consumption, one has to sacrifice design area and circuit performance. In this paper, we propose a new method to reduce static power in the CMOS VLSI circuit using dual stack approach without being penalized in area requirement and circuit performance.

Keywords—dual stack approach, state saving technique, stack effect, dual V-th, static power reduction

I. INTRODUCTION

A large proportion of digital functional blocks are only active for a small fraction of time. When the functional block is not operating, leakage still occurs. In deep submicron technologies, such a phenomenon is aggravated due to the reduced threshold voltage from scaling. Leakage power makes up close to 40% of total power consumption in today's high performance microprocessors. Leakage power reduction becomes the key to a low power design. MOS technology feature size and threshold voltage have been scaling down for decades for achieving high density and high performance. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has

become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper.

II. FULL ADDER CIRCUITS

Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous in pass transistor logic. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability. The conventional CMOS 28 transistor adder, as shown in Figure 1, is considered as Base case throughout this paper. All comparisons are done with Base case. Transistor sizes are specified as a ratio of Width/Length (W/L). It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter. Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. The sizing of each block is based on the following assumption. These sizing will reduce the standby leakage current greatly because sub-threshold current is directly proportional to the Width/Length ratio of transistor. On the other hand, these reduced sizes reduces the area occupied by the circuit. This will reduce the silicon chip area and in turn reduction in the cost.

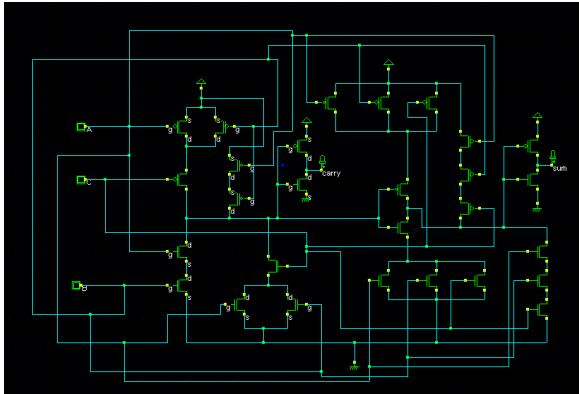


Figure 1. Conventional CMOS full adder

Modified adder circuit of Design 2 shown in Figure 3, the W /L ratio of PMOS is 1.5 times that of W /L ratio of NMOS and each block has been treated as an equivalent inverter. The goal of this design is to reduce the standby leakage power. Further compared to the Base case, Design 1 and Design 2, ground bounce noise produced when a circuit is connected to sleep transistor is reduced.

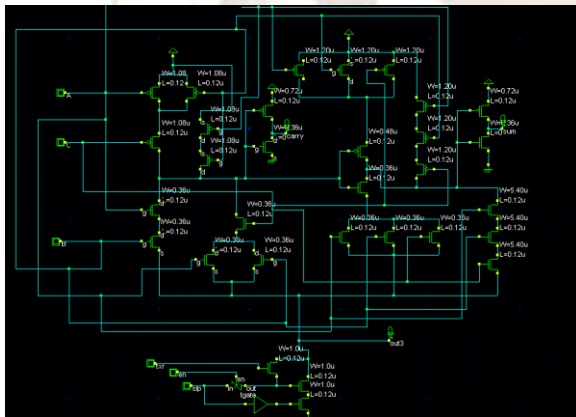


Figure 2. Full adder (Design I) circuit with diode based gating

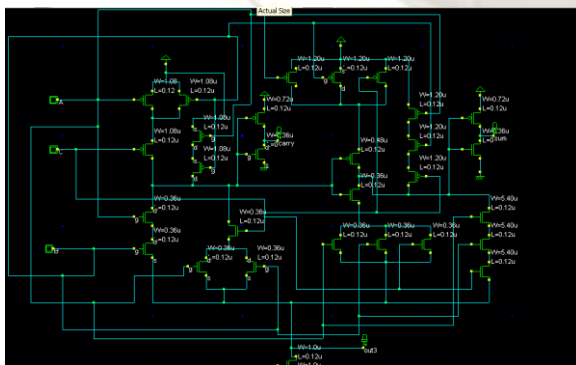


Figure 3. Full adder(Design2) circuit with stacking based gating

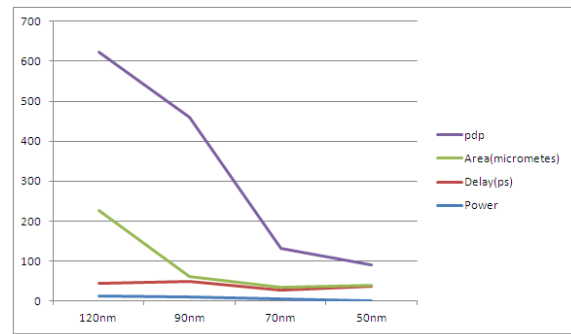


Figure 4. Conventional CMOS power and area calculations.

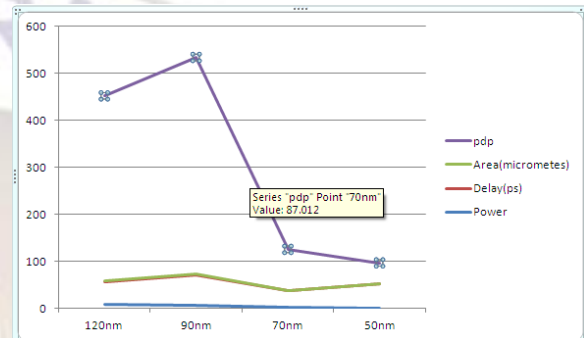


Figure 5. Design 1 power and area calculations.

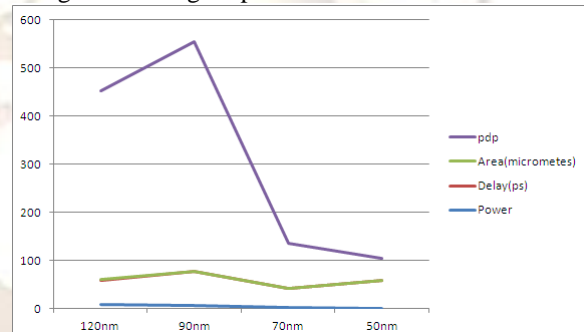


Figure 6. Design 2 power and area calculations.

III. PERFORMANCE ANALYSIS

A. Active Power

Power dissipated by the circuit when the circuit is in active state is termed as Active power. Input vectors are fed into the circuit and the average power dissipation is measured. Almost all of the input combinations are considered for simulation. Same input vector combinations have been given to the all three designs- Base case, Design 1 and Design2, and a comparison has been made for the same in both 90nm and 70nm technology.

B. Standby leakage power

Standby leakage power is measured when the circuit is in Standby mode. Sleep transistor is connected to the pull down network of 1 bit full adder circuit. Sleep transistor is off by asserting an input 0v. Size of a sleep transistor is equal to the size of largest transistor in the network (pull up or pull-down) connected to

the sleep transistor. The sleep transistor size in Design 1 and Design2 is reduced due to the resizing of the adder cells in proposed circuit. Standby leakage power is measured by giving different input combinations to the circuit. Standby leakage is greatly reduced in both Design 1 and Design2 and for both 90nm and 70nm

IV. PROPOSED DESIGN

Four bit adder active and standby power

Full adder cells shown in Figure 1, 2 and 3 are used to design 4-bit ripple carry adder. 4-bit adders in all three designs- Conventional, Design 1 and Design2, for both 90nm and 65nm technology, are constructed. The active power and standby power are calculated. Active power is calculated by setting the Select terminal of the adder to logic high and Standby power is calculated by setting the Select terminal to 0V. Comparison of active and standby power of all the designs in both 90nm and 70nm as shown in figure.

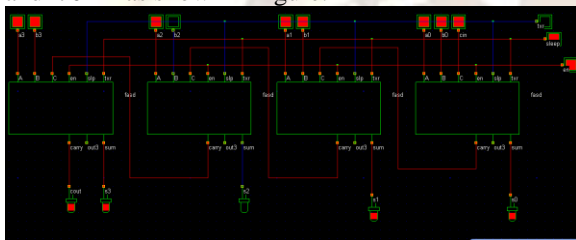


Fig6: four bit full adder design for diode based power gating

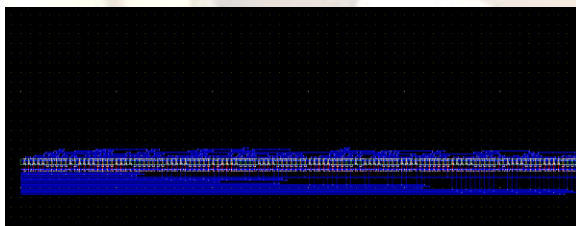


Fig7: four bit full adder layout for diode based power gating

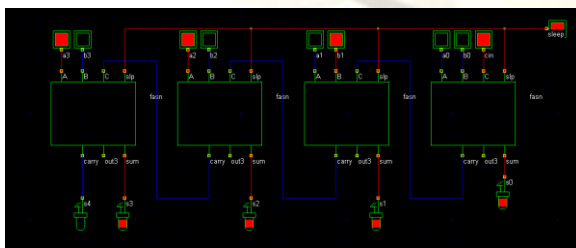


Fig8: four bit full adder design of stacking based power gating

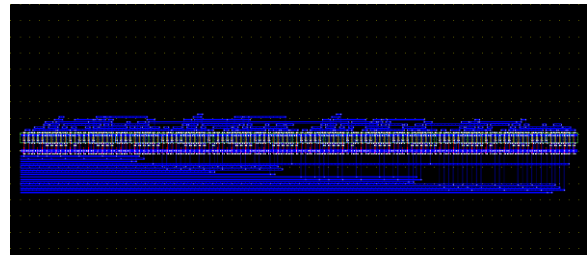


Fig9: four bit full adder layout of stacking based power gating

V. SIMULATION METHODOLOGY

We compare the dual sleep technique with previous approaches explained earlier namely; conventional cmos, conventional cmos with sleep transistor, and ripple carry adder. Thus, we compare these design approaches in terms of power consumption (dynamic and static), delay and area

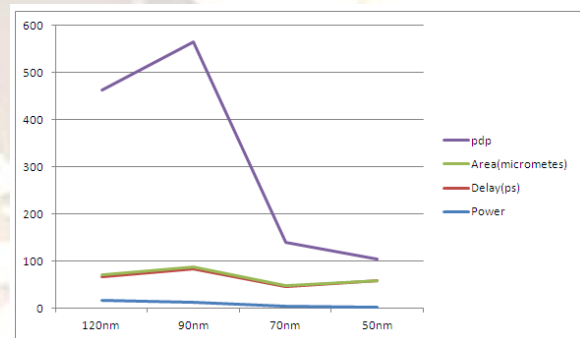


Fig 11: four bit full adder power & area calculations for design 1

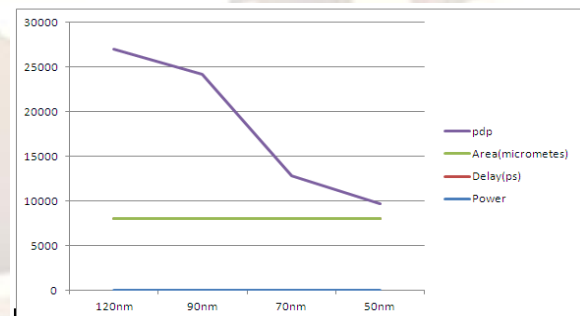


Fig12: four bit full adder power & area calculations for design 2

VI. CONCLUSION

Miniaturization of CMOS technology achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient methodology for reducing leakage power in VLSI design. Our Dual sleep approach shows improved results in terms of static power, dynamic power and power delay product. It gives the CMOS circuit designers another option in designing integrated Circuits more efficiently.

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