K.R.Surendra, K.Venkatramana Reddy / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 4, Jul-Aug 2013, pp.193-199

# Implementation Of Low Power SRAM By Using 8T Decoupled Logic

**K.R.Surendra, K.Venkatramana Reddy**
(Department of ECE, M.Tech Student, SVCET, Chittoor, India)
(Department of ECE, Asst. Professor, SVCET, Chittoor, India)

## ABSTRACT

**We present a novel half-select disturb free transistor SRAM cell. The cell is 6T based and utilizes decoupling logic. It employs gated inverter SRAM cells to decouple the column select read disturb scenario in half-selected columns which is one of the impediments to lowering cell voltage. Furthermore, "false read" before write operation, common to conventional 6T designs due to bit-select and word line timing mismatch, is eliminated using this design. Two design styles are studied to account for the emerging needs of technology scaling as designs migrate from 90 to 65 nm PD/SOI technology nodes. Namely we focus on a 90 nm PD/SOI sense Amp based and 65 nm PD/SOI domino read based designs. For the sense Amp based design, read disturbs to the fully-selected cell can be further minimized by relying on a read-assist array architecture which enables discharging the bit-line (BL) capacitance to GND during a read operation. This together with the elimination of half-select disturbs enhance the overall array low voltage operability and hence reduce power consumption by 20%–30%.**

**The domino read based SRAM design also exploits the proposed cell to enhance cell stability while reducing the overall power consumption more than 30% by relying on a dynamic dual supply technique in combination of cell design and peripheral circuitry. The feasibility of the cell and sensitivity to sense Amp timing has been proved by fabricating a 32 kb array in a 90-nm PD/SOI technology.**

***Keywords***-Column-decoupled, differential/domino read, half-select, low power 8T, SRAM, stability.

## I. INTRODUCTION

DEVICE miniaturization and the rapidly growing demand for mobile or power-aware systems have resulted in an urgent need to reduce power supply voltage (Vdd). However, voltage reduction along with device scaling is associated with decreasing signal charge. Furthermore, increasing intra-die process parameter variations, particularly random dopant threshold voltage variations can lead to large number of fails in extremely small channel area memory designs. Due to their small size and large numbers on chip, SRAM cells are adversely affected. This trend is expected to grow significantly as designs are scaled further with each technology generation [1]. Particularly, it conflicts with the need to maintain a high signal to noise ratio, or high noise margins, in SRAMs and is one of the major impediments to producing a stable cell at low voltage. When combined with other effects such as narrow width effects, soft error rate (SER), temperature, and process variations and parasitic transistor resistance, the scaling of SRAMs becomes increasingly difficult due to reduced margins [2].

The plot indicates that the SRAM area scaling drops below 50% for 32-nm technology and beyond. Furthermore, voltage scaling is virtually nullified. Higher fail probabilities occur due to voltage scaling, and low voltage operation is becoming problematic as higher supply voltages are required to conquer these process variations. To overcome these challenges, recent industry trends have leaned towards exploring larger cells and more exotic SRAM circuit styles in scaled technologies.

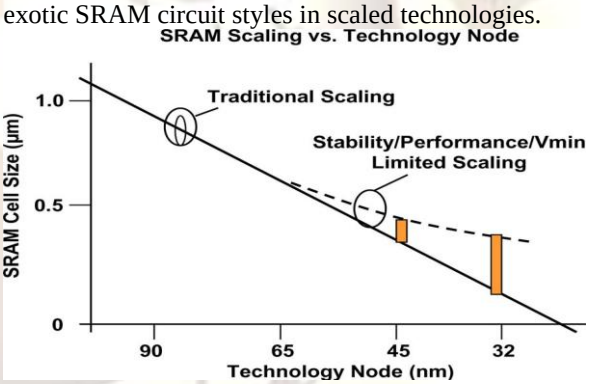


Fig. 1 illustrates the saturation in the scaling trend (dashed line) of SRAM cells across technology generations.

Examples are the use of write-assist design [3], read-modify-write [4], read-assist designs [5], and the 8T register file cell [6], [7]. Conventional 6T used in conjunction with these techniques does not lead to power saving due to exposure to half select condition [3], [4].

Column select/half-select is very commonly used in SRAMs to provide SER protection and to enable area efficient utilization and wiring of the macro. Nevertheless, the use of column select introduces a read disturb condition for the unselected cells along a row (half-selected cells), potentially destabilizing them. In this paper we present a new column-decoupled 6T-based SRAM cell where read

disturb is eliminated for column selected/ half selected cells [5], [8]. The decoupling logic uses two additional devices and henceforth we will refer to the cell as the 8T-column-decoupled-cell (8T-CDC). We study the cell in the presence of two design styles: namely, sense Amp-based read peripheral circuitry that was typical for the 90-nm node, and domino read peripheral circuitry [9] for 65 nm and beyond. In a sense Amp-based read design, the read disturb condition is further minimized for the selected cells by the use of a sense-amp architecture which actively discharges the selected cell(s) BL to GND, thereby eliminating the source of disturb. Through a combination of accurate simulations and hardware (HW) data acquired from a 32 kb SRAM macro, a path towards low voltage SRAM operation of the cells is shown, and the design is shown to enhance read stability and half-select stability problems thereby enabling improved .

However, process variations are increasingly affecting sense Amp designs in PD/SOI designs and it is natural to converge to domino-read designs [9]. In domino read-based designs, the column-decoupled cell still maintains guard against half-select cell disturbs. However, with the absence of read-assist feature in domino designs, we need to account for the read disturb on fully-selected cells. For this, we propose a dynamic dual supply header design that leverages the benefits of the column decoupled cell design and helps save power. As is the case with traditional dual supply techniques, the proposed header design maintains separate cell supply (Vcs) and logic supply (Vdd). However, unlike traditional techniques, the dynamic cell supply changes based on the column selection status. The new header design sets: 1) the selected cell columns at a voltage supply higher than the logic one for improved read stability and 2) maintains a low supply for half-select cells since half-select disturbs are not an issue for this design. Hence, we rely on the column-decoupled cell to enable a simplified low-power high performance column-decoupled domino read based design. We implement the design using simplified bit-select logic and dynamic supply headers with shorter bitlines. In what follows, we provide a thorough analysis into the design modifications compared to the traditional 6T dynamic supply designs. We also highlight the advantages this methodology brings in terms of lower power and yield improvements.

A localized gated inverter consisting of two additional transistors, T1 and T2, effectively perform a logical “AND” operation between the column select signal (BDT0) and the decoded row, or global wordline, GWLE. The output of the inverter is the local wordline signal (LWLE0). The local wordline is ON only when both the column and row are selected (i.e., for fully selected cells only); hence, as illustrated in the waveforms of Fig. 3, LWLE0 of the selected columned turns ON while LWLE1 of the half-selected column remains low.

## II. 8T COLUMN DECOUPLED CELL

### 2.1 Proposed 8T-CDC

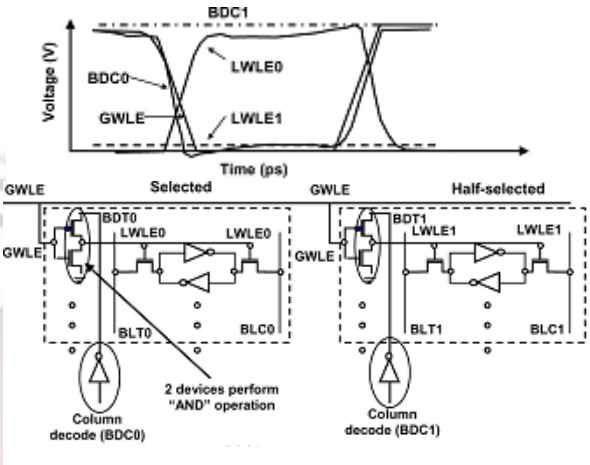


Fig. 2 illustrates a new 8T-CDC SRAM cell (inside dashed rectangle) with a gated wordline which enables the decoupling of the column/half-select condition [5] hence eliminating half select stability fails.

This ensures that the local wordline for only the selected cells is activated, thereby effectively protecting the half-selected SRAM cells from the read disturb scenario that exists in 6T cell due to wordline sharing. Alternatively, it is possible to swap the input and supply pairs of the gated inverter; however this comes at the cost of extra delay stage and power. The advantages of the 8T-CDC cell are as follows: 1) conforming with traditional 6T requirements in terms of (a) allowing the designer to integrate it in a column select fashion and (b) offering/maintaining SER protection while 2) maximizing array efficiency, 3) eliminating the read disturb to the unselected cells, and 4) reducing power with simplification in peripheral logic.

Fig. 3(a) shows a layout view of the 8T-column-decoupled cell in a 90-nm PD/SOI technology. The two extra devices are integrated on top of an existing 6T cell to allow for easy cell mirroring and integration into an array topology. The addition of the two new transistors results in a cell area increase of 40% (all in -direction). Through the use of higher level metallurgy to wire in the column decode (BDC) signal, the growth to the -direction of cell was not impacted. The increase to the – dimension of the cell causes a proportionate increase to the BL metal capacitance while maintaining the original diffusion capacitance contributed by the 6T cell. Column decode signal integrated with higher level metal. Area penalty can be further reduced to 30% via use of 6T thin cell integration in Fig. 3(b); further reduction can be achieved by use of non-DRC clean devices.

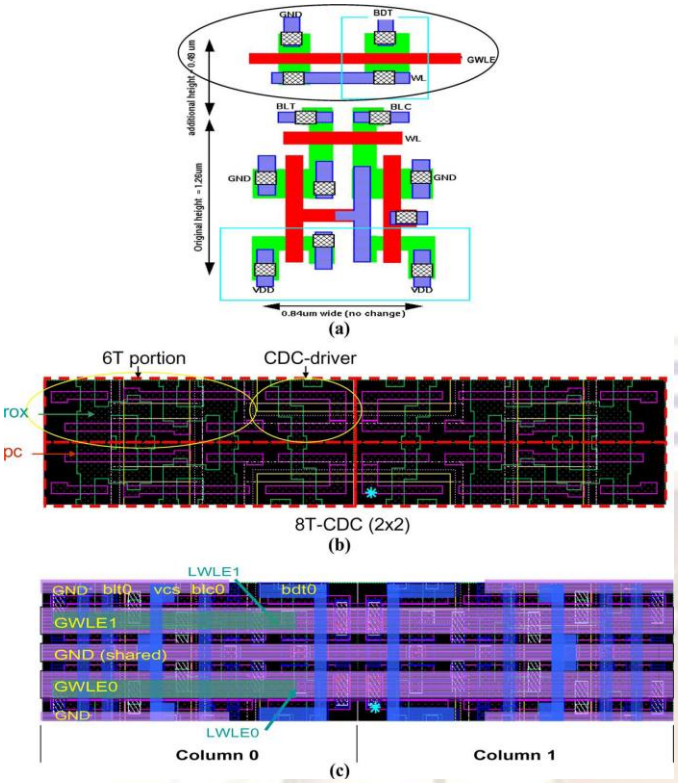


Fig. 3. Layout view of the new 8T-CDC SRAM cell for a (a) typical cell and a (b) 2 □ 2 thin cell front end of the line layout view and (c) back end of the line layout view to show ROX and GND sharing.

Fig. 3(b) and (c) presents the front end of the line (FEOL) and back end of the line (BEOL) layout view of 2 8T-CDC thin cell. The views illustrate how the recessed oxide (ROX) and power buses are shared. The area can be reduced further to 30% by utilizing thin cells as presented in this paper without degrading the bitline capacitance.

### 2.2 Timing Advantages: Elimination of "False Read" Before Write

During the write operation in conventional 6T SRAM, when the wordline precedes ahead the column-select in timing, then the cell starts reading the data [8]. When the bitline droops, "false read" before write happens [see Fig. 4(a)]. This is a disadvantage for conventional 6T SRAM. This particular drawback is overcome by the technique that is proposed here as illustrated in the Fig. 4(b); if the wordline arrives earlier than the column select it will be gated by the column select and thus "false read" before write does not ripple through the bitlines to the evaluation logic.

## III. SENSE AMPLIFIER BASED DESIGN

The 8T-CDC cell together with read-assist sense amp designs [5] can mitigate the read disturb problem both for selected and half-selected designs.

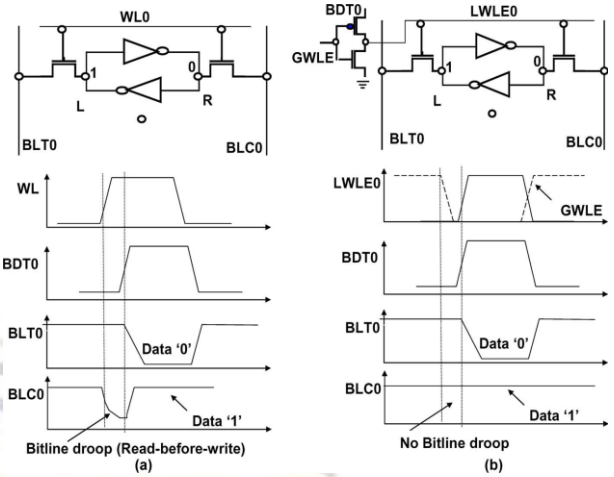


Fig. 4. (a) For conventional 6T SRAM, during write, when the wordline precedes ahead the column-select, the cell starts reading the data [8]. When the bitline droops, "false read" before write happens. (b) This particular drawback is overcome by the 8T-CDC cell; the early wordline (GWLE in dashes) will be gated by the column select and thus "false read" before write does not happen.

### 3.1 Read Assist Sense Amp Based Design

Fig. 5 illustrates the 8T-CDC cell design combined with read assist sense Amp. The sense amplifier is shared among multiple columns. In a typical sense Amp scenario, the bit switch (BDC), and the WL on the selected cells columns are turned off once enough margin is developed for the sense-amplifier to accurately resolve the BL differential. This is done to save ac power (prevents discharge of BL to GND) and to speed up sense-time (smaller capacitance for sense-amplifier to discharge). For this scenario, only the PFET transistor exists (solid bit switch PFET Fig. 7) and it closes during "Sense" to save power and perform faster sense. In a read-assist scenario the bit-switch PFET is converted to a complementary (dashed line) NFET and PFET bit-switch pair. The pair is kept open during the entire WL active phase. Consequently, the sense-amp and the cell discharge the BL completely during a sense-read operation [5]. Hence the sense amplifier "sees" the full BL capacitance during a read operation; it discharges the capacitance to GND, and the cell data is "written back". This helps minimize the amount of read disturb charge induced onto the cell from the bitlines. Temperature/K".

## IV. SENSE AMPLIFIER APPROACH ANALYSIS & RESULTS

To effectively evaluate the 8T-CDC cell, it was compared to two versions of a 6T cell within the same read disturb mitigating system. The first was a default 6T (106 cell) and the second a 40% larger 6T cell (149 cell); the latter is intended to compare functionality gains under similar design area constraints for 6T and 8T-CDC. It should be noted

that the cell devices within the 8T-CDC cell (PG, PD, PU) are identical to the 106 cell, while the 149 cell has devices that are 40% larger than the 106 cell. For each cell type, simulations were run using 90-nm PD SOI technology to determine the cell's sigma to fail as a function of voltage. Simulations were also performed to investigate the effect of SET timings and BL height on each cell type. Finally area and power tradeoffs were studied to determine optimum design points. Also a chip was fabricated and hardware results corroborate well with the simulations.

In a typical scenario, PFET bit-switch closes during sense to save power and perform faster sense. In a read-assist scenario true/comp (dashed line) NFET and PFET bit-switch pair is kept open during sense. Hence the sense Amp "sees" the BL capacitance; it discharges the capacitance to GND, and the cell data is "written back". This helps minimize the amount of read disturb charge.

### 4.2. Simulation Results

In the following analysis, cell and logic supplies are assumed the same. is minimum supply needed to maintain the desired cell yield. Fig. 6 shows the cell yield in sigma values for the three different cell options. For a BL height of 128 cells, clamped half-select condition, and a 10% of Vdd BL differential SET timing, the half-select stability fails dominate in 6T.

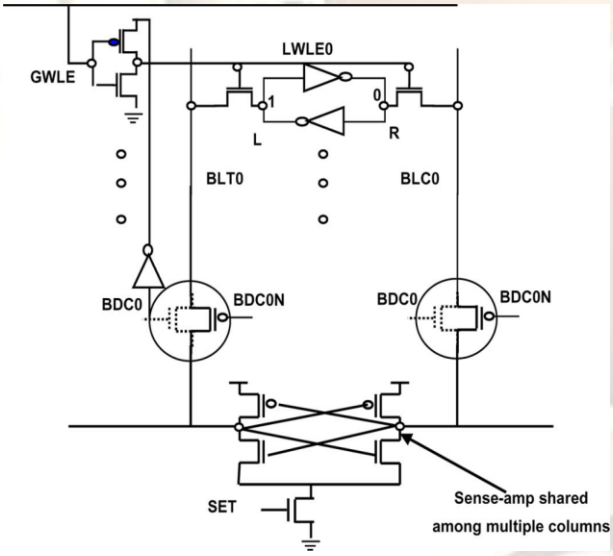


Fig. 5. Gated 8T-CDC cell design combined with read-assist sense Amp [5].

The 8T-CDC cell shows a marked improvement of 200 mV when compared to 6T (106 cell) and 80 mV compared to 6T (149 cell). The comparison was performed at the 5 sigma cell yield point. For unclamped (floating BL) half-select, the 8T-CDC curve remains unchanged; half-select is not an issue for the 8T-CDC cell, and read stability graph remains the same. A small improvement in (30 mV) for the two 6T cells is noticed due to relaxation in the half-select conditions for the 6T. This improvement increases for shorter BL heights (50 mV for 32 cells/BL) [5]. The effect of SET timing (for 8T-CDC) on yield sigma was investigated by advancing the SET signal earlier during the read cycle. Fig. 7 depicts this data for three different SET timings (10%, 7%, and 5% of supply BL differential). 8T-CDC cell improvement between 70 and 130 mV was observed compared to 10% margin (for the 7% and 5%, respectively); again we assumed 5 sigma yield point as the target for $V_{ddmin}$. Advancing SET timing will have no effect on for 6T versions as half-selected cells will not derive any benefit from the read disturb mitigating topology. Finally, the dependence of BL height for the unclamped case on cell was investigated and the results plotted in Fig. 8. It can be seen that to achieve a cell of 0.6 V (with 5 sigma yield), the 6T-106 cell cannot be used, the 6T-149 cell offers only one design option (32 cells/BL), while the 8T-CDC cell offers several options to the designer (32 to 128 cells/BL with 10% to 7% BL margin SET timings).

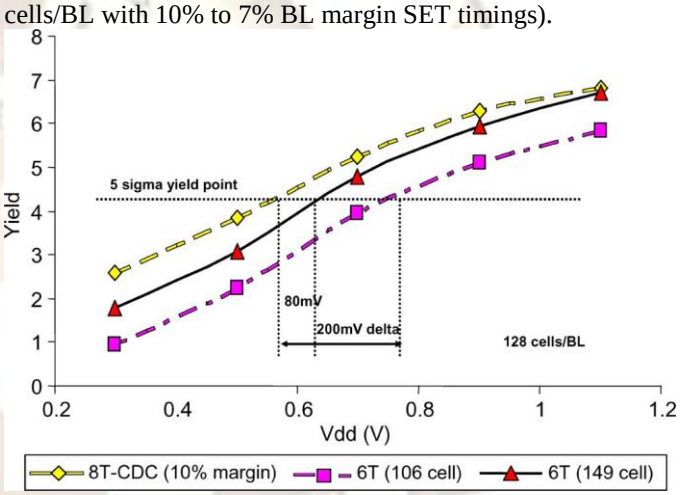


Fig. 6. Cell yield in sigma values versus Vdd. Clamped bitlines; load 128 cells/ bitline. Half-select stability fails dominate in 6T. Even sized-up 6T (6T-149) requires $V_{ddmin}$ increase of 80 mV and the regular 6T requires an increase of 200 mV.

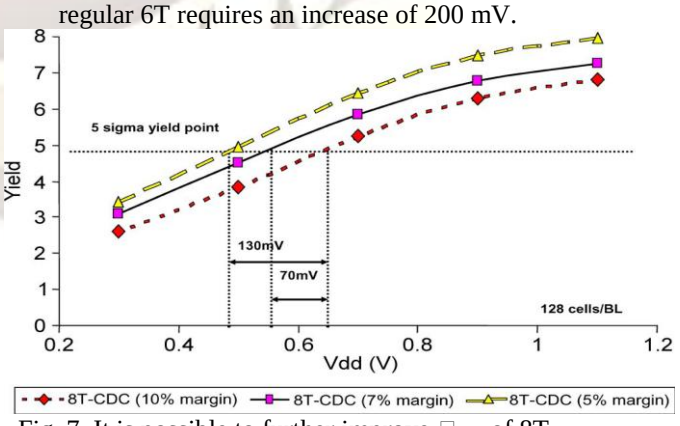


Fig. 7. It is possible to further improve □__ of 8T-CDC with earlier set arrival (due to lowering margin criteria of bitline drop voltage).

## V. DOMINO READ BASED DESIGN

In the following sections, we discuss the advantages of the proposed 8T-CDC design in the presence of domino read based architectures as well as the rationale behind these architectures.

As technology scales, sense-Amp devices suffer from Vt-mismatch and scaling becomes difficult particularly for PD/SOI technology designs due to hysteretic Vt variation. Thus, it is preferred to use large signal domino read circuitry [9]. During a domino read, the dual rail signals from the cell are amplified by skewed inverters to full rails. This eliminates the dependency on bitline differential which can be highly sensitive to Vt-mismatch and we refer the reader to [9] and the references within for a detailed overview of domino based read designs. However, the SRAM cell read disturbs and half-select problems are still critical in a domino read design. In what follows, we study the advantages of combining a decoupled half-select column design cell design with dynamic supply techniques for a 65-nm PD/SOI domino read-based design.

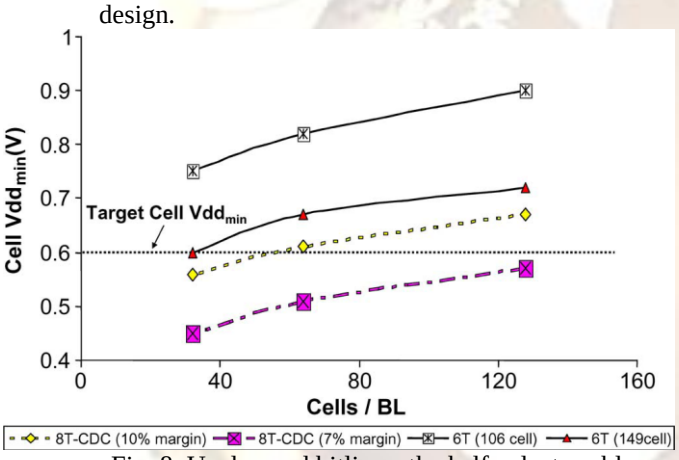


Fig. 8. Unclamped bitlines: the half-select problem still dominates in sized-up 6T-149 cell. For a target of 0.6 V the 6T (149) must operate with 32 cells/bitline, whereas the 8T-CDC offers multiple bitline height options.

Our goal is to exploit the elimination of half-select disturbs together with dynamic supply techniques for optimal yield and power. For this purpose, we propose new header designs for the dynamic supply suitable for the 8T-CDC cell. An overview of the targeted domino-read memory cross-section is illustrated in Fig. 9. Next, we revisit traditional circuit and peripheral logic for 6T domino designs and propose simplifications or modifications as well as novel dynamic header designs suitable for low-power 8T-CDC cell design.

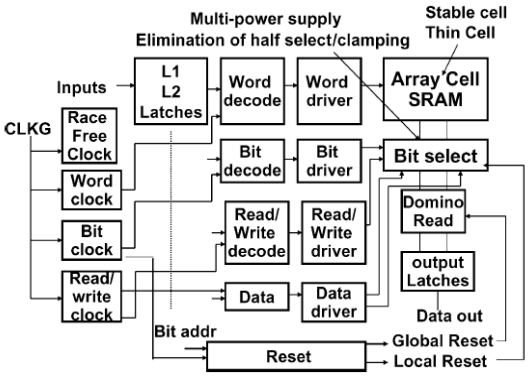


Fig.9. 8T-CDC-decoupled cell memory cross-section for domino read designs.

## VI. SIMULATION RESULTS

In this project we used DSCH [Digital Schematic] software for simulating the circuit and to generate the code, MICROWIND is used to extract the layout of the schematic diagram.

The following figure shows the schematic diagram, Layouts and Simulation results of 6T and 8T SRAM Cell using DSCH & MICROWIND.

### 6.1 SRAM 6T:

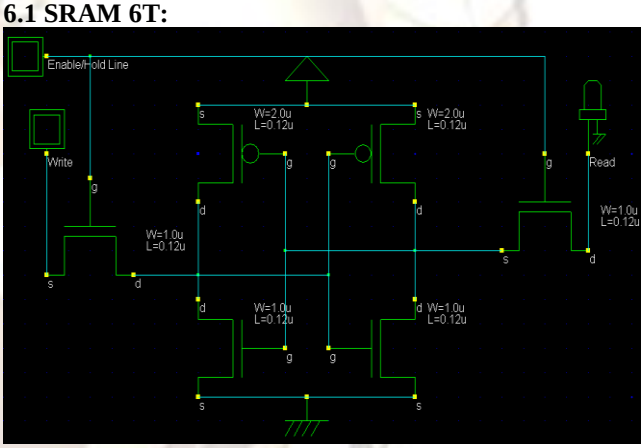


Fig: 6.1 Schematic diagram of one stage 6T SRAM

### 6.2 SRAM 6T LAYOUT:

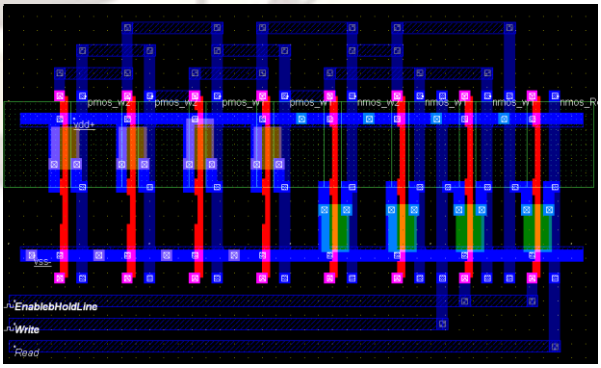


Fig: 6.2 Layout of 6T SRAM cell

**6.3 SRAM 6T PROPOSED:**

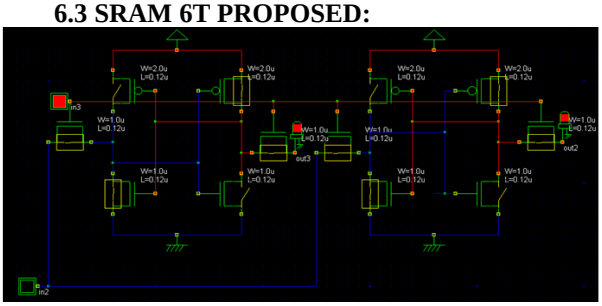

Fig 6.3 Schematic diagram of 2 stages 6T SRAM cell

**6.4 SRAM 6T PROPOSED LAYOUT:**

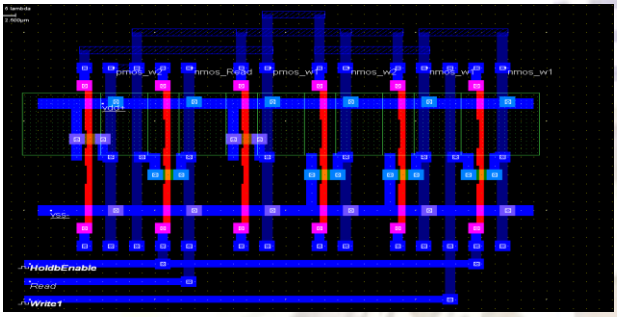

Fig: 6.4 Proposed Layout of 6T SRAM cell

**6.5 SIMULATION RESULT OF SRAM 6T:**

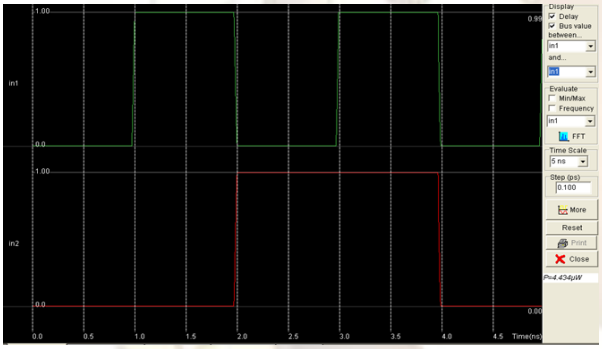

Fig: 6.5 Simulation results of SRAM 6T

**6.6 SRAM 8T:**

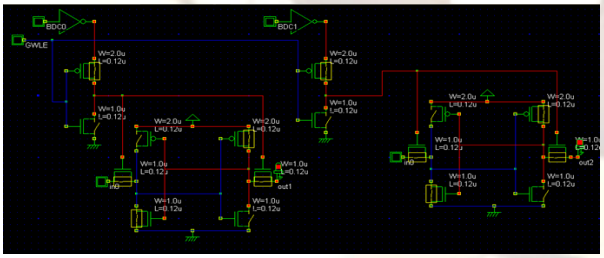

Fig: 6.6 Schematic diagram of SRAM 8T cell

**6.7 SRAM 8T LAYOUT:**

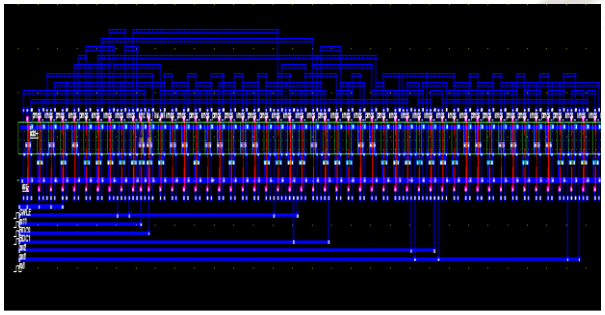

Fig: 6.7 Layout of proposed 8T SRAM Cell

**6.8 SIMULATION RESULT OF SRAM 8T:**

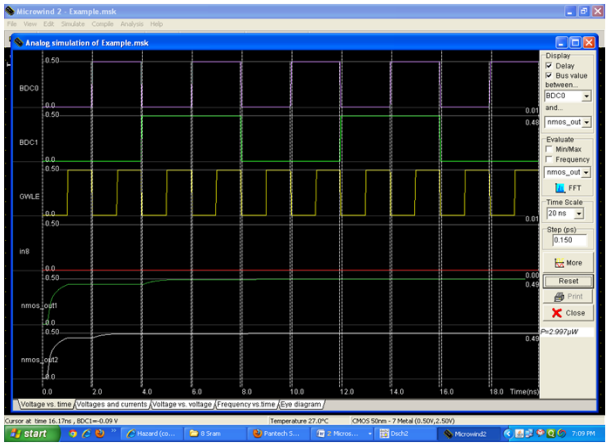

Fig: 6.8 Simulation results of SRAM 8T

## VII. CONCLUSION

We studied a novel 8T-CDC column-decoupled SRAM design. The half-select free design enables enhanced voltage scaling capabilities, and 30%–40% power reduction in comparison to standard 6T techniques. This study involved a 90-nm read assist-based sense Amp design, and a 65-nm domino read-based design with dynamic supply capabilities. The 8T-CDC cell enables significant power savings in terms of reduction for read-assist design, and half-select column power reduction in dynamic dual supply domino read designs with the aid of new header designs. New simplified local evaluation logic and shorter bitlines are employed for the domino read-based design. Simulations showed high performance for the proposed design using shorter bitlines, and dynamic header circuit. Measured hardware data from fabricated chips in 90- and 65-nm PD/SOI technology shows improved stability and yield, and voltage scalability due to the elimination of half-select disturb with comparable access times as that of 6T-based designs.

## VIII. Acknowledgment

We sincerely thank Mr. C. Chandrasekhar, HOD ECE, SVCET, Mr. Lokesh Krishna, Associate Professor, SVCET, Mr. L.Rama Murthy HOD ECE, Vemu IT, Chittoor, and the Staff members of ECE Dept, SVCET, family members, and friends, one and all who helped us to make this paper successful.

## References

[1] R. Joshi, S. Mukhopadhyay, D. W. Plass, Y. H. Chan, C.-T. Chan, and A. Devgan, "Variability analysis for sub-100 nm PD/SOI CMOS SRAM cell," in *Proc. 30th Eur. Solid-State Circuits Conf.*, Sep. 2004, pp. 211–214.

[2] L. Itoh, K. Osada, and T. Kawahara, "Reviews and future prospects of low voltage embedded RAMs," in *Proc. IEEE*

*Custom Integr. Circuits Conf.*, 2004, pp. 339–344.

[3] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, and M. Bohr, "3-GHz 70 MB SRAM in 65 nm CMOS technology with integrated column-based dynamic power supply," in *ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 474–475.

[4] M. Kellah, Y. Yibin, S. K. Nam, D. Somasekhar, G. Pandya, A. Farhang, K. Zhang, C. Webb, and V. De, "Wordline & bitline pulsing schemes for improving SRAM cell stability in low-Vcc 65 nm CMOS designs," in *Proc. VLSI Circuits Symp.*, 2006, pp. 9–10.

[5] V. Ramadurai, R. Joshi, and R. Kanj, "A disturb decoupled column select 8T SRAM cell," in *Proc. CICC*, 2007, pp. 25–28.

[6] W. Henkels, W. Hwang, R. Joshi, and A. Williams, "Provably correct storage arrays," U.S. Patent 6 279 144, Aug. 21, 2001.

[7] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *Proc. IEEE Symp. VLSI Technol.*, 2005, pp. 128–129.

[8] R. Joshi, "Random access memory with stability enhancement and early ready elimination," U.S. Patent Appl. A1/20060250860, Nov. 9, 2006.

[9] R. Joshi, Y. Chan, D. Plass, T. Charest, R. Freese, R. Sautter,W. Huott, U. Srinivasan, D. Rodko, P. Patel, P. Shephard, and T.Werner, "A low power and high performance SOI SRAM circuit design with improved cell stability," in *Proc. SOI Conf.*, Oct. 2006, pp. 4–7.

[10] H. Pilo, J. Barwin, G. Braceras, C. Browning, S. Burns, J. Gabric, S. Lamphier, M. Miller, A. Roberts, and F. Towler, "An SRAM design in 65 nm and 45 nm technology nodes featuring read and write-assist circuits to expand operating voltage," in *Proc. Symp. VLSI Circuits*, Jun. 2006, pp. 15–16.

[11] C. Wann, R. Wong, D. J. Frank, R. Mann, S.-B. Ko, P. Croce, D. Lea, D. Hoyniak, Y.-M. Lee, J. Toomey, M. Weybright, and J. Sudijono, "SRAM cell design for stability methodology," in *Proc. IEEE VLSI-TSA Int. Symp. VLSI Technol.*, 2005, pp. 21–22.

[12] R. Kanj, R. Joshi, and S. Nassif, "Mixture importance sampling and its application to the analysis of SRAM designs in the presence of rare failure events," in *Proc. Des. Autom. Conf.*, Jul. 2006, pp. 69–72.

## ABOUT AUTHORS

1. Mr.K.R.Surendra received Diploma degree from Dr. Y.C.James Yen Rural Polytechnic College, Kuppam, Chittoor Dist, A.P, India and the B.Tech degree from SVPCET, Puttur, Chittoor Dist, A.P, and India. He worked as Asst. Professor in Vemu Institute of Technology during 2010-11. His interested areas are Communications, VLSI and Electronics.

2. Mr.K.Venkataramana Reddy received B.Tech Degree from MITS, Madanapalli, Chittoor, A.P, India and M.Tech from R.V.C.E, Bangalore, and Karnataka, India. His interested areas are digital electronics and VLSI. He has co-authored for several Conference Papers. He thought several subjects for under graduate and post graduate students.