Novel Delay Efficient Approach for Vedic Multiplier with Generic Adder Module

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ABSTRACT

This paper discusses about the implementation of Vedic multiplier in digital hardware. As the multiplier block has adder as the basic component, various generic adder architecture are considered for the implementation the combinational delay for various adder architecture is found. In this paper a 4×4, 8×8, and 16×16, bit multiplier circuit is designed with hierarchical structuring, it has been optimized using Vedic Multiplication "Urdhva Triyagbhyam" Sutra (Algorithm).Algorithm is implemented with Spartan xc2s200-5-pq208 device, Virtex2 Xc2V250FG256-5 device, Virtex5 Xc5VLX220-2ff1760 device, FPGA (Field Programmable Gate Array). The proposed multiplier implementation with Kogge-Stone Adder as a basic component yields a significant reduction in Combinational path delay.

Keywords - **Carry look ahead adder (CLA), Kogge-Stone adder (KSA), Ripple Carry Adder (RCA), Vedic Multiplier**

I. INTRODUCTION

Vedic mathematics is a system of reasoning and mathematical working based on ancient Indian teachings called Veda. It is fast, efficient and easy to learn and use. Vedic mathematics, which simplifies arithmetic and algebraic operations, has increasingly found acceptance the world over. VedicMaths provides answer in one line where as conventional method requires several steps. It is an ancient technique, which simplifies multiplication. The subject was revived largely due to the efforts of Jagadguru Swami Bharathikrishna Tirthaji of Govardhan Peeth, Puri Jaganath (1884-1960). The basis of Vedic mathematics, are the 16 sutras. Urdhva-tiryagbhyam is general formula applicable to all [1].Multiplication is one of the most basic and frequently used operations in a CPU. These operations also form the basis for other complex operations. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. In this paper 4 bit, 8 bit and 16 bit multipliers are implemented using Urdhva-tiryagbhyam sutra and Simulated and synthesized with various generic adder architecture design the adders are the basic components of the Vedic multiplier, the combinational path delay for various adder and various device used for hardware designed is evaluated.

II. GENERIC ADDERS

Adders are the main blocks to complete a multiplier design. The Ripple Carry Adder (RCA) has the smallest area when compared to the other adders. So it is limited to applications where the area must be minimized, while the speed is not important. The ripple carry adder is one of the simplest adders. The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage.A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes. For an n-bit parallel adder, it requires n computational elements (FA). Fig. 1. shows an example of a parallel adder . A 4-bit ripple-carry adder. It is composed of four full adders. The augend's bits of x are added to the addend bits of y respectfully of their binary position. Each bit addition creates a sum and a carry out. The carry out is then transmitted to the carry in of the next higher-order bit. The final result creates a sum of four bits plus a carry out (c4).

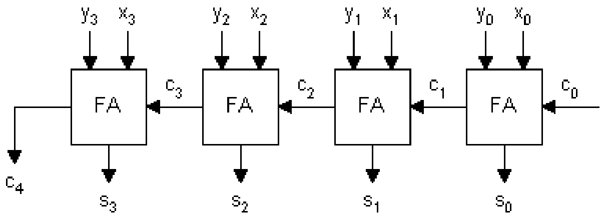

Fig. 1. 4-bit Ripple-Carry Adder Block Diagram

The HDL code for the generic ripple carry adder is given
vsum(i) := (a(i) xor b(i)) xor carry;
carry: = (a(i) and b(i)) or (carry and (a(i) or b(i)));
one of the limiting factors of the ripple carry adder is the time it takes to propagate the carry.
For fast adders, usually the Carry look ahead Adder (CLA) circuit is used. As we know that the ripple-carry adders, one of the limiting factor is the time it takes to propagate the carry. The carry look-ahead

adder solves this problem by calculating the carry signals in advance, based on the input signals. The result is a reduced carry propagation time.

To be able to understand how the carry look-ahead adder works, we have to manipulate the boolean expression dealing with the full adder. Introducing two new signals (propagate P and generate G) in a full-adder, one gets:

$Pi = Ai \oplus Bi$ Carry propagate

$Gi = AiBi$ Carry generate

Both propagate and generate signals only depend on the input bits.The new expressions for the output sum and the carryout are given by:

$Si = Pi \oplus Ci$

$Ci+1= Gi + PiCi$

These equations show that a carry signal will be generated in two cases:

1) if both bits Ai and Bi are 1

2) if either Ai or Bi is 1 and the carry-in Ci is 1.

These equations can be generated for a 4-bit adder:

C1=G0+P0C0

C2=G1+P1C1
=G1+P1(G0+P0C0)=G1+P1G0+P1P0C0

C3=G2+P2C2 = G2 + P2G1 + P2P1G0 + P2P1P0C0

C4=G3+P3C3=G3+P3G2+P3P2G1+P3P2P1G0+P3P2P1
P0C0

These expressions show that C2, C3 and C4 do not depend on its previous carry-in. Therefore C4 does not need to wait for C3 to propagate. As soon as C0 is computed, C4 can reach steady state. The same is also true for C2 and C3

The general expression is

Ci+1=Gi + PiGi-1 + PiPi-1Gi-2 + ……. PiPi-1…. P2P1G0 + PiPi-1 ….P1P0C0.

Carry look-ahead adder's structure can be divided into three parts: the propagate/generate generator.

The Kogge-Stone adder (KSA) is the fastest adder classified as a parallel prefix adder since the generate and the propagate signals are precomputed. These adders are known to be quite fast in exchange for heavier parallel architecture. The Kogge-Stone adder uses a tree structure to compute the overall carry chain.

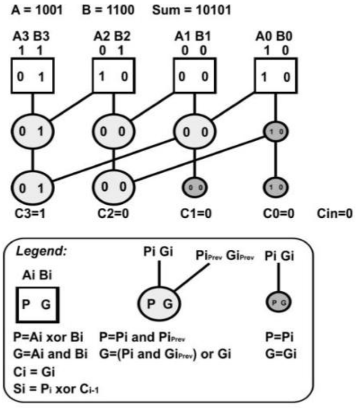

Fig.2.Schematic of 4 bit Kogge Stone Adder

III. Implementation Of Vedic Multiplier

The 4x4 Multiplier is made by using 4, 2x2 multiplier sub blocks. Here, the multiplicands are having the bit size of (n=4) whereas, the result is of 8 bit in size. The input is broken in to smaller groups of size of n/2 = 2, for both inputs, that is a and b. These newly formed groups of 2 bits are given as input to 2×2 multiplier block and the result produced 4 bits, which are the output produced from 2×2 multiplier block are sent for addition to an addition tree.

As the generic adder is designed the designing of high bit multipliers in not an issue using the structural modeling it becomes easy for just call the predefined components and design the multiplier.

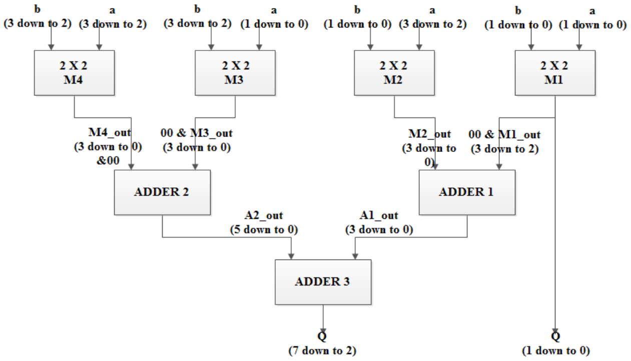

Fig.3. Hardware realization of 4×4 multiplier

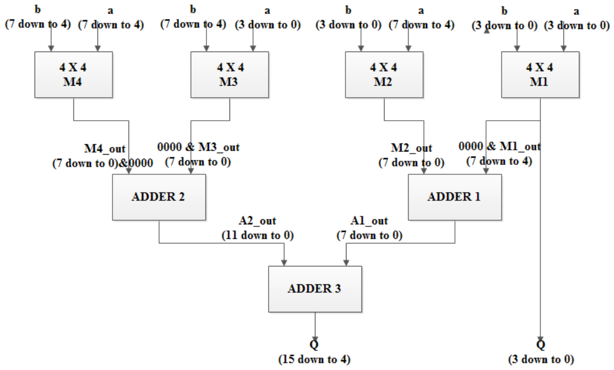

Fig.4. Hardware realization of 8×8 multiplier

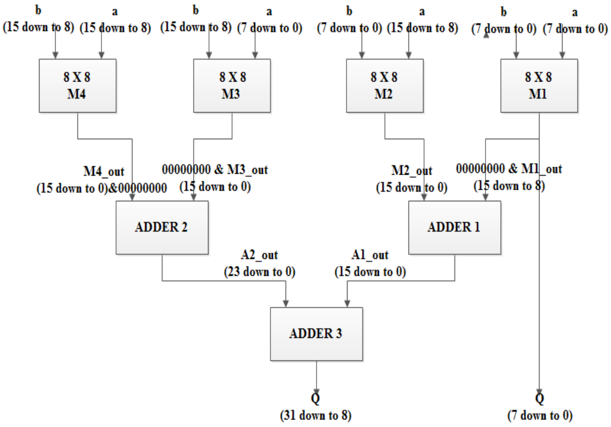

Fig.5. Hardware realization of 16×16 multiplier

In this experimentation adder such as Ripple Carry Adder ,Carry look ahead adder and Kogge-Stone adder are taken for various size of input bits the adders those are designed are generic adders the table below shows the experimentation results.

TABLE I
COMPARISON OF COMBINATIONAL DELAY WITH DIFFERENT ADDER ARCHITECTURE

Device Name	Multiplier	Adder Type and Combinational delay in ns		
		RCA	CLA	KS
Spartan II Xc2S200pq 208-5	4 bit	23.439	24.508	10.334
	8 bit	42.479	42.820	40.176
	16 bit	80.688	78.665	69.648
Virtex2 Xc2V250F G256-5	4 bit	12.964	14.553	13.281
	8 bit	24.442	24.677	22.090
	16 bit	45.227	41.447	37.184
Virtex5 Xc5VLX22 0-2ff1760	4 bit	06.712	06.828	07.718
	8 bit	12.214	10.864	05.640
	16 bit	19.201	20.478	18.995

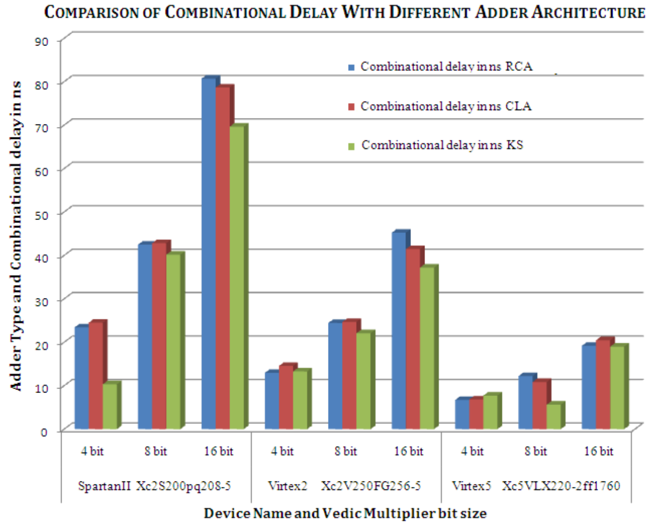

Fig.6. Graph of delay comparisons

IV. CONCLUSION

This paper presents a method of multiplication "Urdhva Tiryakbhyam" Sutra based on Vedic Mathematics. We apply the same idea to the binary number system to make the proposed algorithm compatible with the digital hardware. The design of the proposed 4×4, 8×8, 16×16 bit Vedic multiplier is implemented on Spartan xc2s200-5-pq208 device, Virtex2 Xc2V250FG256-5 device, Virtex5Xc5VLX220-2ff1760 device.The combinatational path delay of the various Vedic multipliers is found with various adder architecture it is concluded that the Kogge-stone adder when used as the component while multiplication the combinatational paths delay reduces. In this work, some steps have been taken towards implementation of fast and efficient Arithmetic Logic Unit or a Math Co-processor, using Vedic Mathematics.

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