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Design and FPGA Prototyping of Embedded Ethernet Controller

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ABSTRACT

Presently, the embedded system, which was composed of SOC, entered into people's life more and more widely. We can see it frequently whether in the mobile phones, television, industrial control equipment or network devices. With the continuous expansion of network scale and the increase of service, the embedded Internet has played an increasingly important role. Ethernet is the most widely used LAN technology in the present day world. With the increasing use of embedded systems, the need for incorporating Ethernet connectivity into the embedded systems is greatly felt. Therefore, the study of Ethernet communication on embedded system is necessary. The embedded Ethernet is widely applied, and its research is very important.

In this paper a 10/100 Mbps embedded ethernet controller has been developed in Verilog-HDL, that can support two speeds (10/100Mbps), two modes (full/half duplex), and can communicate with PHY through MII. The Ethernet controller designed conforms to the standards of IEEE 802.3 communication protocol. The simulation has been done using ModelSim6.4SE. FPGA Prototyping was done using Xilinx EDK tool on Xilinx Virtex-5FX70T FPGA. The packet capture has been done using Wireshark tool.

Keywords-**LAN, Ethernet, OSI reference model, MII, CSMA/CD, EMAC, and Ethernet PHY.**

I. INTRODUCTION

In today's business world, reliable and efficient access to information has become an important asset in the quest to achieve a competitive advantage. File cabinets and mountains of papers have given way to computers that store and manage information electronically. Computer networking technologies are the glue that binds these elements together. Networking allows one computer to send information to and receive information from another. We can classify network technologies as belonging to one of two basic groups. Local area network (LAN) technologies connect many devices that are relatively close to each other, usually in the same building. In comparison to WANs, LANs are faster and more reliable, but improvements in technology continue to blur the line of demarcation. Fiber optic cables have allowed LAN technologies to connect devices tens of kilometres apart.

Ethernet is a family of frame-based computer networking technologies for Local Area Network (LAN). The name came from the physical concept of the ether. It defines a number of wiring and signalling standards for the Physical Layer of the OSI networking model as well as a common addressing format and Media Access Control at the Data Link Layer. The combination of the twisted pair versions of Ethernet for connecting end systems to the network, along with the fiber optic version is the most widespread wired LAN technology. Ethernet has been used from around 1980 to the present, largely replacing competing LAN standards such as token ring, FDDI, and ARCNET[1]. Ethernet has been a relatively inexpensive, reasonably fast, and very popular LAN technology for several decades. Ethernet uses the CSMA/CD access method to handle simultaneous demands. The most commonly installed Ethernet systems are called 10BASE-T and provide transmission speeds up to 10 Mbps. Devices are connected to the cable and compete for access using a Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. Gigabit Ethernet provides an even higher level of backbone support at 1000 megabits per second (1 gigabit or 1 billion bits per second). 10-Gigabit Ethernet provides up to 10 billion bits per second. The main aim of the paper is to study the process of developing verilog code for Ethernet IP core. This IP core is prototyped using Xilinx Virtex5FX70T FPGA. The prototyping is done by using the Xilinx tool called embedded development kit (Xilinx EDK).It is a suite of tools that enables us to design a complete embedded processor system for implementation in a Xilinx Field Programmable Gate Array (FPGA) device. The packet is captured using a network packet analyzer called Wireshark.

II.BACKGROUND

2.1.INTRODUCTION TO NETWORK INTERFACE MODELS AND ETHERNET FRAME FORMAT

Interconnection of two or more networks forms an internetwork. The communication between devices present in an internetwork presents certain

challenges. For example, devices manufactured by different manufactures need to follow certain consistent standards to be able to communicate properly. This led to the development of certain reference models. The network models set a standard as to how information is to be sent over a network. The reference models divide the functions of a network into layers. Layers are arranged to be as independent as possible, with a minimum set of information passing between layers. Each layer (n-1) provides a certain set of services to the layer above it (n), shielding the actual implementation details from the above layers. The two most popular reference models are OSI reference model and TCP/IP reference model. The OSI reference model provides standardization for the protocols to be used in different layers. OSI (Open Systems Interconnection) model is called so because it is concerned with the interconnection of systems which are open for communication with other systems. The OSI reference model has seven layers.

Ethernet is concerned with physical and data link layers of OSI model. The physical layer is responsible for converting the data from the form in which it is represented in the data link layer (frame) to the form in which it is transmitted over the physical medium (raw bits)[5]. It provides the hardware required to send and receive data over the physical medium. This hardware includes signal encoders, line drivers, clock synchronizers, etc.,.This layer also defines the electrical, mechanical and timing specifications for these devices that enable transfer of data over the communication channel. These include line impedances, pin voltages, cabling specifications like cabling type, cabling distance, etc. The data link layer is responsible for transfer of data between stations within a network. The main task of the data link layer is to convert the incoming data into frames. The other functions include error control, addressing, control of access to the shared medium and flow control. Each frame contains destination and source addresses which allow identification of the sending and the receiving stations on the network[7].

The data link layer is divided into two sub-layers namely the Media Access Control sub-layer and the Logical Link Control layer. The Logical Link Control sub-layer acts as interface between physical layer and the higher layer protocols. The data link layer is divided into media access control (MAC), logical link control (LLC) and the optional

MAC control sub layer, as shown in Figure 1(a). The optional MAC control sub layer provided a structure with full-duplex flow control[8]. The MAC sub layer adapts LLC sub layer to different media access technologies and physical media. And its main functions are assembling or disassembling data and the managing of media attaching. The former includes the combining of the frame before sending and the error detection during receiving or after having received. The latter includes the media distribution (i.e. collision avoidance) and competition processing (i.e. conflict processing)[3].

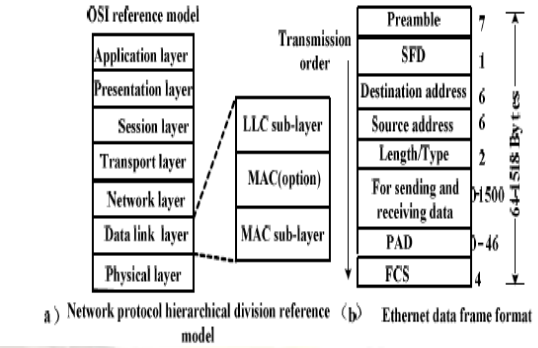


Figure1: OSI reference model and ethernet frame format.

The Ethernet data frame format is shown in Figure 1(b).The preamble is used for synchronization while sending and receiving data, which includes seven bytes of 10101010.The start frame delimiter (SFD, 10101011) indicates the beginning of a frame. The least significant bit (LSB) of the destination address in destination/source address is used to determine unicast (‘0’) or multicast (‘1’). The length/type specifies the length or transmission type of data to be transmitted and received. These data is provided by the upper layer protocol. The PAD is used to ensure that the length of frame is at least 64 bytes. By calculating the CRC [4] of destination/source address, length/type, the data to be transmitted and received and the filling bits, we can get the value of the frame check sequence (FCS)[2].

2.2ETHERNETMEDIA ACCESS CONTROLLER

Ethernet protocol is concerned with bottom two layers of the OSI reference model. They are the Data link layer and the physical layer. The Data Link Layer is divided into two sub-layers. They are:

1. Logical Link Control layer and
2. Media Access Control sub-layer.

The main functions of the logical link control layer are flow control and multiplexing the protocols transmitted over the Media access control sub-layer while transmitting and decoding them while receiving[3]. Ethernet Media access controller implements the functions of the Media access control sub layer. The functions of the physical and data link layers have been illustrated in Figure2.

The functions of an Ethernet MAC (Media access control) can be summarised as follows:

a) Channel access control
b) Framing
c) Error detection
d) Addressing

e) IFG implementation

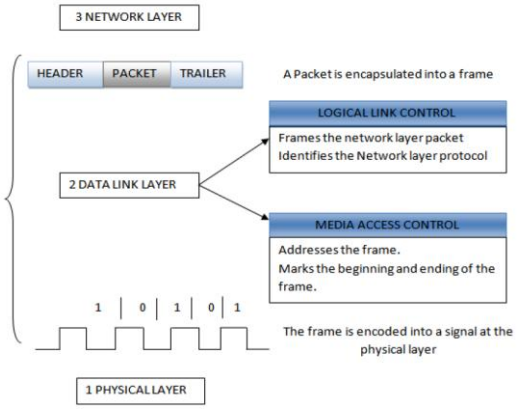


Figure 2: Functions of data link layer

2.3 CARRIER SENSE MULTIPLE ACCESS/COLLISION DETECTION PROTOCOL

CSMA/CD (Carrier Sense Multiple Access with Collision Detection) protocol. In this paper, CSMA/CD protocol has been used to implement Half-Duplex transmission. This protocol provides an effective way for multiple nodes to access a shared medium. According to this protocol, every node on the network has equal access to the channel[5]. A node (station) which wants to transmit a frame has to first sense the channel to check if another node is transmitting (carrier sense). If the channel is idle, then the node will broadcast after waiting for an interframe gap of 96 bit times. A collision may still occur due to the channel propagation delay (i.e., two nodes may not hear each other's transmission). In this case, the node has to detect if is message was destroyed (collision detection). The node then sends a jam signal for 512 bit times to intimate to the stations on the network that a collision has occurred. The station then waits for a random amount of time called the back off period before attempting to transmit again. The CSMA/CD protocol follows a binary exponential back off strategy. This means that if a collision has occurred n times, (i.e., if n attempts have been made by a node to transmit) then, the node chooses a random number k from the set {0, 1, 2… (2n-1)}. The node waits for a time equal to the product k*512 bit times before it attempts to transmit again. The bit time is 0.1 µsec for 10Mbps Ethernet and 0.01 µsec for 100Mbps Ethernet. The maximum value of k is 1024. If the node does not sense any collision throughout the duration of its frame propagation, then the node is done with its frame transmission[6].

2.4 MEDIA INDEPENDENT INTERFACE (MII)

Media Independent Interface (MII) is a standard interface used to connect a Ethernet(10/100Mb/s) MAC to a PHY chip. Media independent means that different types of PHY devices can be connected to different media (i.e. twisted pair, copper, fiber optic.) without replacing or redesigning the MAC hardware. Any MAC may be used with any PHY, independent of the transmission media since the MII bus which is standardized as IEEE 802.3u connects different types of PHYs to Media Access Controllers.MII bus transfers data using 4-bit words(i.e..nibble (i.e. 4 transmit data bits ,4 receive data bits) in each direction[9].

2.5 ETHERNET PHY

PHY is the physical interface transceiver which is often called as Phyceiver operates at physical layer of the OSI network model. The IEEE 802.3 standard defines the Ethernet PHY. It complies with IEEE 802.3 specifications for both 10BaseT and 100BaseTX. PHY connects a link layer device which is often called as a Media Access Control or MAC address to the physical medium. PHY chip provides physical and analog signal access to the link, which is commonly found on Ethernet devices[10]. A PHY device includes Physical Coding Sub layer (PCS), Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) layer. The data that is being transmitted and received is encoded and decoded by Physical Coding Sub layer. The main functionality of PHY is to handle how the data is actually moved to/from the wire. The PHY provides either 10 or 100-Mbps operation and can be a set of integrated circuits (or a daughter board) on an Ethernet port, or an external device supplied with a Medium Independent Interface (MII) cable that plugs into an MII port on a100BaseT device (similar to a 10-Mbps Ethernet transceiver). It contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 3 and 5 unshielded twisted pair.

III.ARCHITECTURE OF 10/100 EMBEDDEDETHERNET CONTROLLER

The controller is mainly composed of transmit module, receive module, dual port RAM,CRC generator and checker module, fifo, transmit and receive control logic.

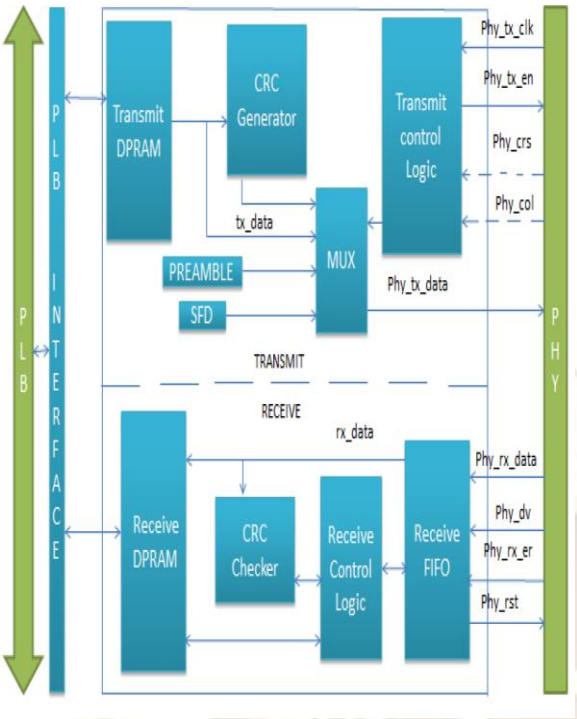


Figure3:Architecture of Ethernet controller

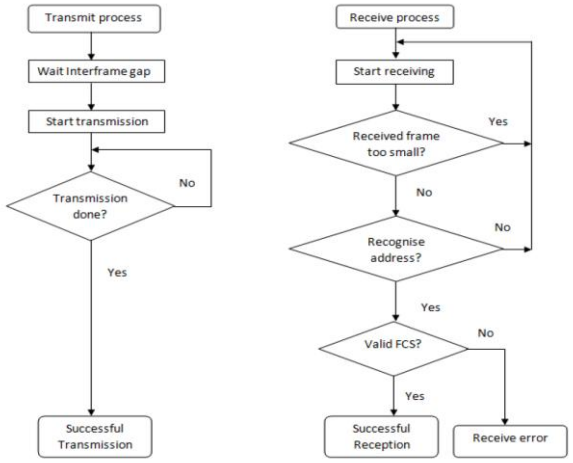
(Solid line: Architecture of full duplex ethernet controller Solid+dotted line: Architecture of half duplex ethernet controller)

1.TRANSMIT

The Ethernet transmitter receives a 32-bit input data from the processor through PLB interface. This 32-bit data is given as input to dual port RAM which is asynchronous since the write and read operations are controlled by different clocks. Fast ethernet supports nibble wise transmission. The 4-bit output is given to crc generator module which performs crc computation using 32-bit crc polynomial. Then crc output, 4-bit output from dpram , prm and sfd all are routed to mux. The multiplexer routes the incoming data to the output of the Ethernet transmitter based on the select input received from the Transmit control state machine.

2.RECEIVE

As long as the Phy_dv is high ,the data is received and crc is computed. If the checksum value of both matches, then the packet passes else the packet gets discarded.



(a) (b)

Figure4:(a)Full duplex transmit flow(b)full duplex receiving flow

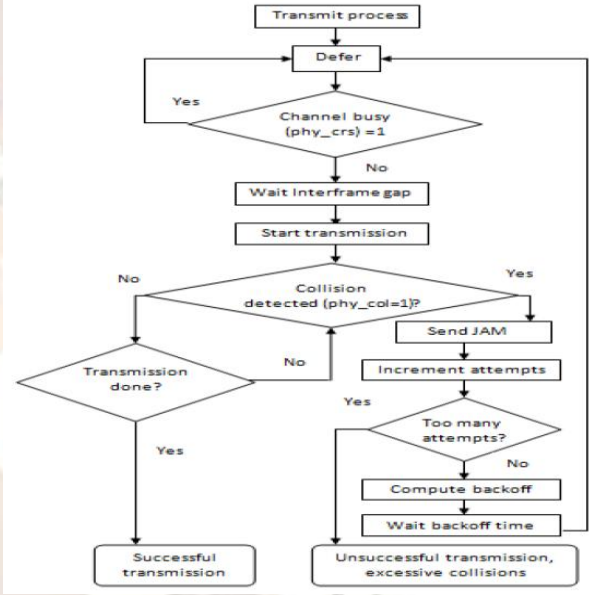


Figure 5: half duplex transmit flow

IV. SIMULATION RESULTS

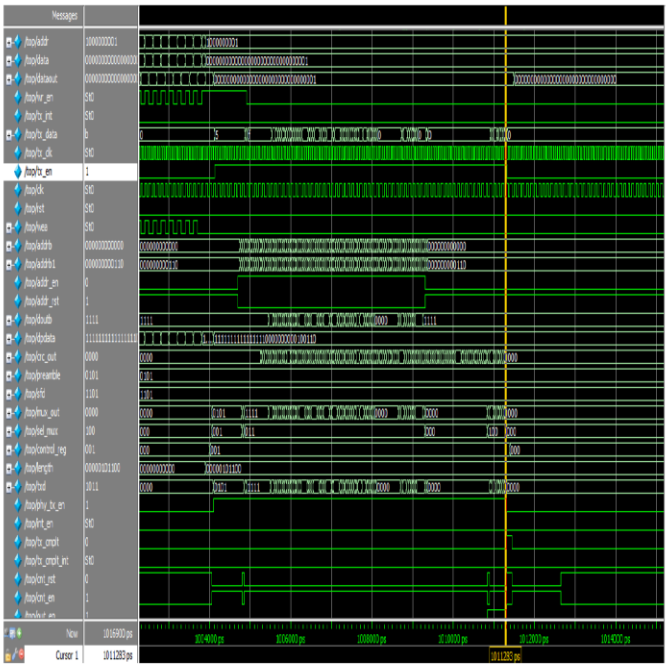


Figure 6:full duplex waveform

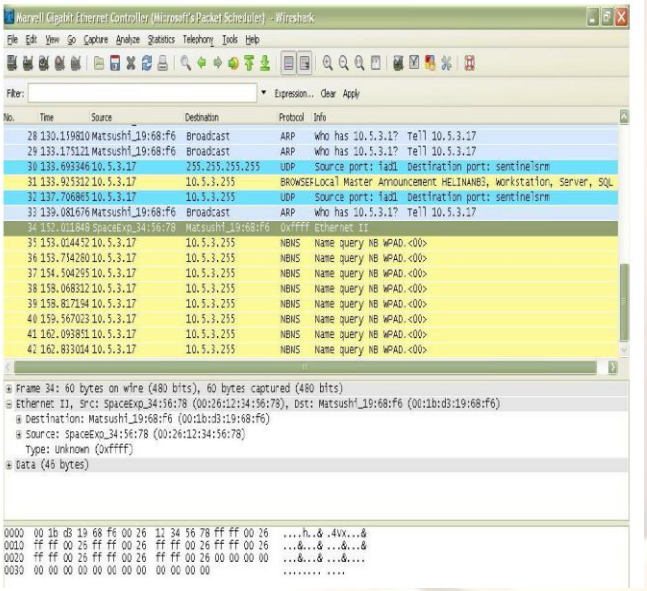


Figure 7:Transmitted packet captured in wireshark

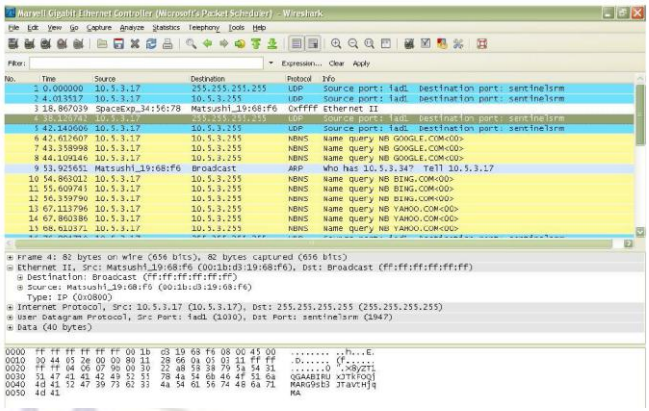


Figure8:Received packet captured in Wireshark

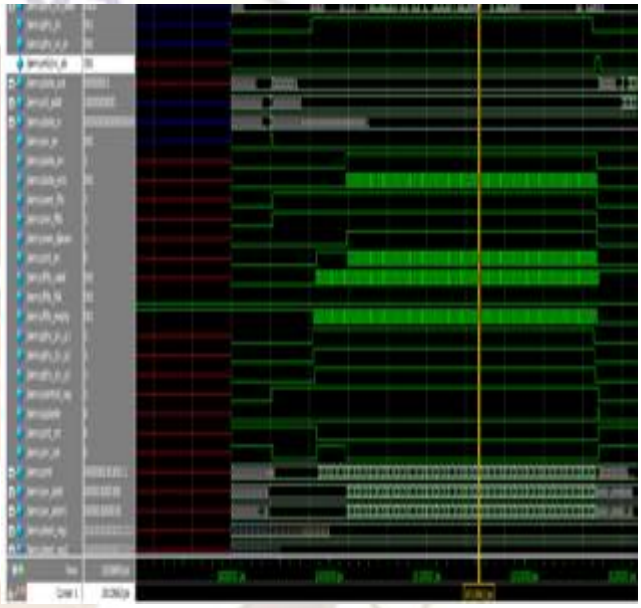


Figure 9:half duplex waveform

V. CONCLUSION

This paper simply focuses on the application or simulation of Ethernet MAC IP (Intelligence Property) and it provides a design method of 10/100 Mbps Ethernet controller based on embedded. Through software simulation and hardware verification, the design of the Ethernet controller is effective and it can be applied in the embedded network systems. Since the embedded Gigabits Ethernet has been not widely applied at present, studying the Gigabits Ethernet controller should be the next step.

VI. FUTURE WORK

Traditionally TCP/IP is implemented in software and executed on a processor. With the advent of higher bandwidth networks this has become a major bottleneck in data transfer as the processor must spend more of its time handling incoming frames rather than running user algorithms. This

performance degradation negatively impacts network efficiency and is inconsistent with real time applications. To solve this more functions are now being offloaded in to dedicated networks. So we can offload checksum calculation to hardware so as to decrease the processor clock cycles and increase the performance. Also, 1Gbps and 10Gbps Ethernet Media Access Controller can be implemented.

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