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Implementation of Carrier Synthesis Technique Using DPLL

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Abstract

DPLLs are used widely in communications systems like radio, telecommunications, computer and other electronic applications. Digital PLLs are a type of PLL used to synchronize digital signals. While DPLLs input and outputs are typically all digital, they do have internal functions which are dependent on analog signals. The main blocks in demodulator are DDS core, Filters, Arc tan estimator, Loop filter. The area reduction for on-chip applications can be achieved through optimization of the number of micro rotations in proposed design. For better loop performance of second order complex DPLL and to minimize quantization error, the numbers of iterations are also optimized. Modelsim Xilinx Edition (MXE) and Xilinx ISE will be used simulation and synthesis respectively. The Xilinx Chipscope tool will be used to test the FPGA inside results while the logic running on FPGA. The Xilinx Spartan 3 Family FPGA development board will be used this project.

Keywords—*Digital Signal Processing, DPLL, Micro-rotation, Loop performance, Arctan estimator.*

I. INTRODUCTION

The progress in increasing the performance, speed, reliability and the simultaneous reduction in size and cost of integrated circuits has resulted in strong interest being shown in the implementation of control and communication systems in the digital domain. Aside from the general advantages associated with digital systems, a digital version of the phase-locked loop solves some of the problems associated with its analogue counterpart; namely sensitivity to DC drifts and component saturations, difficulties encountered in building higher order loops and the need for initial calibration and periodic adjustments. In addition, with the ability to perform elaborate real-time processing on the signal samples, the DPLLs can be made more flexible and versatile, especially by the use of microprocessors.

The earliest efforts on DPLLs concentrated on partially replacing the analogue PLL (APLL) components with digital ones. The first all DPLL was reported by Drogin in 1967.Since then, different authors have suggested many kinds of all digital phase-locked loops and have discussed various aspects of implementing them. All DPLLs are categorized into two classes as follows:

1. Uniform sampling DPLL, in which the input signal is sampled at a fixed rate (Nyquist rate).
2. Non-uniform sampling DPLL in which the sampling rate is variable.

DPLL is suitable for coherent (all digital) communications. This DPLL contains a purely digital phase detector, loop filter and voltage-controlled oscillator, providing an extremely wide tracking frequency range and a completely linear behavior.

DPLL is very popular in synthesizer applications. Frequency synthesis is currently a very important PLL application area.

In this project, we will recover the carrier signal. This carrier signal is high speed recovery signal and we achieve area optimization, reprogrammable and low power features.

The remaining paper is organized as follows: Section-II deals with the background of the DPLLs, section-III describes the proposed design and section-IV gives the simulation results and the analysis of the proposed design.

II. BACKGROUND

PLL Stands for phase-locked loop and is basically a closed loop frequency control system, which functions based on the phase sensitive detection of phase difference between the input and output signals of the controlled oscillator. The PLL method of frequency synthesis is now the most commonly used method of producing high frequency oscillations in modern communications equipment. PLL circuits are now frequently being used to demodulate FM signals, making obsolete the Foster-Seerly and radio detectors of the early years. Other applications for PLL circuits include AM demodulators, FM demodulators, FSK demodulator, and other communication areas.

The PLL technique has surprisingly been around for a long time. In the 1930's the super heterodyne receiver was in its hayday, however attempts were made to simplify the number of tuned stages in the super heterodyne.

In the early 1930's the super heterodyne receiver was king. The super heterodyne eventually extended its domain far beyond commercial broadcast receivers and for microwave radar receivers developed during worldwar2.

In the 1940's the first wide spread use of the phase locked loop was in the synchronization of the horizontal and vertical sweep oscillators in television receivers to the transmitted sync pulses. Such circuits carried the names synchro-lock and synchro-guide. Since that time, the electronic phase locked loop principle has been extended to other applications. For example, radio telemetry data from satellites used narrow band, phase-locked loop receivers to recover low-level signals in the presence of noise other applications now include AM and FM demodulators, FSK decoders.

Normally PLLs are classified into 4 classes.

a. Analog or Linear PLL (APLL)
b. Digital PLL (DPLL)
c. All digital PLL (ADPLL)
d. Software PLL (SPLL)

In this, project we will discuss on DPLL. It consists of all digital PLL blocks. Traditional DPLL block diagram consists of three major functional units.

1. Phase detector
2. Digital loop filter
3. Voltage-controlled oscillator.

III. PROPOSED SYSTEM

Main objective of this project is high speed carrier recovery using DPLL. We designs second order complex DPLL which functions as a FM demodulator.

The proposed design consists of the reprogrammable, area optimized and low power features. The modulator and demodulator contain a compressed direct digital synthesizer (DDS) for generating the carrier frequency with spurious free dynamic range. The demodulator has been implemented based on the digital phase locked loop (DPLL) technique and it is shown on fig.1. Here we had given the modulated signal to this block. The proposed FM modem has been implemented and tested using Spartan 3e board as a target device.

FM Demodulator:

The main blocks of demodulator are

1. DDS
2. Filters
3. Arc tan estimator
4. Loop filter

DDS: DDS is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as a part of a digital phase-locked loop.

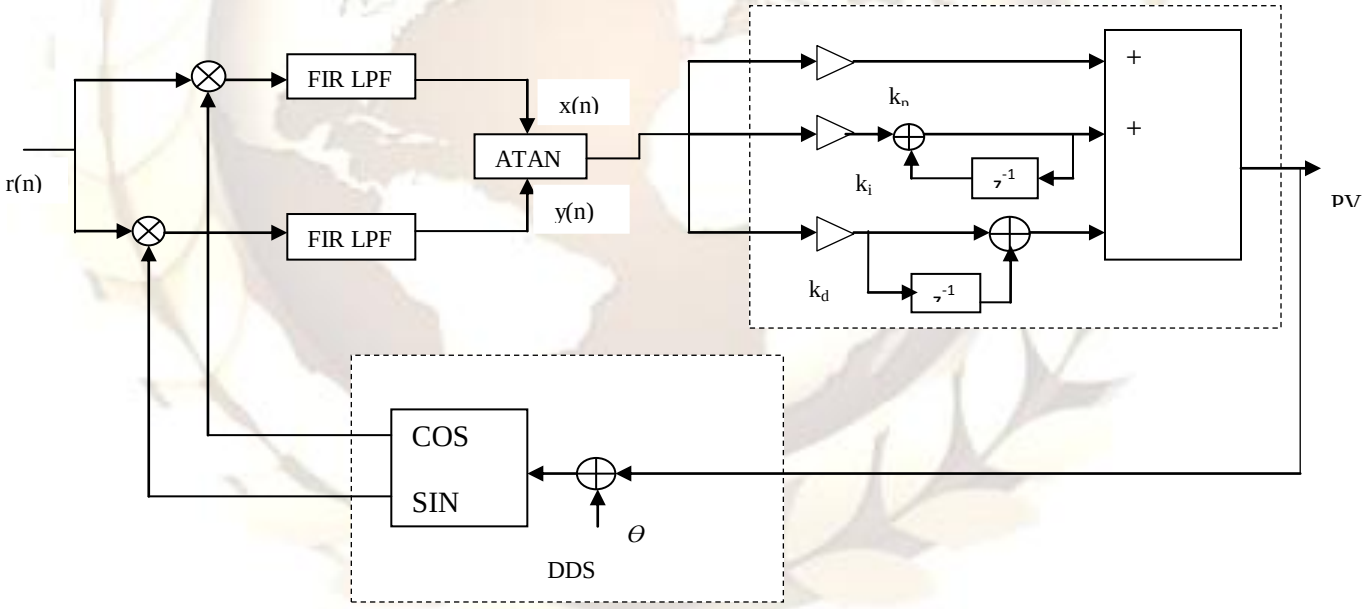

Fig1: Demodulation block diagram using DPLL

A basic direct digital synthesizer consists of a frequency reference, a numerically controlled oscillator and a digital-to-analog converter. A DDS has many advantages over its analog counterpart, the phase-locked loop including much better frequency agility, improved phase noise, and precise control of the output phase across frequency switching transitions.

Filter: The carrier waves (cosine and sine) that are generated by DDS core is given as input to the filter. The direct form of FIR filter is standard linear convolution, which described the output as convolution of input and impulse response of the filter.

$$y[n] = x[n] * c[n]$$
$$= \varepsilon\, x[k]c[n-k]$$
$$= \varepsilon\, c[k]x[n-k]$$

Where c[n] values represent filter coefficients, and x[n] represents the input samples.

Finite impulse response (FIR) filters are the most popular type of filters implemented in software. Filters are signal conditioners. Each functions by accepting an input signal, blocking pre-specified frequency components, and passing the original signal minus those components to the output. FIR filter is a filter structure that can be used to implement almost any sort of frequency response digitally. An FIR filter is usually implemented by using a series of delays, multipliers, and adders to create the filter's output.

Arc tan estimator as Phase detector: The outputs of filters are given to this module. Arctan (y/x) returns in radians. The result is between –pi and pi. The phase detector is a device that compares two input frequencies, generating an output that is a measure of
their phase difference. This module gives the frequency.

Loop filter as PID Controller: A Proportional-integral-derivative controller is a generic control loop feedback mechanism widely used in industrial control systems, a PID is the most commonly used feedback controller. A PID Controller calculates an error value as the difference between a measured process variable and desired set point. The controller attempts to minimize the error by adjusting the process control inputs. The PID controller calculation involves three separate constant parameters, and is accordingly sometimes called three-term control: the proportional, the integral and derivative values, denoted P, I, and D. These values can be interpreted in terms of time: P depends on the present error, I on the accumulation of past errors, and D is a prediction of future errors, based on current rate of change.

If a controller starts from a stable state at zero error (PV=SP), then further changes by the controller will be in response to changes in other measured or unmeasured inputs to the process that impact on the process, and hence on the PV. Variables that impact on the process other than the MV are known as disturbances. Generally controllers are used to reject disturbances and/or implement set point changes.

In theory, a controller can be used to control any process which has a measurable output (PV), a known ideal value for that output (SP) and an input to the process (MV) that will affect the relevant PV. Controllers are used in industry to regulate temperature, pressure, flow rate, chemical composition, speed and practically every other variable for which a measurement exists.

The loop filter/loop controller used is PID Controller. The transfer function of the PID Controller looks like the following:

$$K_P + \frac{K_I}{S} + K_D\, S = \frac{K_D S^2 + K_P S + K_I}{S}$$

Where

- K_P = Proportional gain
- K_I = Integral gain
- K_D = Derivative gain

Tuning a control loop is the adjustment of its control parameters to the optimum values for the desired control response. Stability is a basic requirement, but beyond that, difference systems have different behavior, different applications have different requirements, and requirements may conflict with one another.

If the PID controller parameters are chosen incorrectly, the controlled process input can be unstable, i.e. its output diverges, with or without oscillation, and is limited only by saturation or mechanical breakage. Instability is caused by excess gain, particularly in the presence of significant lag. Generally, stability of response is required and the process must not oscillate for any combination of process conditions and set points, though sometimes marginal stability is acceptable. The response from arctan estimator is given to loop filter. This helps in minimizing the error.

IV. SIMULATION RESULTS AND ANALYSIS

The FM modem process and the architecture is developed. Here modelsim tool is used in order to simulate the design and to check the functionality of the design. Once the functional verification is done, the design is taken to the Xilinx tool for synthesis process and the netlist generation.

This simulation is performed before synthesis process to verify RTL (behavioral) code and to confirm that the design is functioning as intended. Behavioral simulation can be performed on VHDL design. In this process, signals and variables are observed, procedures and functions are traced and break points are set. This is a very fast simulation and so allows the designer to change the HDL code if the required functionality is not met with in a short time period. Since the design is not yet synthesized to gate level, timing and resource usage properties are still unknown.

In this project we recovered high speed carrier signal, minimized the area and also achieved low power features.

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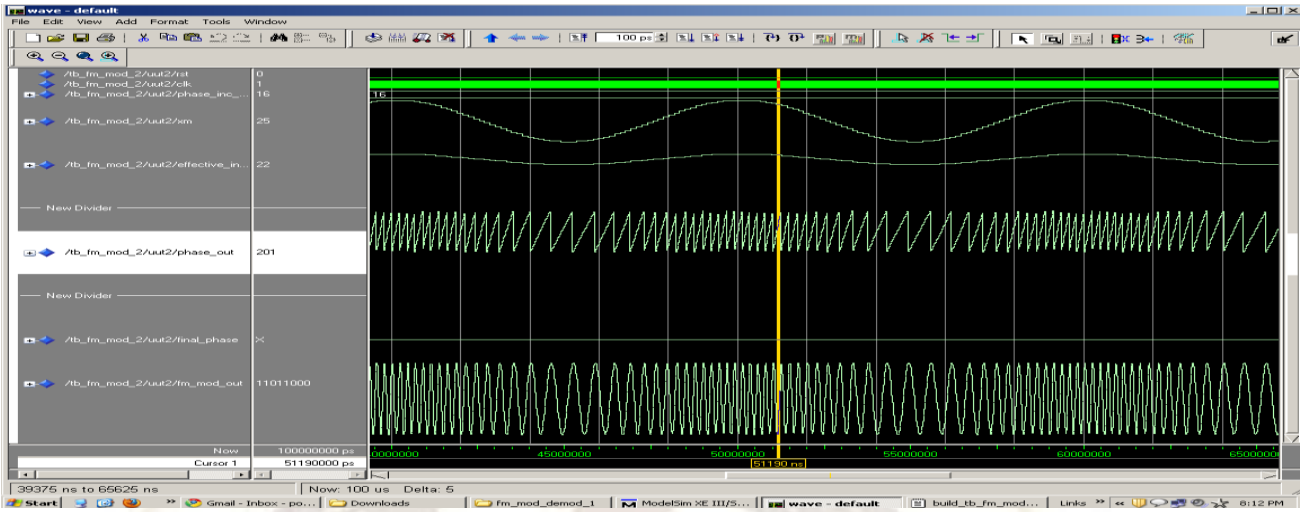

Fig1: Modulated signal

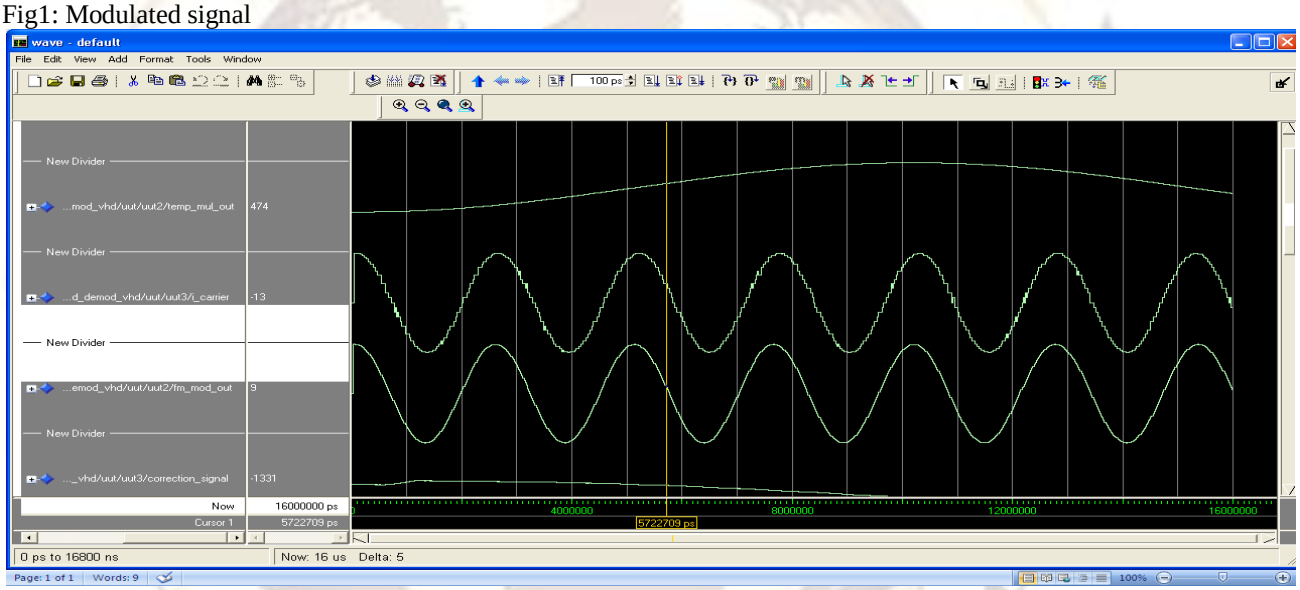

Fig2: Intermediate signals

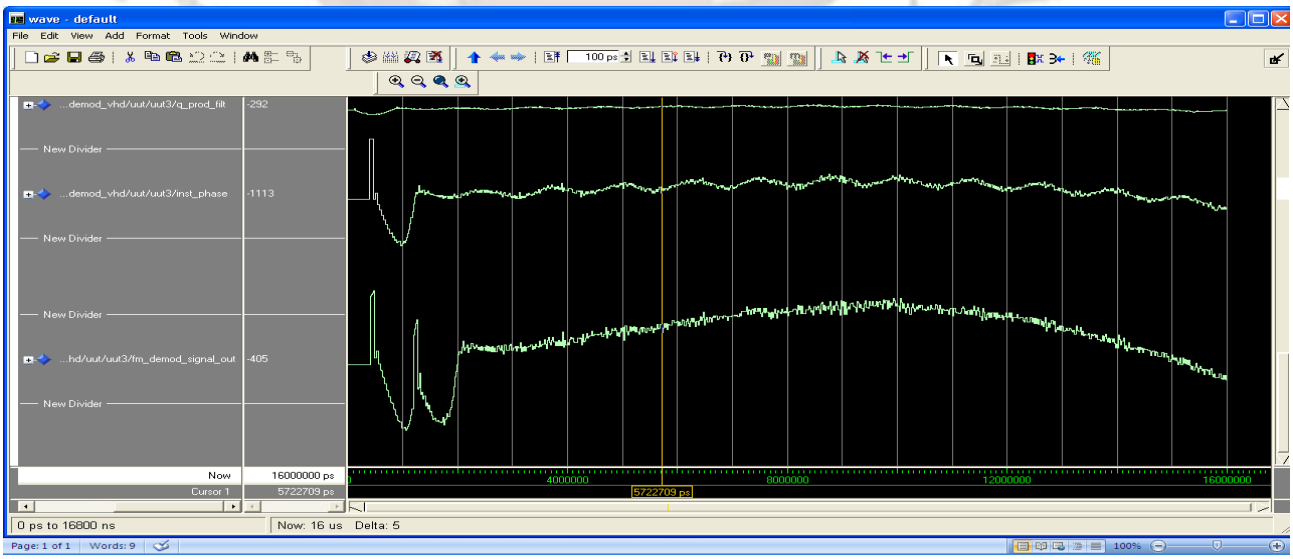

Fig3: Loop filter output