A Proposed Design of Five Transistor CMOS SRAM Cell for High Speed Applications

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Abstract

Static random access memories (SRAMs) is made up of very large scale integrated (VLSI) circuits. A SRAM cell to operate in the deep sub-micron ranges it should meet some stringent requirements . This paper presents a new five transistor (5T) CMOS SRAM cell to accomplish improvements in stability, power dissipation, and performance over previous designs, for high speed and high stability memory operation. This circuit is simulated in a proprietary 180 nm CMOS process, using Cadence Spectre and BSIM3v3 models. Here we are comparing 5T SRAM cell with 6TSRAM cell and thus proving how 5T SRAM cells are more beneficial through various simulations.

Keywords– *CMOS, SRAM, VLSI, Static Noise Margin (SNM).*

I. Introduction

Colossal advances in CMOS technology have made it possible to design chips with high integration density, better performance, and low power consumption. To attain these objectives, the feature size of the CMOS devices has faced aggressive scaling down to very small features and dimensions. However, the leakage current has increased immensely with technology scaling, and has become a major contributor to the total IC power [1]. In addition, as feature size of CMOS devices scales down, the random variations in process parameters have emerged as a major design challenge in circuit design [2]. These random variations of device parameters in nano-scale CMOS technologies include random variations in channel length, channel width, oxide thickness, threshold voltage, etc [2]. These random parameter variations result in significant variation in the characteristic of digital circuits.

Modern microprocessors employ on-chip caches, which can effectively reduces the speed gap between the processor and main memory to boost system performance. These on-chip caches are usually implemented using arrays of SRAM cells. A six transistor (6T) SRAM cell, shown in Fig. 1, is conventionally used as the memory cell. However, the mismatch in the strength between transistors of 6T SRAM cell due to process variations can results in failure during read operation, i.e. flipping of the cell data while reading, especially at lower levels of V_{DD}[3]. Therefore, conventionalSRAM cell shows poor stabilityat verysmallfeature size. In addition, as CMOS technology scales down, an increase in total leakage current of a chip is observed.

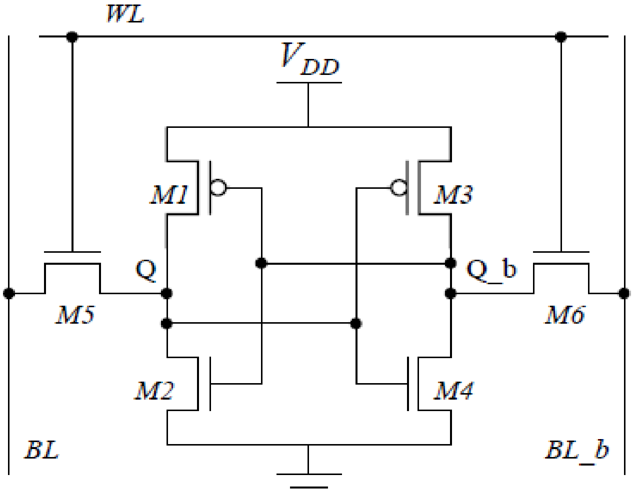

Fig. 1. Conventional 6T SRAM Cell

Moreover, the total leakage current of a chip is proportional to the number of transistors on the chip. Since the SRAM includeslarge number of transistors on a chip, the SRAM leakage has also become a more significant component of total chip leakage in scaled CMOS technology. Hence, stability during read operation and leakage current of SRAM cell are two most prominent parameters in designing of SRAM cell in nano-scale CMOS technologies.

A novel 5T SRAM cell [4] has been previously proposed as an improvement to the standard six transistor (6T) SRAM cell model in various aspects. This 5T SRAM cell, as shown in Fig. 2, comprises two inverters, connected back-to-back and one additional transistor that is used to access the cell for read and write. Here both the bit-lines are precharged to V_{DD} to retain the data during standby mode. However, the speed of a cell, which characterizes the performance of the cell, is still to be improved to reduce the speed gap further between processor and main memory.

In response to these challenges in both conventional 6T and novel 5T SRAM cells, a new 5T SRAM cell has been proposed and its performance issues are discussed. The rest of the paper is organized as follows.Section II discusses basic structure, write, and read operationsof the proposed 5T SRAM cell.Section III explores detailed static noise margin (SNM) analysis of the proposed cell under various modes.Section IV presents the simulation resultsperformed

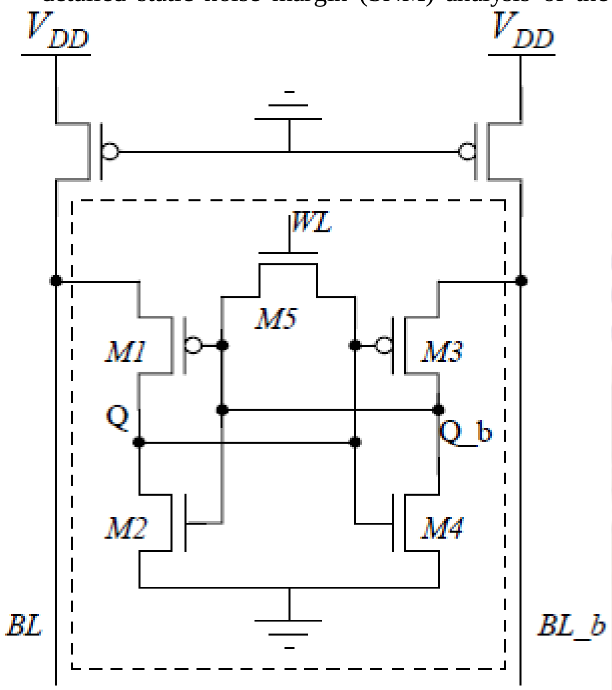

Fig. 2. Novel 5T SRAM Cell

in a proprietary 180 nm CMOS process.On the basis of results analyzed, section V concludes the significance of the proposed cell in various high speed, high stability, and low power applications.

II. PROPOSED 5T SRAM CELL

Fig. 3 shows the proposed five transistor (5T) SRAM cell. In this cell, Inverter NMOS transistors (*M*1, *M*3) are directly connected to the bit lines, PMOS transistors (*M*2, *M*4) are connected to power supply voltage (V_{DD}), and thereis an additional transistor *M*5 coupling the inverters. Unlike standard cell, no word line transistors are needed to provide access during the read and write cycles. In contrast to novel 5T cell, bit lines of the proposed cell are precharged to ground.

A. Standby Mode

Before discussing the operation of proposed SRAM cell, operations of the previously introduced novel 5T cell will be reviewed to clarify the difference between former and later.In the novel 5T cell, introduced earlier [4], when the cell is in a stand by cycle, *M*5 is turned off by keeping wordline(*WL*) at ground, the bitlines are precharged to V_{DD}, and the data is preserved by the cross-coupled inverters.In the proposed 5T cell, as shown in Fig. 3, during stand by period (precharge stage) the wordline (*WL*) associated with *M*5 is set to low, which turns off *M*5, and bitlines are precharged to ground so that the data which was written during write operation is retained by the cross-coupled inverters.

B. Write Operation

The write operation is accomplished by effectively asserting the wordline (*WL*).Simultaneously, depending on

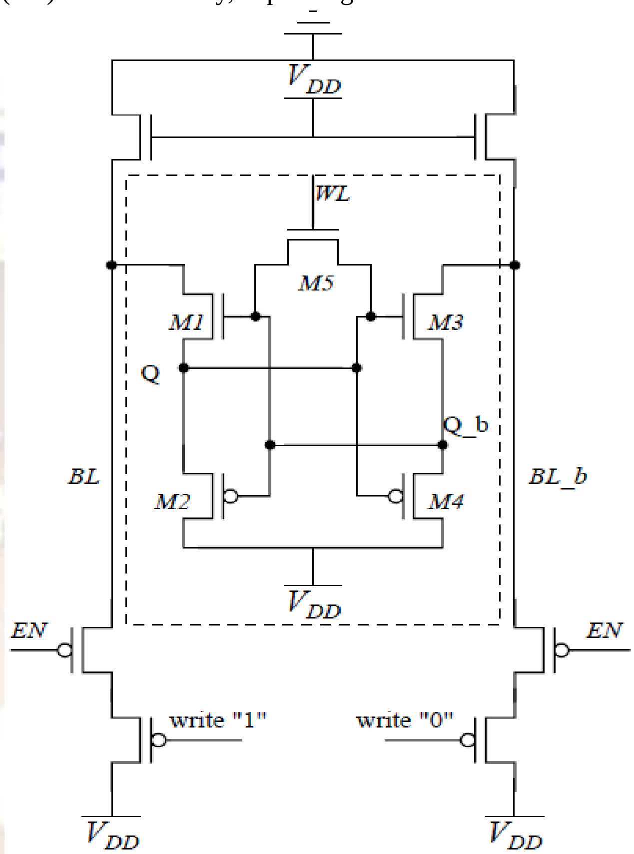

Fig. 3. Proposed 5T SRAM Cell

the state already stored in the cell, either write “0” or write “1” signalis activated to push one of the bitlines to approximately 2/3 V_{DD} so that the contents of the cell will flip to reflect the bitline data. Consider the situations for the two possible write operations that can be performed on the cell:

Write “0” Operation

Assume that initially, i.e. before write “0” operation, the values of the Q and Q_b of the cell are at “1” and “0” respectively. In this stage, transistors *M*2 and *M*3 are in the triode region, and *M*1 and *M*4 are in cut-off. The operation of write “0” is accomplished by forcing *BL_b* to approximately 2/3V_{DD} by turning on both the PMOS transistors associated with write “0” and *EN* signals. Now the source voltage of the NMOS transistor *M*3 is at approximately 2/3 V_{DD} rather than “0”, and there is a charge transfer between input terminals of the inverters because of turn on transistor *M*5. Thus Q_b is getting charged towards V_{DD} due to *M*3, which is conducting in the triode region. When the voltage at Q_b exceeds the threshold voltage of M1, the voltage at Q starts discharging towards “0”. This initiates a regenerative effect between the two inverters [5]. Eventually, $M2$ turns off and the voltage at Q falls to “0” due to the pull-down action of $M1$. Simultaneously, $M4$turns on and the voltage at Q_brises to V_{DD} due to the pull-up action of $M4$. When the cell finally flips to the new state, the wordline associated with $M5$ is returned to its low stand by level.

Write “1” Operation

Assume that initially, i.e. before write “1” operation, the values of the Q and Q_b of the cell are at “0” and “1” respectively. In this stage, transistors $M1$and $M4$ are in the triode region, and $M2$ and $M3$ are in cut-off. The operation of write “1” is accomplished by forcing *BL* to approximately 2/3 V_{DD} by turning on both the PMOS transistors associated with write “1” and *EN* signals. Now the source voltage of the NMOS transistor $M1$ is at approximately 2/3 V_{DD} rather than “0”, and there is a charge transfer between input terminals of the inverters because of turn on transistor $M5$. Thus Q is getting charged towards V_{DD} due to $M1$, which is conducting in the triode region. When the voltage at Q exceeds the threshold voltage of $M3$, the voltage at Q_b starts discharging towards “0”. This initiates a regenerative effect between the two inverters [5]. Eventually, $M4$ turns off and the voltage at Q_b falls to “0” due to the pull-down action of $M3$. Simultaneously, $M2$ turns on and the voltage at Q rises to V_{DD} due to the pull-up action of $M2$. Both write operations are clearly shown in Fig. 4.

C. Read Operation

The read operation is achieved simply by asserting the wordline (*WL*), which is associated with the additional transistor$M5$. Consider the situations for the two possible read operations that can be performed on the cell:

Read “0” Operation

Assume that a “0” is stored in the cell, which implies that Q and Q_b of the cell are at “0” and “1” respectively. Therefore, transistors $M1$ and $M4$ are in the triode region and $M2$ and $M3$are in cutoff. Initially, *BL* and*BL_b*are precharged toa low voltage around ground by a pair of column pull-down transistors as shown in Fig. 3. The wordline (*WL*), held low in the stand by state, is now raised to V_{DD} which turns on additional transistor $M5$, which in turn creates a current path from the bitline to V_{DD} through the cell. This results in the voltage at Q increases to a littleamount from ground and at the same time the voltage at Q_b decreases by a little amount from V_{DD}. The voltage at Q is transferred immediately to *BL* due to $M1$, which is conducting in the triode region.Meanwhile, on the other side of the cell, the voltage on *BL_b* remains low since thecolumn pull down transistor dominates the transistor $M3$, which is conducting at the edge of the cut-off region. The difference between *BL* and *BL_b* is fed to a sense amplifier in a proper manner to generate a valid low output, which is then stored in a data output buffer. In contrast to conventional 6T SRAM cell, here the bitlines are fed to the sense amplifier in inverted fashion to read proper data from the cell. Upon successful completion of read cycle, the wordline (*WL*) is returned to its low stand by level and both the bitlines are precharged back to a value around ground.

Read “1” Operation

Assume that a “1” is stored in the cell, which impliesthat Q and Q_b of the cell are at “1” and “0” respectively. Therefore, transistors $M2$ and $M3$ are in the triode region and $M1$ and $M4$are in cutoff.Initially, *BL* and*BL_b*are prechargedtoa low voltage around ground by a pair of column pull-downtransistors asshown in Fig. 3. The word

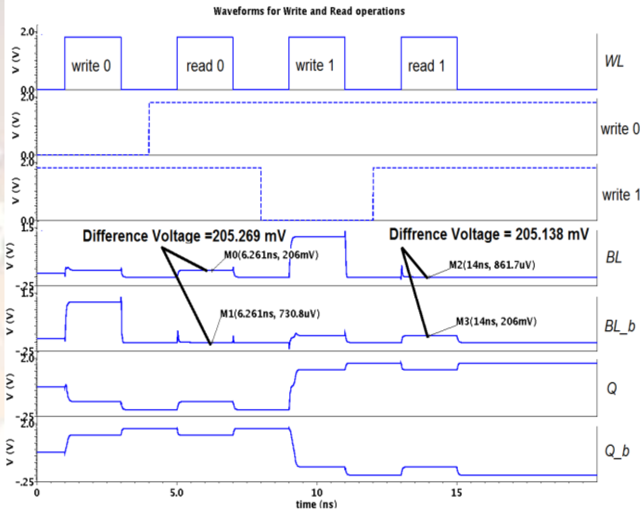

Fig. 4. Waveforms for writeand read operations of proposed 5T SRAM

line (*WL*), held low in the stand by state, is raised to V_{DD} which turns on additional transistor $M5$, which in turn creates a current path from the bitline to V_{DD} through the cell. This results in the voltage at Q_b increases to little amount from ground, and at the same time the voltage at Q decreases by a little amount from V_{DD}. The voltage at Q_b is transferred immediately to *BL_b* due to transistor $M3$, which is conducting in the triode region. Meanwhile, on the other side of the cell, the voltage on *BL* remains low since the column pull down transistor dominates the transistor $M1$, which is conducting at the edge of the cut-off region. As mentioned in read “0” operation, here also the difference between *BL* and *BL_b* is fed to a sense amplifier in a proper manner to generate a valid high output. The length of the additional transistor $M5$ is 3-4 times longer than the minimum length (L_{min}), and all the transistor sizes have been properly designed so that the cell can preserve data during read operation. Both the read operations are clearly shown in Fig. 4.

III. Static Noise Margin Analysis of Proposed Five Transistor SRAM Cell

The stability and robustness of a proposed SRAM cell is usually evaluated by analyzing both its dynamic and static behavior during the write, read, and hold operations. Stability of the memory cell can be estimated from the static noise margin (SNM) analysis. SNM is defined as the minimum DC noise voltage needed to flip the cell state [6],and is used to quantify the stability of the SRAM cell using a static approach. A significant effort has been devoted to explore the impact of process variations using the SNM. Here about proposed 5T SRAM cell's static stability during read and hold period has been presented, and the differences between SNM during hold and read modes are compared. The read mode is usually identified as the cell's weakest mode.

A. SNM During Hold Mode

The SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that the cell can tolerate at the output nodes of the cross-coupled inverters without flipping the cell. The graphical method to determine the SNM uses the static voltage transfer characteristics (VTC) of the SRAM cell inverters.

Fig. 5 superimposes the VTC of one inverter to the inverse VTC of the other inverter. The resulting two lobed graph is called a "butterfly" curve and is used to determine SNM. Its value is defined as the side length of the largest square that can be fitted inside the lobes of the "butterfly" curve [6]. Fig. 5 shows that the variation of the "butterfly" curves for two supply voltages (V_{DD}, 2/3 V_{DD}) during hold operation. It clearly shows that lowering the power supply voltage reduces the SNM.

B. SNM During Read Mode

Static noise margin is a key performance factor to estimate the ability of the cell that can preserve data during the read operation. SNM during read can be evaluated from voltage transfer characteristic curves obtained by setting wordline (*WL*) to high, while both the bitlines are precharged to a low voltage around ground. Generally, SNM during read takes its lowest value and the cell is in its weakest state.

The "butterfly" curves, shown in Fig. 6, are formed by superimposing of both inverter VTCs taken under read operation. Fig. 6 shows the variation of SNM for two power supply voltages during read operation, and degradation of the static noise margin with reduction of power supply voltage.

The SNM during hold and read operation for two different power supply voltages corresponding to an SRAM

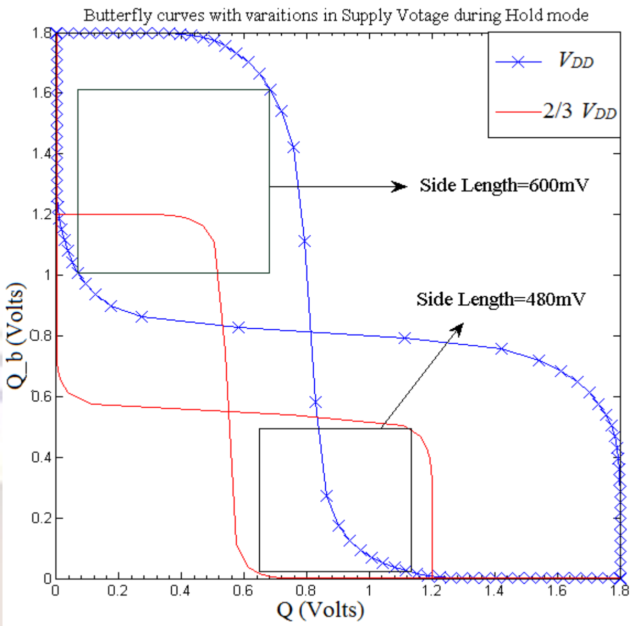

Fig. 5. "Butterfly" curves during Hold operation

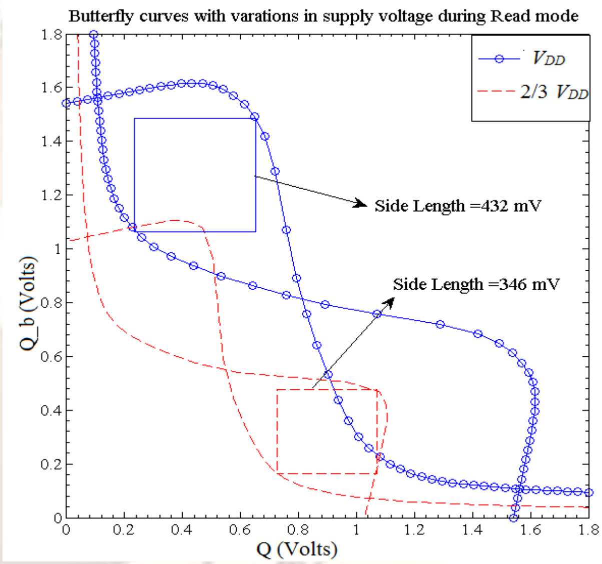

Fig. 6. "Butterfly" curves during Read operation

cellwith cell ratio (r) of 2 are tabulated in Table I. Cell ratio(r) is defined below:

$$Cellratio(r) = \frac{\beta_{driver}}{\beta_{access}} (1)$$

Where, β_{driver} is the transconductance of the storage transistors and β_{access} is the transconductance of the access transistors. $M1$ and $M3$ act as access transistors and $M2$ and $M4$act as storage or driver transistors in the proposed design.The SNM reduction during read operations with respect to hold operations is considerable at each supply voltage.

C. *Impact of Power Supply Voltage Modulation on Read SNM*

Fig. 7 shows that the impact of power supply voltage reduction on read SNM under various process corners. It is clear that irrespective of the process variations, SNM is reduced significantly with the reduction of power supply voltage. Hence, it is more preferable to maintain full V_{DD} while reading the memory.

IV. SIMULATION RESULTS

The above implemented proposed 5T SRAM with cell ratio (*r*) of 2 was simulated along with conventional 6T and novel 5T SRAM cells in 180 nm CMOS process using Cadence Spectre and BSIM3v3 models.

SNM DURING HOLD AND READ OPERATIONS VERSUS POWER SUPPLY VOLTAGE

Mode of operation	**SNM@V_{DD}(mV)**	**SNM@2/3 V_{DD} ((mV)**
HOLD	600	480
READ	432	348

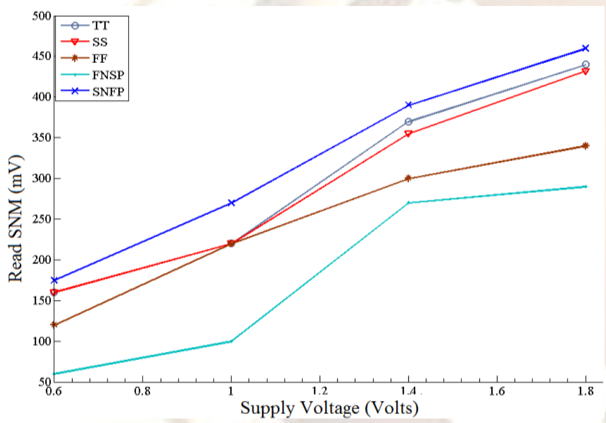

Fig. 7. Impact of Power Supply Voltage Reduction on Read SNM

The layout of the proposed 5T SRAM cell is shown in Fig.8, and all the parasitic capacitances, which were extracted from the layouts, along with some additional bitline capacitance approximately 100 fF are included during simulations. The comparison of the proposed 5T SRAM to the conventional 6T and novel 5T SRAMs are tabulated in Table II and Table III respectively. It is observed that the proposed 5T SRAM cell shows good stability over both the conventional 6T and novel 5T SRAMs with better performance and low power consumption.

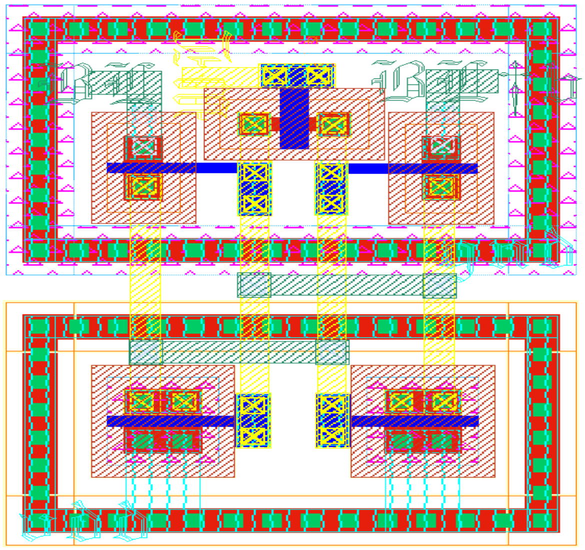

Fig. 8.Layout of theProposed 5T SRAM Cell

TABLE I. PERFORMANCE COMPARISON BETWEEN PROPOSED 5T AND CONVENTIONAL 6T SRAM CELLS

Metric	**Conventional 6T SRAM**	**Proposed 5T SRAM**	**%Improvement**
Read SNM	255 mV	432 mV	40.97
Write Delay	120 ps	101.41 ps	15.49
Read Delay	392.4 ps	303.46 ps	22.66
Power Consumption	139.14 µW	117.1µW	15.84

TABLE II. PERFORMANCE COMPARISON BETWEEN PROPOSED 5T AND NOVEL 5T SRAM CELLS

Metric	**Novel 5T SRAM**	**Proposed 5T SRAM**	**%Improvement**
Read SNM	400 mV	432 mV	7.4
Write Delay	300 ps	101.41 ps	66.19
Read Delay	469 ps	303.46ps	35.29
Power Consumption	122.94 µW	117.1 µW	4.75

V. CONCLUSION

With the aim of attaining a high stability and better performance SRAM, a five transistor (5T) SRAM cell is designed and simulated using a 180 nm CMOS process. The proposed cell exhibits 22.66% better performance with respect to conventional 6T, and 35.29% improvement with respect to novel 5T SRAM cell. Read static noise margin of the proposed cell is 40.97% higher than the conventional 6T SRAM cell with significant reduction in power consumption. Simulated results, as seen from process corner analysis, quite well justify the robustness of the design even at worst case process variations. Therefore, the proposed 5T SRAM cell design would be suitable for various high speed and low power embedded cache, stand-alone IC, and network applications.

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