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FPGA Implementation of cache memory

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Abstract
We describe cache memory design suitable for use in FPGA-based cache controller and processor. Cache systems are on-chip memory element used to store data. Cache serves as a buffer between a CPU and its main memory. Cache memory is used to synchronize the data transfer rate between CPU and main memory. As cache memory closer to the micro processor, it is faster than the RAM and main memory.The advantage of storing data on cache, as compared to RAM, is that it has faster retrieval times, but it has disadvantage of on-chip energy consumption. In term of detecting miss rate in cache memory and less power consumption, The efficient cache memory will proposed by this research work, by implementation of cache memory on FPGA. We believe that our implementation achieves low complexity and low energy consumption in terms of FPGA resource usage.

Keywords- cache Tag memory, cache controller, counter, cache Tag comparator**.**

I. INTRODUCTION

Field-programmable gate arrays (FPGAs) have recently been garnering attention for their successful use in computing applications. Indeed, recent work has shown that implementing computations using FPGA hardware has the potential to bring orders of magnitude improvement in energy-efficiency and throughput vs. realizing computations in software running on a conventional processor. While a variety of different memory architectures are possible in processor/accelerator systems, a commonly-used approach is one where data shared between the processor and accelerators resides in a shared memory hierarchy comprised of a cache and main memory. The advantage of such a model is its simplicity, as cache coherency mechanisms are not required despite this potential limitation; we use the shared memory model as the basis of our initial investigation, with our results being applicable (in future) multi-cache scenarios[1]. In our work, data shared among the processor and parallel accelerators is to accessed through a shared L1 cache, implemented using on-FPGA memory.

Cache systems are on-chip memory element used to store data. A cache controller is used for tracking induced miss rate in cache memory. Any data requested by microprocessor is present in cache memory then the term is called 'cache hit'. The advantage of storing data on cache, as compared to RAM, is that it has faster retrieval times, but it has disadvantage of on-chip energy consumption. This paper deals with the design of efficient cache memory for detecting miss rate in cache memory and less power consumption. This cache memory may used in future work to design FPGA based cache controller.

II.SYSTEM ARCHITECTURE OVERVIEW

Cache controller that communicates between microprocessor and cache memory to carry out memory related operations. The functionality of the design is explained below.

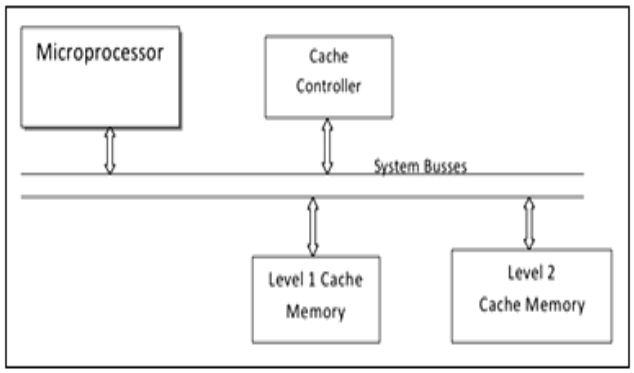

Fig 1 - system block diagram

Cache controller receive address that microprocessor wants to access Cache controller looks for the address in L1 cache. If address present in L1 cache the data from location is provided to microprocessor via data bus. If the address not found in L1 cache then cache miss will occur. Cache controller then looks same address in cache L2. If address present in L2 cache the data from location is provided to microprocessor. The same data will replace in cache L1. If the address not found in L2 cache then cache miss will occur.

In our paper work we design single cache memory for detecting miss rate in cache memory and less power consumption. This work will be used in design of FPGA based 2-way, 4-way, 8-wayset associative cache memory and used in cache controller for tracking induced miss rate.

III. DESIGNED WORK

In our designed work, we designed cache memory L1 using FPGA. In future with reference to designed work we can design set associative cache memory as set associative cache strike a good balance between lower miss rate and higher cost[5]. Cache memory consist Cache tag memory, cache data memory, cache tag comparator and counter. Our paper work deal with detection of cache misses. We designed cache tag memory, cache tag comparator and 10-bit counter and need not to design cache data memory for detecting cache misses as address is stored in tag memory and data is stored data memory. Address Requested by microprocessor is compared with address of data in main memory those are stored in tag memory.

The cache tag memory stored address of data in main memory. Cache tag memory is modelled using behavioural style of modelling in VHDL (for example: 22-bit cache tag memory).

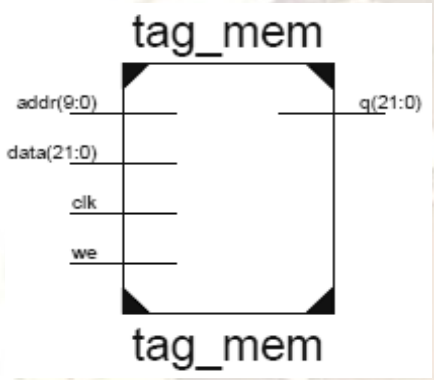

Figure 2: cache tag memory

Figure 2 shows the diagram of cache tag memory of 22 bit. When 'we'=1 it performs writing operation and 'we'=0 it performs reading operation. Data stored in the tag memory will be a addresses of main memory. The 10-bit counter used to generate 10 bit address for writing and reading operation of cache tag memory**.** 10-bit counter is modelled using behavioural style of modelling in VHDL.

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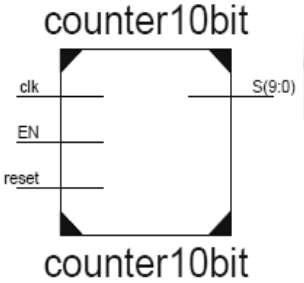

Figure 3: 10-bit Counter

Figure 3 shows the diagram of 10-bit counter. For each clock pulse counter is incremented by one. 10-bit counter provides 10-bit addresses to cache tag memory during writing and reading operation. The 22-bit cache tag comparator Cache tag comparator is used to compare address requested by microprocessor and address stored in tag memory. 22-bit cache tag comparator is modelled using behavioural style of modelling in VHDL.

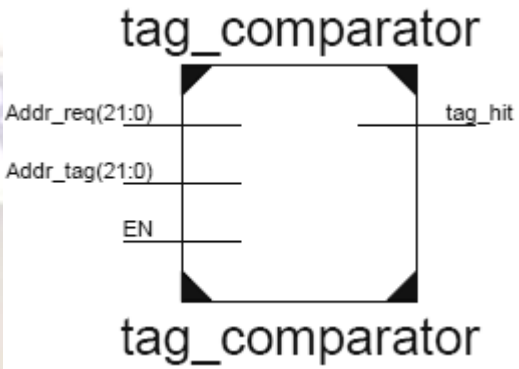

Figure 4: 22-bit cache tag comparator

Figure 4 shows the diagram of 22-bit cache tag comparator .22-bit Cache tag comparator is compare 22-bit address requested by microprocessor and 22-bit address stored in tag memory. Address requested by microprocessor is 32-bit out which 22-bit address is used to compare with tag address.8-bit address is used as a set address and 2-bit address is used as a offset word address. To design set associative cache memory, we have to make number of sets of such cache memory which will be our future work.

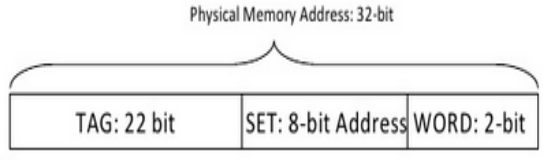

Figure 5: physical memory address

The implementation of cache memory requires cache tag memory, 10-bit counter and cache tag comparator as shown in figure 6

IV: SIMULATION RESULTS

Figure 7 shows the simulation results of cache memory. Cache memory is written in a VHDL. modelsim platform is used for simulation. To achieve the synthesis of cache memory, Xilinx platform is used. as shown in simulation results it is found that if address requested by microprocessor is matched with the address stored in cache tag memory then the cache hit will occurs, if not then cache miss will occurs.

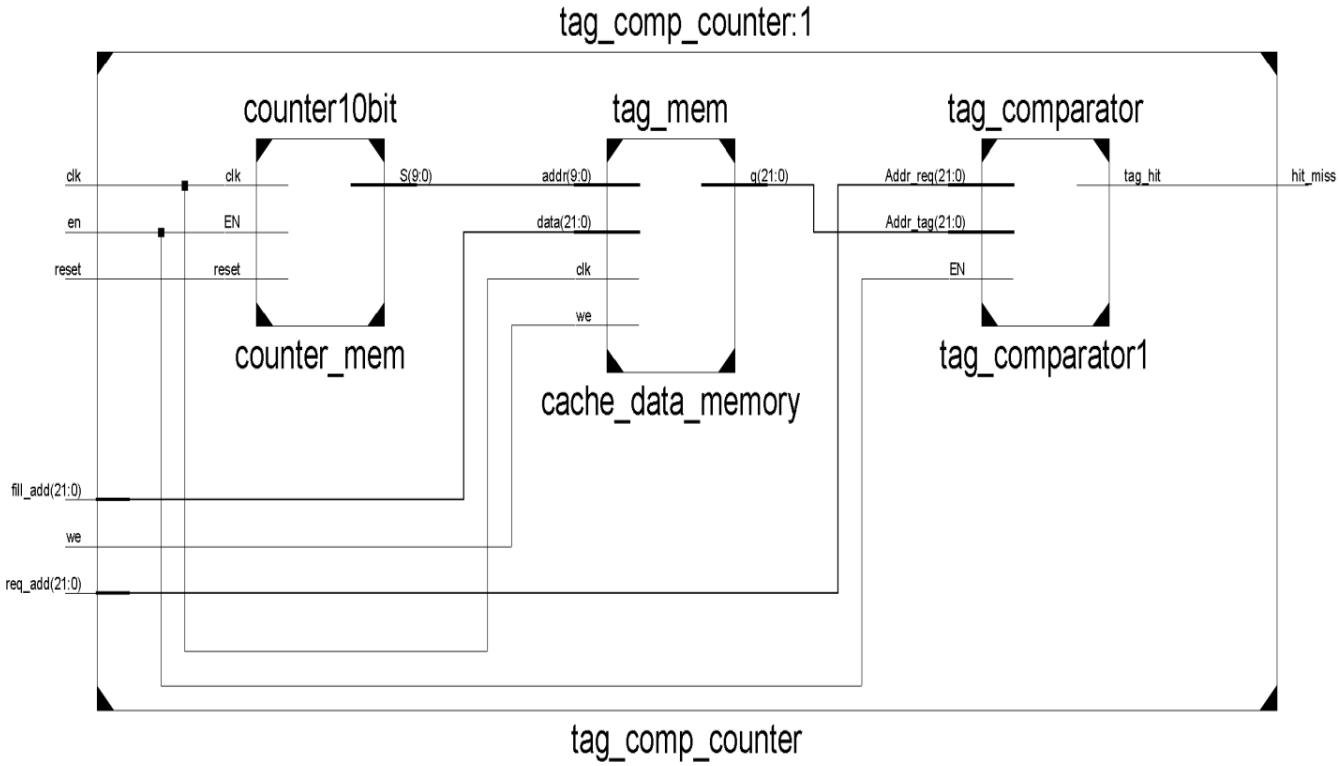

Figure 6: cache memory

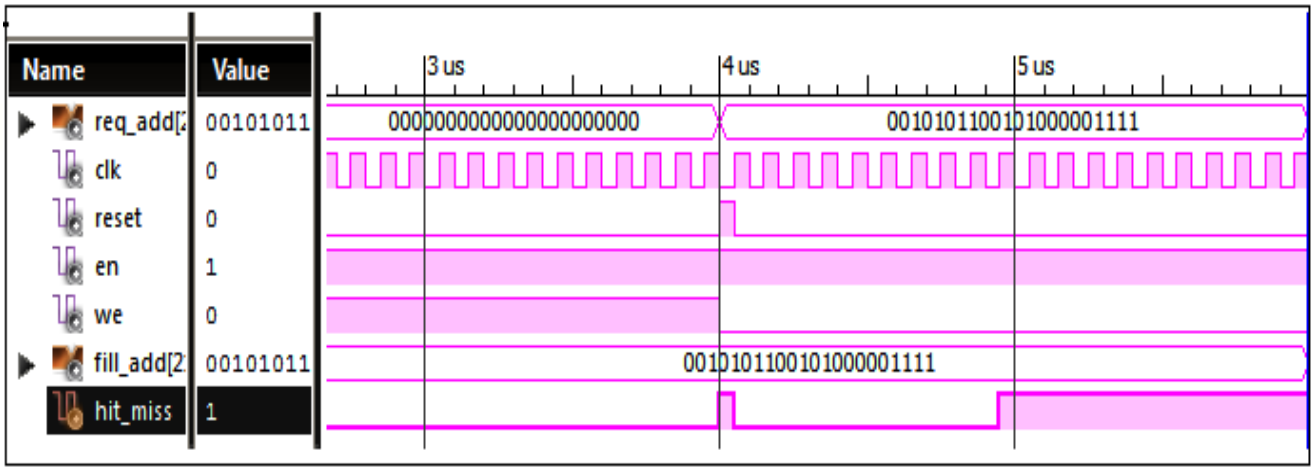

Figure 7: simulation results

VII. CONCLUSION

In this paper, we have presented design of cache memory on FPGA for detecting cache miss. Such an approach would be of great utility to many modern embedded applications, for which both high-performance and low-power are of great importance. This cache memory may used in future work to design FPGA based set associative cache memory and cache controller for tracking the induced miss rate in cache memory.

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