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3G Receiver system level design

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Abstract

In order to meet the requirements of telecommunication hardware standards and general Technology for mobile networking systems, A3G mobile networks based on the International Telecommunication Union(ITU) family of standards is conceived from Universal Mobile TelecommunicationService (UMTS) concept for high speed networks forenabling variety of data intensive applications. It consists of two main standards – CDMA 2000 &W-CDMA3G network operators offer wide range of advanced service to its users and it can be achieved by Spectral efficiencyServices – wide-`area wireless voice Telephone, videocalls, and broadband wireless, data all in a mobile environment [1,2,3,4].

A key requirement in future wireless system is their ability to provide broadband connectivity with end-to-end Quality of Service (QoS), a high network capacity, and throughput at a low cost. In this paper, a 3G RF front end system is proposed as a broadband communication system [5, 6, 7].

Keywords;3G; ITU; UMTS; CDMA2000; W-CDMA

I. INTRODUCTION

In this paper the UMTS band I standard specifications are fetched. A direct conversion receiver system is chosen. The available RFICs are explored from different vendors, such as Avago, Maxim, Dallas, Hittite, Mini-Circuits, Analog Devices, Ma-com, Triquint and Anatec Electronics, then, the optimum components are selected according to the required design specifications. The chosen ICs are modeled either using the available vendors models or by creating behavioral models to achieve a system simulation for the proposed receiver chain using Agilent Advanced Design System.

II. SYSTEM LEVEL DESIGN OF 3G DCR

A. Proposed 3G DCR.

Figure 1 shows a simple block diagram of direct-conversion transceiver architecture [11, 12, 13]. Based on this architecture, a complete system level design calculations (sensitivity, noise figure, third order intercept point, etc.) for the target 3G UMTS Band I UE receive RF front end is carried out, to get out with the necessary circuit blocks required for the implementation. Based on these calculations, corresponding circuit building blocks from different vendors are surveyed. Appropriate choices that achieve the required specs given in Table 1**Error! Reference source not found.** are made.

B. Specifications and proposed block diagram.

Table 1 :main characteristics of a 3G receiver

Specifications	Limits
Sensitivity	≤ -117 dBm
Selectivity	≥ 33 dB @ ±5 MHz (ACS) *≥ 43 dB @ ±10 MHz*
Linearity	*IIP2: 8 → 47 dBm* *IIP3: -21.3 → -8 dBm*
Noise	*SNR ≥ -18.9 dB* NF ≤ 7.9 dB (Phase Noise)LO ≤ -128.9 dBc/ Hz
Gain	*Gain: 22 → 95 dB*
Power	*Pin : -117 → -25 dBm*

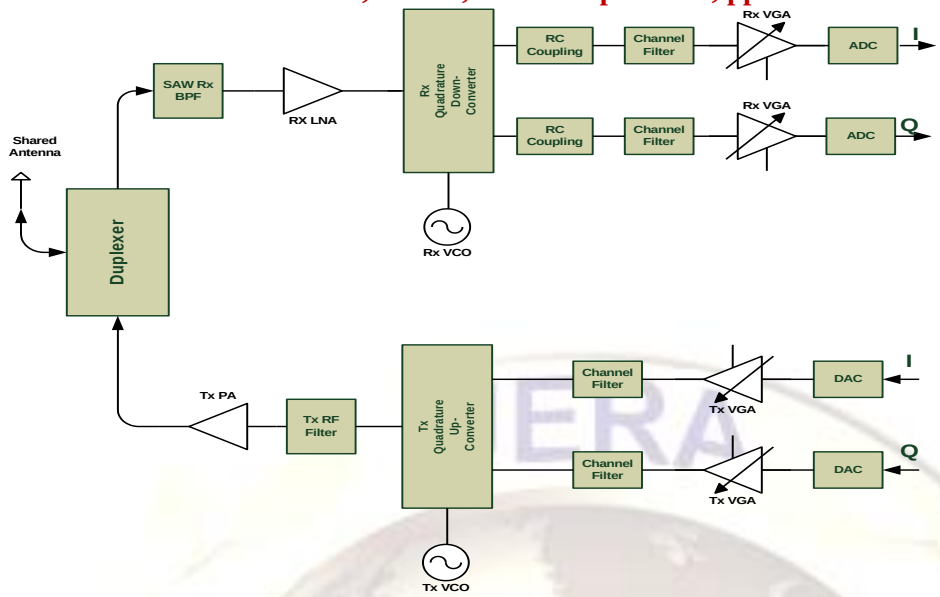

Figure1: Block diagram of a zero-IF W-CDMA transceiver front-end.

III. CHOICE OF RFIC COMPONENTS FOR DIFFERENT STAGES

Based on the block diagram of the entire receiver shown in figure 1, we are Targeting to implement the RF front end portion only (i.e. from the antenna to the Demodulator) that satisfies the extracted specifications, using the available ICs in the international market [15, 16].

A. Duplexer Selection

The chosen duplexer is [ACMD-7612] by Avago, which provides 1.1 dB insertion loss from the antenna to the receiver (2110 → 2170) MHz, 1.1 dB insertion loss from the transmitter (1920 → 1980) MHz to the antenna and about 55 dB isolation between the transmitter and the receiver.

B. Receiver SAW filter Selection

The chosen Rx SAW band-pass filter (BPF) is the [856562] by [Triquint] and it has the frequency response contributes about -2 dB in the losses and provides good out-of band attenuation. It also provides about 48 dB attenuation to the noise of the associated transmitter signal, which will help in avoiding the desensitization of the receiver by the transmitter interferer.

C. RF Gain and Low Noise Amplifier Selection

Two identical LNA RFICs are chosen; each is [MGA-14516] by Avago that provides the possible minimum noise figure. The typical parameters of each are (G = 31.7 dB, NF = 0.68, IP3 = 38dBm, OP1db=23.5) .

D. Voltage Controlled Oscillator (VCO)

Our choice was the [HMC384LP4] by Hittite that achieves these specs especially in the required phase noise & output power level. A source modeling for such a VCO is performed in ADS.

E. System Linearity and Downconverter Selection

Our choice converged to Maxim's MAX2023, which achieves the required specs, the blocks used within this behavioral model especially the double balanced mixer is simulated on its own.

IV. SYSTEM INTEGRATION

The complete block diagram of the receiver front-end chain with the chosen components is shown in next figure.

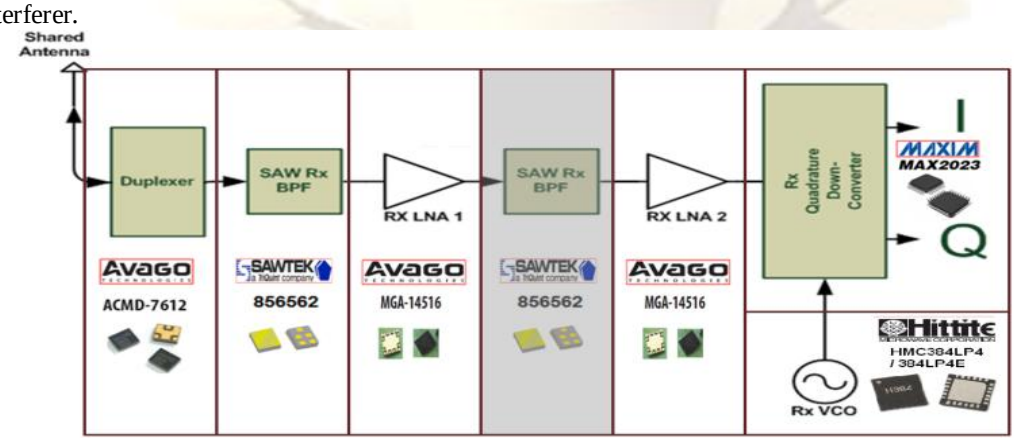

Figure2: block diagram of the receiver front-end with the chosen components.

Since the passive filters are extremely linear, their IIP3 is infinite but they are modeled as 100 dBm and they contribute by their loss in the total noise figure.

The noise figure of cascade n-noisy stages can be derived in terms of the noise figures and gains of the individual blocks. Generally, this is known as Friis formula from equation 1[17, 18, 19, 20, and 21]:

$$F = F1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \frac{F_g - 1}{A_1 A_2 \ldots A_{g-1}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where NF total is the cumulative noise figure of n stages referring to the input of the first stage, N_{Fn} is the noise figure of the g_{th} stage; A_i is the power gain of the g_{ith} stage.

IIP3 in n -Cascade Stages

$$\frac{1}{IIP_3} = \frac{1}{IIP_{3,1}} + \frac{A_1}{IIP_{3,2}} + \frac{A_1 A_2}{IIP_3,_3} + \ldots \frac{A_1 A_2 A_3 .. A_{N-1}}{IIP_3, N} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

In a cascaded system, the overall IIP3 of the system is given by it can be seen from the equation 2 that in a cascade system the linearity requirements on the blocks at the back-end are more stringent because their effects on the overall system are "magnified" by the preceding gain [22, 23].

The next table shows system calculation, total noise figure, total gain, and total third intercept point.

Table 2: System calculations.

	Duplexer	**Band Pass Filter**	**Low Noise Amplifier 1st Stage**	**Low Noise Amplifier 2nd Stage**	**I-Q Down Conversion**
Component Data (from datasheets):					
Gain (dB)	-1.1	-2	31.7	31.7	-9.5
N.F(dB)	1.1	2	0.68	0.68	9.6
IIP3 (dBm)	100	100	38	38	38
Calculated Linear data [=10 ^ (db/10)]:					
Gain (linear)	0.776	0.631	1479.11	1479.11	0.112
N.F(linear)	1.288	1.585	1.169	1.169	8.913
IIP3 (mw)	$1*10^{10}$	$1*10^{10}$	6309.57	6309.57	6309.57
Running Total (cascaded) Gain [product of linear gain]:					
Stage	G1	G1.G2	G1.G2.G3	G1.G2.G3,G4	G1.G2.G3.G4.G5
Gain (linear)	0.776	0.49	724.255	1071252.94	119980.329
Total Noise figure (linear) = 2.39 → Total Noise figure(dB) = 3.79					
Total IIP3(linear) =5.886*10^{-3} → Total IIP3(dBm)= -22.3					
Total Gain(dB) = 50.8					

The complete block diagram of the receiver front-end chain with the specifications of the chosen components is shown in figure 3. The power levels at each component are shown too for both RF detected signal and the Transmitter interferer.

As shown in figure 3, the duplexer and receiver saw bandpass filter strongly attenuates the Transmitter signal in order not to desensitize the receiver front-end, also this attenuation must assures that this signal cannot saturate the LNA of the receiver where the Transmitter signal level did never exceed the compression points of any stage of the LNA stages at the receiver. But here the second stage of LNA will saturate since the Transmitter signal level exceed the compression points, and by system by adding filtration stage between the two stage of LNA figure 3shows that

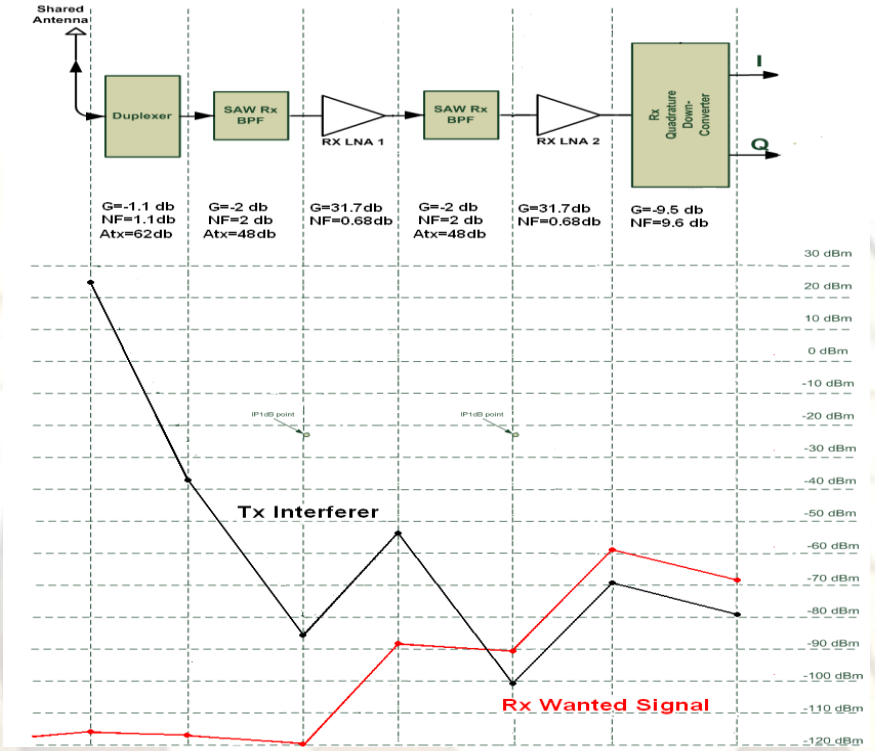

Figure3: modified Entire system profile diagram.

The overall gain is in order of 63.4dB (gain) – 14.6 dB (losses) i.e. 48.8 dB RF gain. Also the wanted signal at the receiver propagates, within the receiver front-end chain, without reaching neither the compression point of any stage nor the third-order intercept point at any stage and succeeds the dynamic range of the receiver specs in table 1. Avoiding reaching the compression point of any stage assures a proper linear operation without saturating any of the active components within the chain, whereas avoiding reaching the value of the third-order intercept point assures minimum intermodulation distortion and better receiver sensitivity. The entire system is powered using a 5 V source, it consumes a DC current of 362 mA, with a total DC power consumption of 1.81W.

V. CONCLUTION

A complete system level design, for the RF receiver front end of a 3G UMTS Band I user equipment, has been designed based on direct conversion architecture. The appropriate components from different vendors have been chosen. Necessary simulations that quantify the performance of such components have been performed based on Agilent Advanced Design System. Finally, an overall system performance is simulated and compared to the main required specifications of UMTS Band I, most of the requirements are satisfactory obtained except for linearity issue which may need some extra enhancement. Also, the VCO is not achieving the required phase noise.

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