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Harmonic Compensation and Load Balancing Using Cascaded H-bridge Multilevel Inverter in High Voltage Systems

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ABSTRACT

This paper presents detailed modeling and simulation of a compensator for Load balancing and harmonics Compensation based on a five-level cascaded H-bridge multilevel voltage source inverter. This type of compensator, which is installed in parallel with the load, is usually referred to as the shunt active power filters (APF). Nowadays use of high voltage non-linear loads are widely used in industrial and commercial applications and elimination of harmonics in HV system has become an important aspect. Implementation of multilevel inverter (MLI) as compensator in HV system eliminates use of bulky and high cost transformer.The compensation process is based on concept of p-q theory, which is comprised of positive sequence voltage and instantaneous real-power theory. The controller method successfully eliminates harmonics even the supply voltage is distorted. The Phase Shifted Carrier PWM (PSCPWM) technique is used to generate firing angles to cascaded H-bridge multilevel inverter (CHBMLI) switches which reduces the individual device switching frequency.The distribution network which supplies mixed linear and non-linear loads and employing MLI is simulated by MATLAB/SIMULINK software. The simulation result validates the proposed control method in high voltage system.

Keywords-Load Balancing, Harmonic Compensation, Multilevel Inverter, Active Power Filter, Phase Shifted Carrier PWM, Instantaneous P-Q Theory, High Voltage Systems.

I. INTRODUCTION

Nowadays non-linear and fluctuating loads, such as a diode/thyristor rectifiers, semi converters, arc furnaces, adjustable-speed drives, ac voltage regulators, etc., are widely used in industrial and commercial applications. These non-linear loads create harmonic and distortion current in electrical networks and have disadvantages such as: reducing electric power quality, increasing the losses of the distribution system and changing in power quality [1]. On the other hand this electric power delivered under conditions of unbalanced and non-sinusoidal source voltage system [2].

Passive filters are used for harmonic mitigation due to their advantages of simplicity, low cost and easy maintenance. But passive LC filters for reducing the current harmonic pollution are ineffective, because those are large in size, resonate with the supply impedance, have ageing and tuning problems and the filtering characteristics are dependent on the source impedance which is not exactly known [3].

To provide high power quality at the point of common coupling (PCC) of a distribution system, active power filters are widely studied recently, for the compensation not only of current harmonics produced by fluctuating loads, but also of reactive power and unbalance of non-linear and distorting loads[4],[5].

At low voltage levels, conventional two level inverters are used. At medium voltage levels, the conventional two level inverters either require interface transformers between the inverter terminals and the supply terminals or need active devices to be connected in series to achieve the required voltage levels [6]. In this case, use of transformer for medium or high voltage applications requires high VA rating of transformer which results in high magnitude of current on low voltage side and causes more losses. The system becomes bulky and costly [7]. The multilevel inverters are able to achieve the required voltage levels using devices of low voltage rating. The use of MLI also eliminates the need of transformer to feed the power to HV system [8],[9].
Three major kinds of multilevel inverters topologies are realized, namely, diode-clamped, flying-capacitor clamped and cascaded h-bridge multilevel voltage source inverter for generating smooth sinusoidal voltage. The major advantages of the CHBMLI over the other two types are summarized as follows [10]:

1) Construction and maintenance cost of H-bridge is less.
2) Requires a low number of components per level.
3) Simple voltage balancing modulation.
4) Maximum output can be utilized from the DC sources.
5) Possibility to implement soft-switching.

For higher-level applications, voltage balance control of diode-clamped converter shows no advantage with more than three DC capacitors, because the problem of capacitors' voltage balance is complicated when the output level beyond four. Moreover the higher the level is, the more serious the unbalance is. Many researchers have done much work [11],[12] on this but no effective method especially for topologies higher than five levels until now. This is one of the main reasons that block its industry application.

In this paper, the configuration of compensator based on five-levelcascaded H-bridge inverter without using the transformer is presented. Then, the proposed control technique for load balancing and harmonics compensation is discussed in detail.

This paper is organized as follows: Section II describes the MLI topology and modulation strategies in part A, B separately. Section III includes proposed controller method based on P-Q theory. Section IV gives the simulation results and analysis of five-level cascaded inverter simulation in two conditions. Finally, section V presents our conclusions.

II. Basic of Cascaded Multilevel Inverter

A. *Topology of the Inverter*

Cascaded multilevel inverter is one of the most important topology in the family of multilevel inverters. Multilevel inverters do not need a coupling transformer to interface it with high power system. A five level cascaded H-bridge inverter at the high voltage level has been considered and is operated at a carrier frequency of 3 KHz. The system configuration is shown in Figure 1.

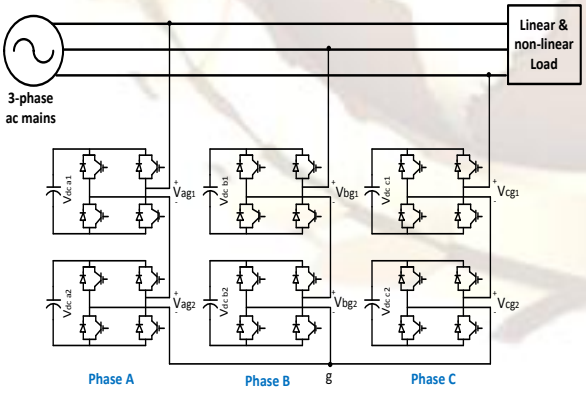

Fig. 1. Cascaded Multilevel Inverter

The cascaded multilevel inverter used here composed of six H-bridges and six dc capacitors. It is connected to the power system in parallel. The number of output phase voltage levels in a cascadedinverter is given as$m = 2s + 1$, where s is the number ofseparate dc sources and m is the inverter level. To obtain 5-level output, two H-bridges are used per phase as shown in Fig.1. If the dc voltage of each cell is set to the same value (Vdca1 = Vdca2 = E), then the resulting inverter can operate with five output voltage levels. Table I. shows the zero and positive voltage levels obtainable from this inverter as well as the voltage levels from the individual H-bridge cells [13].

Table I. output voltage of inverter for phase a

$V_{ag} = V_{ag1} + V_{ag2}$	V_{ag1}	V_{ag2}
0	E	-E
	0	0
	-E	E
E	E	0
	0	E
2E	E	E

B. *Modulation*

The modulation technique used is based on PSCPWMstrategy, In the phase shifted multicarrier modulation, all triangular carriers have same peak to peak amplitude and the same frequency but there is a phase shift between any two adjacent carrier waves of magnitude given by

$$\Phi_{cr} = \frac{360°}{m-1} \quad (1)$$

Where *m* is the voltage levels of MLI. Gate signals are generated by comparing the modulating wave with the carrier waves. In this PWM method the equivalent switching frequency of the whole converter is (m-1)times as the each power device switching frequency. This means PSCPWM can achieve a high equivalent switching frequency effect at very low real device switching frequency which is most useful in high power applications [13]. The carrier 1 and carrier 2 are used to generate gating for the upper switches in left legs of power cells H1 and H2 in Fig. 1 respectively. The carrier 1 and carrier 2 are two triangular carrier waves shifted by 90° from each other. The inverted signals are used for upper switches in the right legs. The gate signals for all lower switches operate in a complementary manner with respect to their corresponding upper switches.

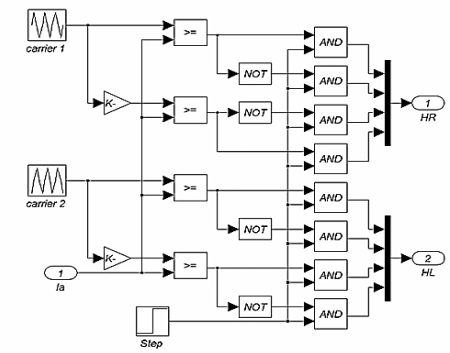

Fig 2. Gating Signal Generation by PSCPWM

Fig. 2 gives the block diagram to generate the gating signals, where modulating signal is MLI reference current and is compared with carrier 1 and 2. The advantage of PSCPWM that the semiconductor device can be used at comparatively low switching frequency so that switching loss is reduced greatly [13],[14].

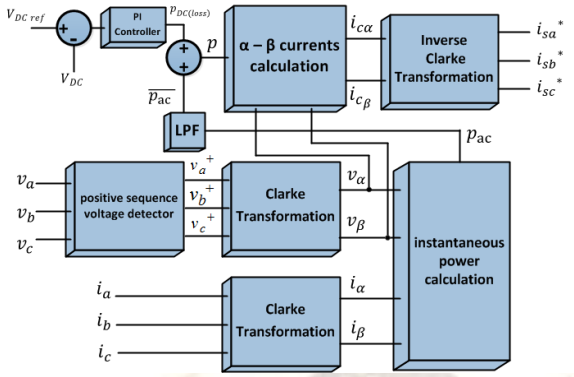

Fig 3. Control block diagram for reference current generation

III. Proposed Controller Based On P-Q Theory

The control block diagram Based Onp-q theory for the three phases MLI is shown in Fig. 3.The sinusoidal and immediately extraction control strategy is applied to extract the reference current or fundamental components from the distorted line current. This proposed controller is comprised of positive sequence voltage detector and real-power theory concept. Fundamentals of this theory were reported in [15] and many other publications. This postulate led to the formulation of the famous p-q theory of reactive power.

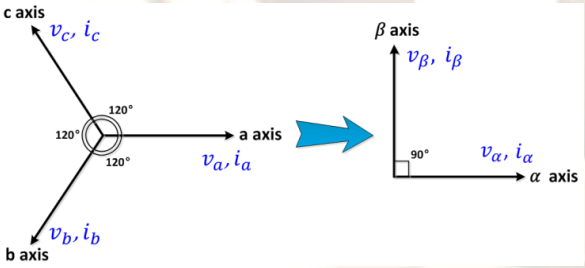

Fig 4. α-β coordinates transformation

The p-q theory is based on the α-β transformation, also known as the Clarke transformation. With considering Fig. 4, for simple calculation, the three-phase voltages and currents are considered only, excluding zero-sequence components.

The positive-sequence voltage detector consists of PLL circuit and instantaneous real-power calculation is shown in fig. 5. The balanced or distorted voltage sources are transformed into the α-β coordinates using Clarke transformation

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (2)$$

An integrated circuit with a VCO chip (PLL circuit) should determine accurately the fundamental frequency(f_v+) of the system voltage, subsequently, PLL-circuit produced auxiliary signals i_α' and i_β'. These currents used to calculate the auxiliary powers p' and q' follows as

$$p' = v_\alpha i_\alpha' + v_\beta i_\beta' \quad (3)$$

Similarly, the instantaneous reactive power is defined as

$$q' = v_\beta i_\alpha' + v_\alpha i_\beta' \quad (4)$$

Using a first order Low Pass Filter (LPF), the average $\overline{p'}$ and $\overline{q'}$ powers are composed onlyfrom the fundamental positive sequence voltage, since the auxiliary currents are also composed only from a fundamental positive sequence component. The instantaneous voltagesv_α' andv_β' it can be derived as

$$\begin{bmatrix} v_\alpha' \\ v_\beta' \end{bmatrix} = \frac{1}{(i_\alpha')^2 + (i_\beta')^2} \begin{bmatrix} i_\alpha' & i_\beta' \\ i_\beta' & -i_\alpha' \end{bmatrix} \begin{bmatrix} \overline{p'} \\ \overline{q'} \end{bmatrix} \quad (5)$$

Finally, the instantaneous three-phase voltages values (v_a^+, v_b^+, v_c^+) of the fundamental positive sequence voltage, are determined by applying the inverse Clarke transformation, it derived as

$$\begin{bmatrix} v_a^+ \\ v_b^+ \\ v_c^+ \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha' \\ v_\beta' \end{bmatrix} \quad (6)$$

The positive sequence voltage detector prepares good dynamic response and satisfactory even under unbalanced or distorted voltage source conditions.

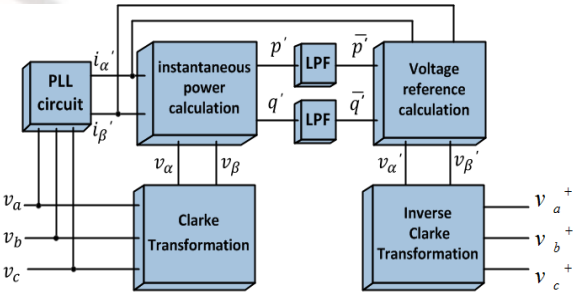

Fig. 5. Block diagram of the fundamental positive-sequence voltage detector.

After producing positive sequence of voltage, reference current generation is obtained. According to Fig. 4, the instantaneous space vector voltage and current v_a, i_a are set on the a-axis, v_b, i_b are on the b-axis, and v_c, i_c are on the c-axis. These space vectors are easily transformed into α-β stationary. It consists in a real matrix to transform measured three-phase source voltages (v_a, v_b, v_c) and source currents (i_a, i_b, i_c) into the α-β stationary reference frame as shown in (7) and (8).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (8)$$

Conventional instantaneous real-power for three-phase circuit can be defined as

$$p_{ac} = v_\alpha i_\alpha + v_\beta i_\beta \quad (9)$$

The instantaneous real-power (p_{ac}) is passing through Butterworth design based LPF. The LPF cut-off frequency 50 Hz that allows only the fundamental signal to the active power section that calculates the AC components of the real-power losses.

The DC-power loss is calculated from the comparison of the dc-side voltage of the cascaded multilevel inverter and desired reference voltage. The proportional integral-controller [$K_p = 1$, $K_i = 163$,] is determining the dynamic response and settling time of the dc-side voltage. The DC component power losses can be written as

$$p_{DC(loss)} = \left[v_{DC\ ref} - v_{DC}\right]\left[k_p + \frac{k_i}{s}\right] \quad (10)$$

The instantaneous real-power (p) is calculated from the AC component real-power losses and the DC component power losses($P_{DC(Loss)}$). It can be defined as follows

$$p = \overline{p_{ac}} + p_{DC\,(loss)} \quad (11)$$

The AC and DC component of the instantaneous real power p is related to the harmonic compensation currents. The instantaneous current on the α – β stationary of $i_{c\alpha}, i_{c_\beta}$ are divided into two kinds of instantaneous current components: real-power losses and reactive-power losses, but this proposed controller calculates only the real-power losses [8]. The α – β coordinate currents $i_{c\alpha}, i_{c_\beta}$ are calculated from the v_α, v_β voltages with instantaneous real power (p) only and the instantaneous reactive power is set to zero. This approach reduces the calculations and implements better than the conventional methods; the compensating currents α – β coordinate are derived by using equation

$$\begin{bmatrix} i_{c\alpha} \\ i_{c_\beta} \end{bmatrix} = \frac{1}{v_\alpha{}^2 + v_\beta{}^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ 0 \end{bmatrix} \quad (12)$$

Finally, The compensation current references in the α −β coordinates are then transformed back into the a-b-c coordinates through the inverse simplified Clarke transformation as given by:

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} \quad (13)$$

These reference currents are subjected to a PSCPWM in order to generate the switching pattern for IGBT switches of MLI. The reference current waveforms and the six triangular carrier waveforms are compared to generate the PSCPWM signals for a five-level CHBMLI.

IV. Simulation Results

The operation of cascade multilevel inverter for APF is evaluated by simulating the proposed scheme in MATLAB Simulink. Three phase uncontrolled converter with R-L elements towards their dc-side is used as non-linear load. Table II shows the simulation parameters.

Table II. System parameters

AC Source Line Voltage	25 k
Frequency	50 Hz
Source Inductor	0.5 mH
Source Resistance	0.6 Ω
AC side Filter Inductance	10 mH
DC Capacitor	5000 μF
Carrier Frequency	3 KHz

The source-current detection control method by detecting the current through section III is adopted in MLI. The performance of the APF is analyzed under various operating conditions via sinusoidal and distorted voltage source with load perturbation. Simulation waveforms of the combined system in two cases are given as below.

A. Sinusoidal Voltage Source Condition

In this case three-phase balanced sinusoidal voltages supplying to three phase uncontrolled converter with R-L elements towards their dc-side as non-linear load. Three-phase source voltages, unbalanced non-linear load currents, 1-phase compensation current of MLI and source currents after compensation are shown in Fig. 6. A three-phase non-linear load with a resistor and an inductance runs at first. Thus the load current includes harmonic current and inductance reactive current. The five-level inverter generates the distorted injecting current to compensate the distorted current which 1-phase of that as shown in Fig. 6 (c). Similar current but with 120° phase shift is injected by legs 'b' and 'c' of the MLI into phases 'b' and 'c' of the distribution system. The three phase source currents after compensation is shown in Fig. 6(d) which is perfectly balanced and in-phase with the respective voltages.

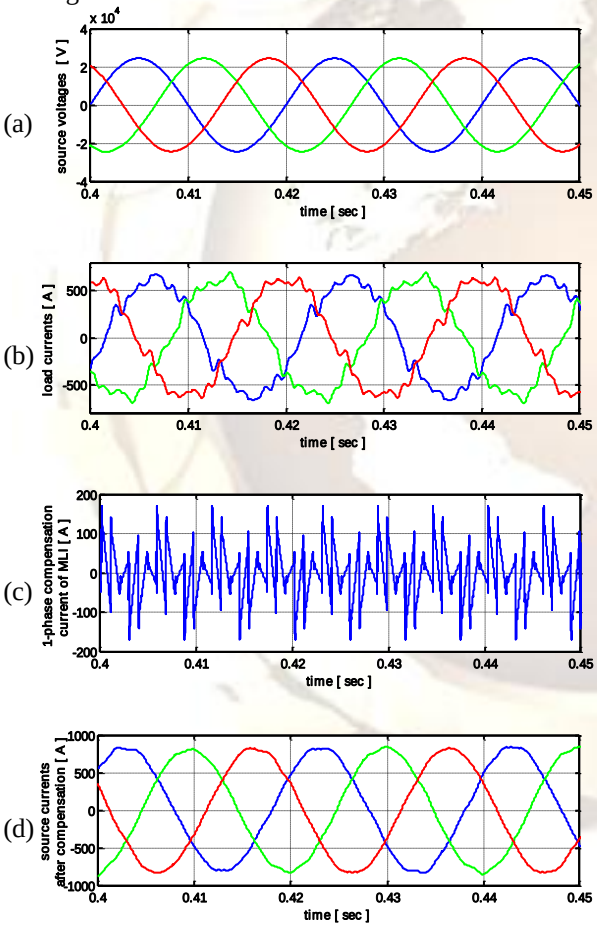

Fig. 6. Waveforms of ideal mains voltage (a), load current (b), 1-phase compensation current of MLI(c) and source current after compensation (d) in sinusoidal voltage source condition.

Fig. 7 shows the three-phase source currents before compensation. Fig. 6 (d) shows the three-phase source current waveforms after the compensator run.

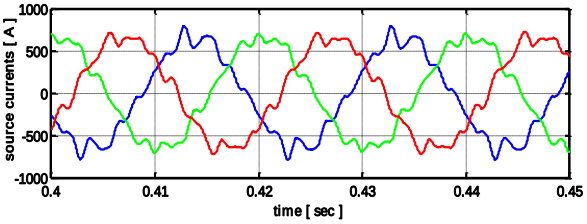

Fig. 7. Waveforms of source current before compensation in distorted supply voltage condition.

The harmonic spectrum and THD of source currents before and after compensation are shown in Fig. 8. As observed the source current THD is successfully minimized to 2.14 % as compared to the result before compensation which is 21.81 %.

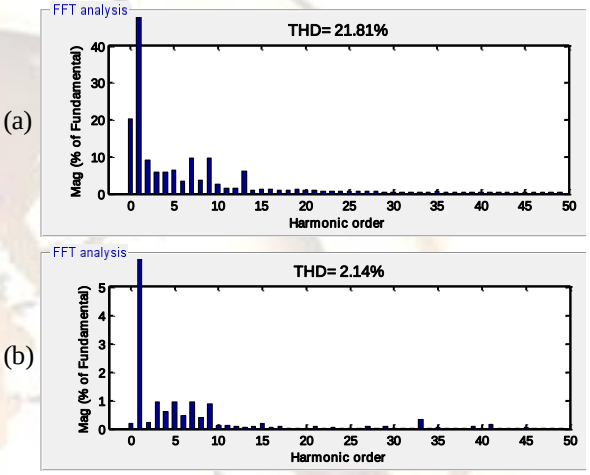

Fig. 8 Order of harmonics of source currents without (a) and with (b) five level cascaded h-bridge inverter in sinusoidal voltage source condition.

B. distorted Voltage Source Condition

In order to get a non-sinusoidal voltage for simulation study a 3rd and 5th harmonic voltage source is added in series with phase 'a', 'b' and phase 'c'. The performance of MLI with p-q theory and distorted mains voltage is represented in Fig. 9. The distorted mains voltage affects the calculation accuracy of the reference current and there will be effective for harmonic compensation, which is shown in Fig.9.

The load current is unbalanced and polluted with a harmonic distortion, since the load current wave shape in each phase is different with each other. Compensated source currents are found to be sinusoidal and balanced after compensation. The three-phase non-linear load currents before compensation are shown in Fig 9 (b) that indicate that the source current is distorted or having harmonic currents. 1-phase of distorted injecting current that generated by MLI to compensate the distorted current as shown in Fig. 6(c). For phase b and c this current is injected but with 120° phase shift. The three-phase source current after compensation is shown in Fig 9 (d) that indicates that the current is sinusoidal.

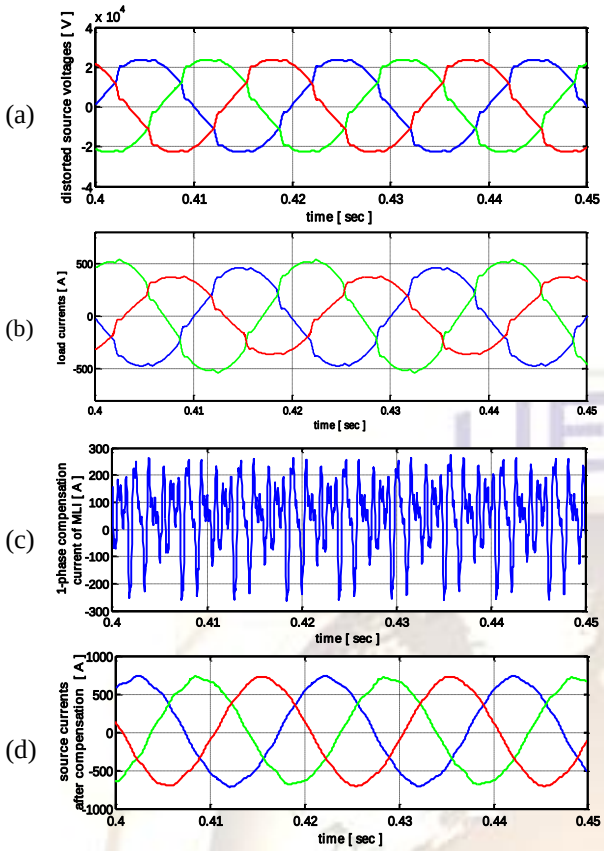

Fig. 9. Waveforms of distorted supply voltage (a), load current (b), 1-phase compensation current of MLI (c) and source current after compensation (d) in distorted voltage source condition

In Fig.10 1-phase of line side AC voltage waveform of MLI is shown.

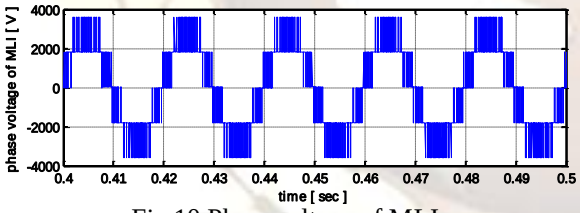

Fig.10 Phase voltage of MLI

Fig. 11 shows the three-phase source currents before compensation in distorted voltage source condition. The three-phase source current waveforms after the MLI is connected are shown in Fig. 9 (d).

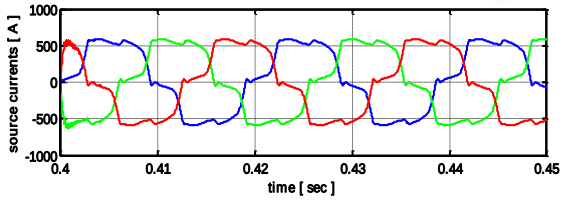

Fig.11. Waveforms of source current before compensation in distorted supply voltage condition.

The FFT analyses of source currents before and after compensation are shown in Fig. 12. This produces harmonics in the source current with the THD of 25.63% without MLI as given in the non-sinusoidal waveform of the source current is shown in Fig.11. By injecting the compensating current through the five-level cascaded H-bridge inverter the source current has become almost sinusoidal as depicted in Fig. 9 (d) and the source current THD is significantly reduced to 2.91 %.

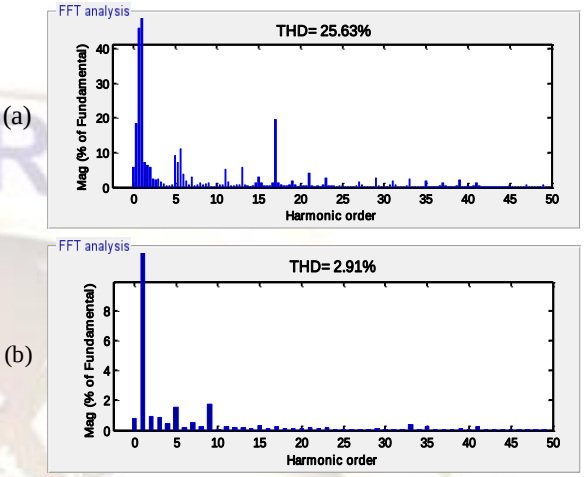

Fig. 12 Order of harmonics of source currents without and with five level cascaded H-bridge inverter in sinusoidal voltage source condition.

FFT analysis indicates that MLI with proposed controller method brings down the THD of the source current to be less than 5% in compliance with IEEE 519 and IEC 61000-3 harmonic standards [16],[17]. Thus the simulation results prove that the proposed controller method successfully compensates the harmonics even the mains voltage is non-sinusoidal and distorted.

V. CONCLUSION

In this paper cascaded H-bridge multilevel inverter based APF is implemented in distribution system. This eliminates need of high cost transformer with MLI in high voltage systems. Cascade type inverter has certain advantages as compared with other types. Positive sequence voltage detector and instantaneous real-power theory is used to generate reference currents of APF. The Phase Shifted Carrier PWM method reduces individual device switching frequency despite high frequency output of the converter. Simulated results validate that the cascaded multi-level inverter based APF can compensate harmonics without use of transformer in high voltage system. It can be concluded that the proposed technique is best suited for load compensation under unbalanced load, distorted and unbalanced supply voltage conditions. Total Harmonic Distortion of the source current has been reduced from a high value to an allowable limit to meet IEEE 519 and IEC 61000-3 harmonic standard.

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