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Test Sequence Generation of Random Single Input Change (RSIC) Based on Counter

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ABSTRACT

In any VLSI circuit, power consumption is very important factor that should be taken into consideration. Generally, dynamic power consumption is more dominant when compared to that of static. To reduce the internal switching activity rate of the circuit under test (CUT), we can recombine testing vector to raise the correlation between testing vector. Random Single Input Change (RSIC) test theory is proposed, which optimize the switching activity of circuit-under-test and then result in decrease of test power consumption. It is suitable for BIST of digital VLSI especially. The proposed circuit is simulated in DSCH and Cadence- Virtuso. The results obtained in various tools are presented in this paper.

Keywords – Built-in-self-test, Cadence Virtuso software, Test pattern generator, low power testing.

I. INTRODUCTION

In recent years, with the development of very large-scale integrated circuit and system of chip (SoC), test of integrated circuits faces more and more difficulties; especially power consumption under testing pattern is greatly higher than that under working pattern, this problem attracts more attention. Following the continuous improvement of IC working frequency integration and complex, the power consumption of IC rapidly increases. Taking Intel processor as example, its biggest power consumption increases by 100% each four years.

Especially under the technology of deep sub-micron, the width of line is smaller and smaller, so the electronic density requirement to line becomes stricter. Electric moving speed becomes faster with the rise of temperature, which leads to increase the invalid rate of connection line, thus reducing the

reliability of the whole circuits. The temperature rise caused by high power consumption also lowers the moving rate of charge carrier, which increases the switching time of transistor, then reduces the performance of system.

II.CMOS CIRCUIT ENERGY AND POWER CONSUMPTION

Power consumption in CMOS VISL is divided into two kinds static and dynamic.

2.1 STATIC:

Static power consumption is mainly produced by leak current. The structure of CMOS circuit is complementary and symmetry, only one tube is on at the same time, leak current is small, so static power consumption isn't the major part of system power consumption.

2.2DYNAMIC

Dynamic power consumption is from short circuit current generated by '0/1'or '1/0'switching of component, and from power consumption produced by discharging or charging of load capacitance. Generally speaking, dynamic power consumption is the main source of circuit power consumption.

In CMOS circuit, average dynamic power consumption P_d of one CMOS logical gate can be expressed as[4]:

$$P_d = \alpha f C_L V^2_{DD} \qquad (1)$$

In this formula, α is the rate factor of switching activity of reaction circuit, f is working frequency, C_L is output node of the whole load capacitance, V_{DD} represents mains voltage.

From formula (1) we can know dynamic power consumption in CMOS VLSI mainly depends on three parameters: mains voltage V_{DD} clock frequency f and rate factor α which reflects the switching activity rate of node . Through reducing mains voltage V_{DD} and clock frequency f , it may drop power consumption, but this way also lowers the performance of circuit. So it's a main technology to reduce power consumption through lowering the switching activity.

III. INDENTATIONS AND EQUATIONS

There is only one different vector called "Random Single Input Change" between two adjoining random vectors. It has high correlation between Random Single Input Change testing vector, which can realize low power consumption during testing through dropping switching activity rate of under-test circuit. Documentary [5]

researches the theory of single input change, it proves single input change vector can be more effective than random vector to reduce the switching activity rate of under-test-circuit node. Figure 1 shows circuit design method of RSIC sequence generated by logical circuit, which consists of n digits shift register (n-1) counter and several two input XOR.

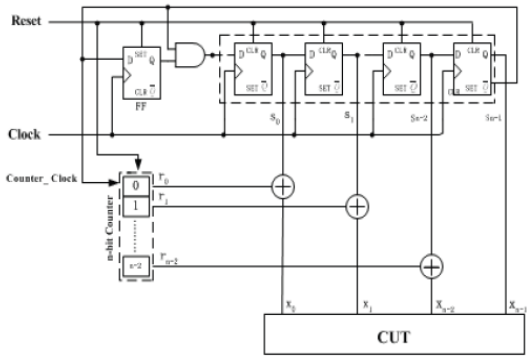


Figure3.1. RSIC TESTING GENERATOR

First of all, shift register SR is initiated to (0, 0, 0, …, 0), flip-flop is set to "1"by enable signal, FF and SR are controlled by common testing clock signal, SR produces testing vector in the (n+1) clock cycle: {(0,0,0,…,0),(1,0,0,…,0), (1,1,1,…,0), …(1,1,1,…,1)}. When next signal is started, the first level of SR is set to "o" by "or" gate, after n clock pulses, the output of SR is {(0,1,1,…,1),(0,0,1,…,1), (0,0,0,…,1), …(0,0,0,…,0)}, at
last, it recycles above process continuously.

After initiation, the output of counter stays stable during (2n+1) clock period, but SR produces (2n +1) different testing vector. Affected by signal counter-clock, SR makes "XOR calculation of corresponding digit", which can produce (2n+1) single input change (SIC) testing vector. It can be used to test power consumption for integrated circuit.

IV. SIMULATION RESULTS

4.1 Schmatics in DSCH

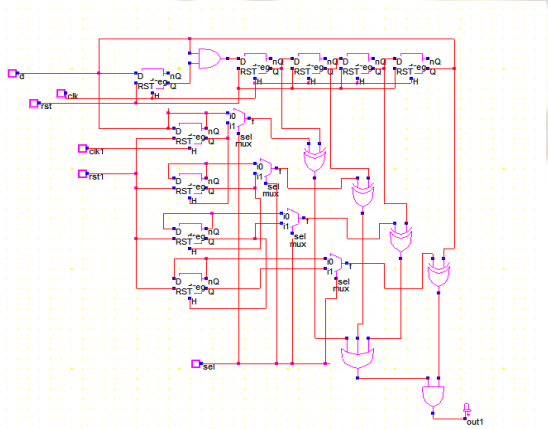
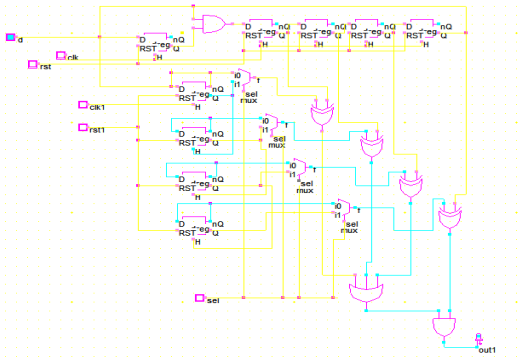
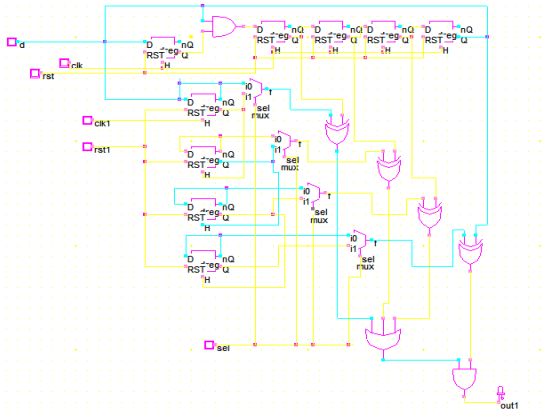


Fig1. RSIC Testing Generator in DSCH

When CUT Generating output '1':



When CUT Generating output '0':



In this DSCH tool, the correct path is displayed in one colour and the path with fault is displayed in another colour so that we can differentiate faulty paths easily.

3.2 Schematics in Cadence

In cadence, to create the entire schematic, initially it is necessary to create symbols for each and every block in the circuit. In RSIC Testing Generator, the main blocks that exist are D-Flip flop, Multiplexer, 2- input XOR gates, 2- input AND gates, 3- input OR gates. So, if we create schematics for those blocks then the respective symbols can be instantiated in the main module.

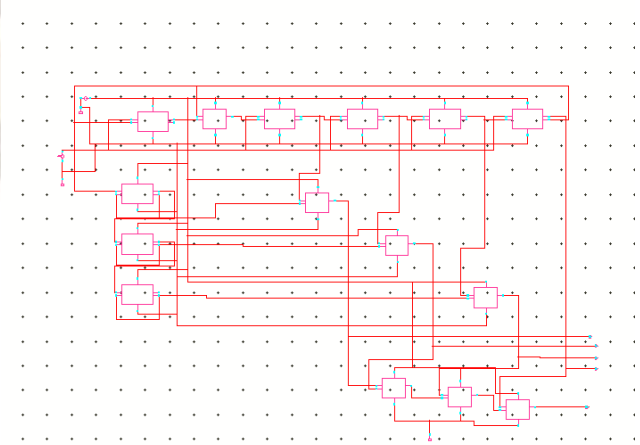


Fig 2. RSIC Testing Generator schematic in Cadence-Virtuso

The following are the output waveforms in Cadence:

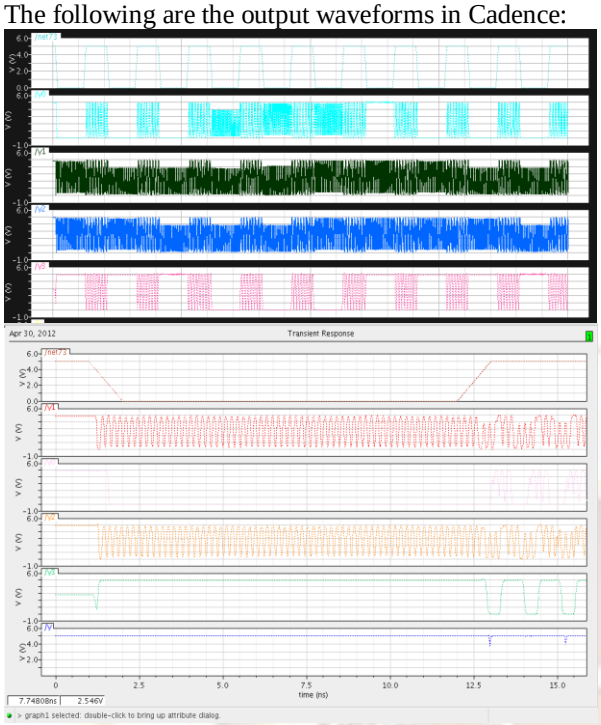


Fig3. Output waveform in cadence

Power Dissipation Values

D- Flip flop : 935.898 pW
2- input XOR gate : 1.27603 nW
2- input OR gate : 32.4249 pW
2- input AND gate : 653.021 pW
2- input NAND gate : 187.583pW
RSIC circuit : 213.034 mW
Delay in RSIC circuit is : 10.59E-9

Power dissipation values for the each module can be known while generating its transient analysis. Log file of the particular module contains its power dissipation value.

V. CONCLUSION

In this paper mainly deals with generation of random testing sequence using single input change based on counter. The research of this paper indicates single input change testing sequence has higher correlation than multi-input change. During testing, it can reduce switching activity rate α of under-test-circuit internal node in order to lower power consumption. This circuit is implemented in DSCH, Cadence and its results are mentioned in the paper.

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