Design Of 2:1 Multiplexer Using Two Phase Drive Adiabatic Dynamic CMOS Logic For Low Power Applications

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Abstract:

A MULTIPLEXER is an essential electronic device which is basically used for all kind of electronic switching. It is commonly called as data selector. The contemporary in VLSI is demanding the need of devices which dissipates low power. Adiabatic logic family is fulfilling our demands, which dissipates low power through them. In this paper, we have studied the various adiabatic logic styles: Adiabatic dynamic CMOS logic, two phase drive adiabatic dynamic logic, Glitch free and Cascadable adiabatic logic and two phase clocked adiabatic static CMOS logic. Further, we design a 2:1 multiplexer using Static CMOS and 2PADCL logic style. The 2:1 multiplexer was designed and simulated using HSPICE with 180nm technology parameters provided by predictive technology. The 2:1 multiplexer designed using 2padcl is analyzed on the basis of average power consumed by them for various values of load capacitance, input frequency and temperature. The results are then compared with static CMOS. It is observed that, multiplexer designed using adiabatic logic consumes low power in comparison to multiplexer designed using static CMOS and also, this power saving comes at the cost of increased propagation delay. Under certain operating conditions, 2PADCL of adiabatic logic design of 2:1 multiplexer successfully accomplished a power saving of upto 65% in comparison to multiplexer designed using static CMOS logic.

Keywords - CMOS; adiabatic; energy restoration; low power; 2:1 multiplexer.

I. INTRODUCTION

In this modern era of technology, people need electronic device which are portable, versatile and dissipates low power. The current static CMOS technology provide the basis for low power dissipation with an advantage of small fabrication space compared to similar technologies but still it dissipates enormous energy in the form of heat, mostly when switching. This type of power dissipation is dynamic in nature. Adiabatic logic family is a superlative approach to reduce dynamic power dissipation [1][2][3][4][5][11] and [12].

The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to recycle the energy stored in the load capacitor rather than the traditional way of discharging the load capacitor to the ground and wasting this energy. Adiabatic circuits use the following two methods to achieve low power dissipation: slow charging and discharging, and charge recycling to minimize the power consumed. Different styles of adiabatic logic have been represented by different authors in their research work [2][5][6][7][8][9][10] and [13].

In this paper, we have designed a 2:1 multiplexer using one of the adiabatic logic styles i.e. 2PADCL. Further, we compared our adiabatic logic style with static CMOS on the basis of power dissipation for different values of load capacitance, frequency and temperature.

II. OVERVIEW OF POWER DISSIPATION

The power consumed when the CMOS circuit is in use can be decomposed into two basic classes: static and dynamic.

A. STATIC POWER :

The static or steady state power dissipation of a circuit is expressed by following relation:

$$P_{stat} = I_{stat} V_{DD} \qquad (1)$$

Where, I_{stat} is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static(DC) power since in the steady state there is no direct path from V_{DD} to ground as PMOS and NMOS transistors can never turn on simultaneously. Of course, this scenario can never be realized in practice since in reality the MOS transistor is not a perfect switch. Thus, there will always be leakage currents and substrate injection currents, which will give to a static component of CMOS power dissipation.

B. **DYNAMIC POWER :**

The dynamic component of power dissipation arises from the transient switching behavior of the CMOS device. It can be further divided in two categories: Switching Power, Short circuit Power and leakage current.

Switching power is the power dissipated in MOSFET resistances while charging or discharging the load capacitances.

At some point during the switching transient, both the NMOS and PMOS devices will be turned on. This occurs for gate volatges between V_{tn} and V_{DD}-V_{tp}. During this time, a short-circuit exists between V_{DD} and ground and the currents are allowed to flow[11].

The dynamic or switching power dissipation of a circuit is expressed by the following realtion:

$$P_{dyn} = \alpha C V^2_{DD} f. \qquad (2)$$

Where, α is the switching activity which goes from 0 to 1 for every transition, C is the load capacitance, V_{DD} is the power supplied to the circuit and f is clock frequency.

As power dissipation due to leakage depends upon material used, so it is impossible to gain control over static power dissipation whereas power dissipation due to switching, logic activity and glitches is dynamic in nature and can be controlled using suitable methods.

III. ADIABATIC LOGIC

The term "adiabatic" comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure supports reducing the power dissipation across the device. Adiabatic logic is a potential successor for static CMOS design when it comes to ultralow power energy consumption. Future development like the revolutionary shrinking of the minimum feature size as well as the revolutionary novel transistor concepts will change the gate level savings gained by adiabatic logic [9].

Basically, adiabatic logic uses "reversible logic" to conserve energy. So they conserve charge by following key rules:

* Slow charging and discharging.
* Charge recycling to minimize the power consumed.

IV. CHARGING/DISCHARGING PROCESS IN STATIC CMOS AND ADIABATIC LOGIC STYLE [9][11]

CHARGING/DISCHARGING IN STATIC CMOS:

The power dissipation in Static CMOS is static and dynamic. As static power dissipation totally depends on the material used, so we are left with dynamic power dissipation, which is needed to charge and discharge the capacitive nodes in the circuit and hence is the major factor of power dissipation in Static CMOS. To charge the capacitive node upto supply potential of V_{DD}, an energy $E = CV^2_{DD}$ is needed from the power supply. When input is low, PMOS turns ON and one half of this energy ($E = CV^2_{DD}$) gets temporarily stored in load capacitor and other half gets dissipated as heat due to the ON resistance of PMOS transistor. Now, when input gets high, NMOS turns on and discharges the energy stored in load capacitor from potential of V_{DD} to ground and as heat. So, during a complete cycle of charging and discharging, the energy equivalent $E = CV^2_{DD}$ is drawn for power supply and is dissipated as heat [9][11].

ADIABATIC CHARGING/DISCHARGING:

Charging in static CMOS suffers from high potential across the switching device due to abrupt supply of power. Adiabatic logic does not abruptly switch from 0 to V_{DD} and vice versa. They use a ramp voltage to charge the capacitor to V_{DD} and recover energy from the output. The ramp voltage is generated using a time varying source to charge a capacitor. This time varying source slowly rises towards high potential ensuring no high potential across the switching device. The charging of adiabatic logic is shown in the figure 1[11]:
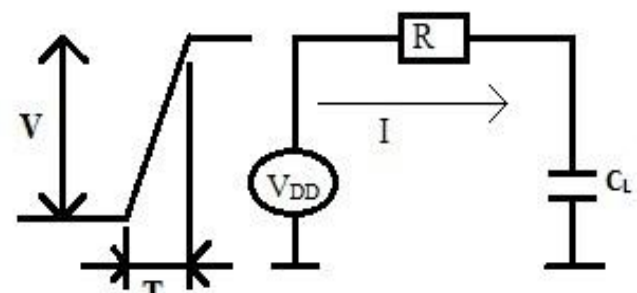

Figure 1: Adiabatic Charging.

R is the resistance in the charging path across the circuit, consists the ON resistance of the PMOS transistor in the charging path. So the current will be [11]:

$$I = C_L V_{DD}/T \qquad (3)$$

Thus energy dissipated during charging can be written as [11]:

$$E_{Diss} = (RC_L/T)C_L V^2_{DD} \qquad (4)$$

Whole process consists of charging and discharging. Discharging process will also led to same amount of energy dissipation, so the overall dissipation of energy across adiabatic logic can be represented as [11]:

$$E_{DISS} = 2 \; (RC_L/T)C_L V^2_{DD} \qquad (5)$$

From equation (3), we can see that slower the circuit is charged, less will be the energy dissipated across the circuit. Larger the value of T, less will be the power dissipation.

V.ADIABATIC LOGIC STYLES

In recent years, many adiabatic logic styles have been described by different researchers in their research works Different styles of adiabatic logic have been represented by different authors in their research work [1][2][5][6][7][8][10] and [13]. These adiabatic logic styles differ in their circuit complexity and number of power clocks. Due to the different circuit complexity and different number of power clocks, adiabatic logic differs in their working process and gives different advantage over one another for different applications. The adiabatic logic can easily be derived from known static CMOS without doing any much change in the configuration. In this section we will study about following adiabatic logic styles: adiabatic dynamic CMOS logic, two phase drive adiabatic dynamic CMOS logic, glitch free and cascadable adiabatic logic, two phase clocked adiabatic static CMOS logic.

A. Adiabatic dynamic CMOS logic(ADCL)

Adiabatic dynamic CMOS logic was proposed by K. Takahashi and Mizunuma [5]. It is a diode based adiabatic logic which uses one power clock and is used for low power applications. The clock used is either sinusoidal or triangular. It uses two rectifying diodes, one each in charging and discharging path to control the charge flow. We have used MOSFET as diode by shorting gate and drain of MOSFET together. The sources that may cause energy dissipation in this logic family are threshold voltage of MOSFET, diode cut in potential and energy dissipated in resistance of MOS devices. The use of slowly varying power clock ensures the small energy dissipation across the ON resistance of MOS devices [9].

This logic style comes with major drawbacks: the problem of delay associated with it [5]. The propagation delay in this logic family depends on period/frequency of power clock. Beside the delay problem, it also requires a load capacitor to hold the output. The schematic of an inverter using this logic family along with resulting waveforms after simulation is shown in fig.2 [5] [9]:
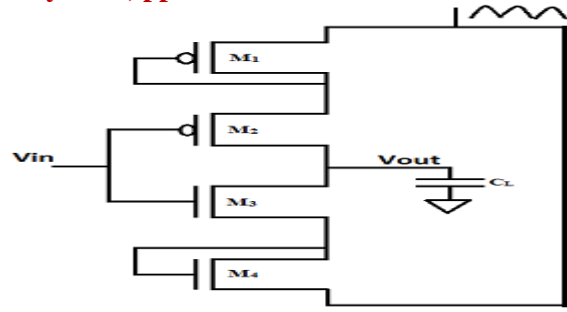

Figure 2: ADCL inverter.

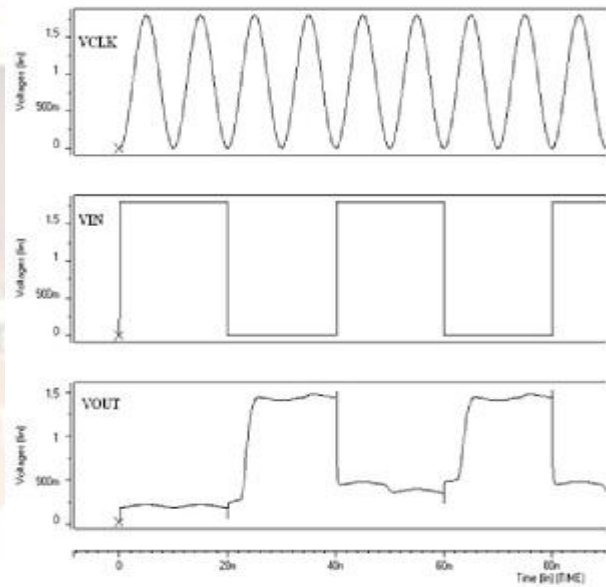The resulting simulations of ADCL are shown below in fig.3:

Figure 3: Waveform after simulation.

B. Two phase drive adiabatic dynamic CMOS logic(2PADCL)

The problem associated with ADCL is its delay. To overcome this delay, Y. Takahashi et al [13] introduced 2PADCL. The two phase drive adiabatic dynamic CMOS logic resembles the behavior of static CMOS. It uses complementary two phase supply with 180° phase shift. These supplied clock waveforms consists of two modes "evaluation" and "hold" [9]. When both power supplies, V_{clk} and V_{clk}' are in evaluation mode, there is an conducting path in either PMOS devices or NMOS devices. Output node may evaluate from high to low or low to high or will remain unchanged. Output node will hold its value when $V_{clk \; and} \; V_{clk}$' are in hold mode. Circuit nodes are not necessarily charging and discharging every clock cycle, reducing the switching activity. Reducing the switching activity leads to the faster performance of 2PADCL in comparison to ADCL circuits [13].

The threshold voltage of MOSFET, diode turn on voltage and dissipation across conducting MOSFETs are the major sources of energy dissipation in 2PADCL. The schematic of an inverter using this logic family along with resulting

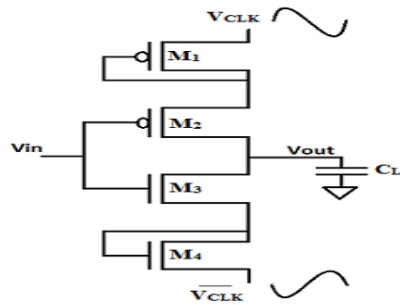waveforms after simulation is shown in fig. 4 [9] [13]:

Figure 4: 2PADCL inverter

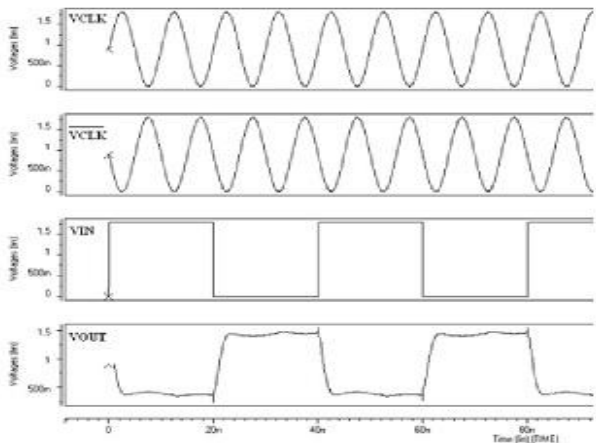The resulting simulations of 2PADCL are shown in fig. 5 below:

Figure 5: Waveform after simulation.

C. Glitch free and cascadable adiabatic logic(GFCAL)

This logic family was introduced by Reddy, Satyam and Kishore et al [10]. GFCAL is simple and does not require complimentary signals or complex clocking. It uses single clock signal as supply and uses rectifying diodes at both charging and discharging path, so that ripples does not occur and it becomes suitable for cascadable operations [10]. Like 2PADCL, we have used MOSFET as diode by shorting gate and drain.

Its drawback is the use of rectifying diodes for controlling the charging and discharging of output nodal capacitance. These rectifying diodes are responsible for power dissipation due to the cut in voltage drop across them. The schematic of an inverter using this logic family along with resulting waveforms after simulation is shown in fig.6 [9]:
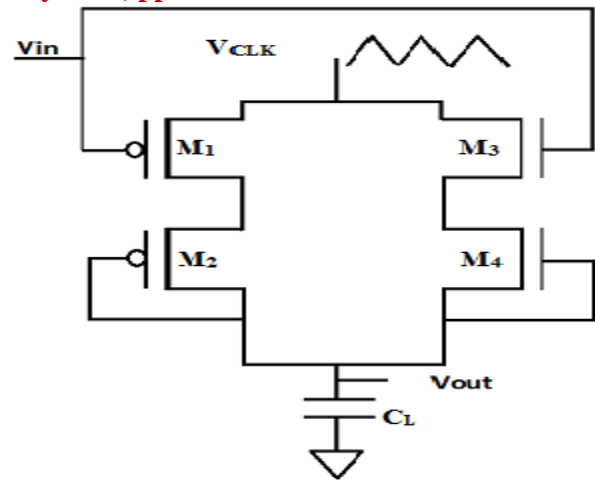

Figure 6: GFCAL inverter.

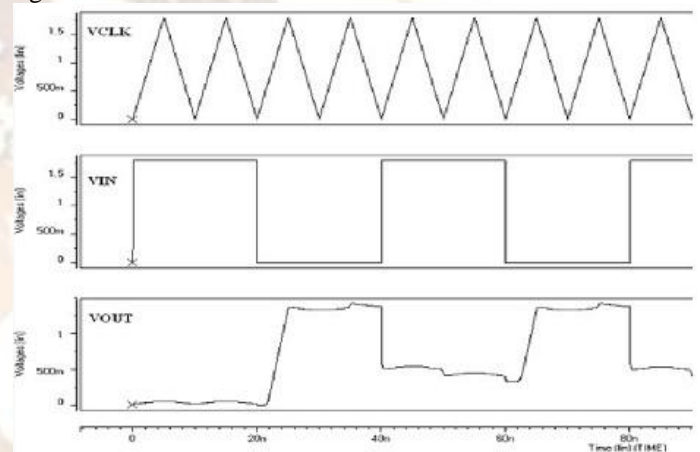The resulting simulations of GFCAL are shown in fig. 7 below:

Figure 7: Waveform after simulation.

This adiabatic logic style introduces delay. The use of single power clock is the reason for delay in this logic family.

D. Two phase clocked adiabatic static CMOS logic(2PASCL)

The logic style we have discussed so far: ADCL, 2PADCL and GFCAL, all suffers from the problem of output amplitude degradation as they use diode in charging path. To overcome output amplitude degradation, Annur et al [6][7] proposed new logic family named 2PASCL.

The removal of diode from the charging path, 2PASCL will lead to higher amplitude and also, power consumption due to diode is reduced. 2PASCL uses two complementary split level sinusoidal power supply clocks whose peak to peak value is equal to $V_{DD}/2$ [7].

Dissipation of power in 2PASCL is because of threshold voltage of MOSFET, diode cut-in

potential and dissipation in resistance of PMOS and NMOS while charging or discharging the load.

The schematic of an inverter using this logic family along with resulting waveforms after simulation is shown in fig 8 [9]:
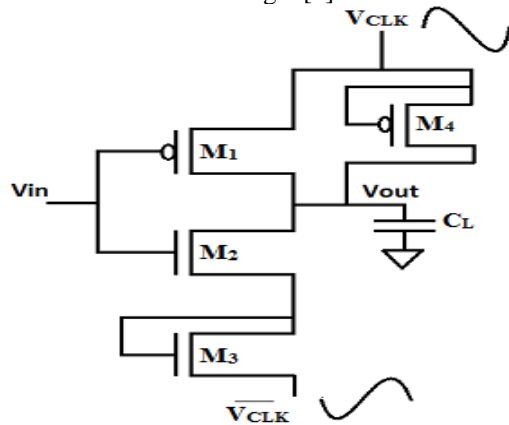

Figure 8: 2PASCL inverter.

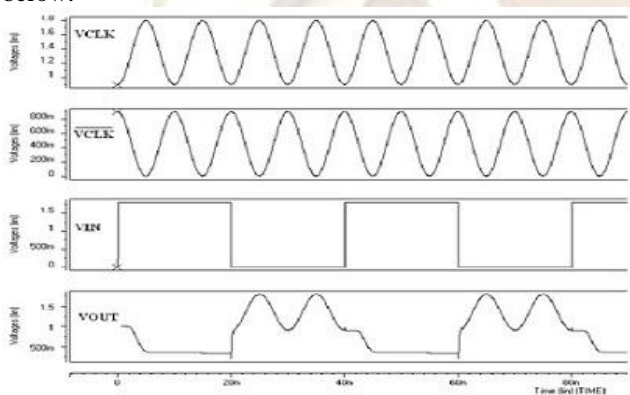The resulting simulations of 2PASCL are shown in the fig. 9 below:

Figure 9: waveforms after simulation.

E. Static CMOS logic

All the logic style we have studied so far, were based on basic static CMOS style. The basic static CMOS inverter consists of complimentary transistors, PMOS and NMOS. Both PMOS and NMOS are connected in series with a power supply of V_{DD}. This configuration helps increasing the processing speed by reducing resistance compared to NMOS-only or PMOS-only type devices. Also, it reduces the power consumption since one of the transistors is always remains off in both logic states.

The schematic of an inverter using static CMOS inverter along with resulting waveforms after simulation is shown in fig. 10:
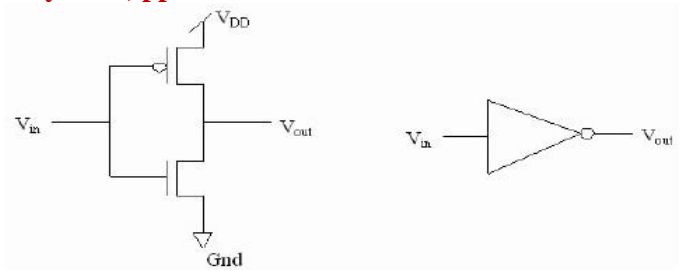

Figure 10: Static CMOS inverter.

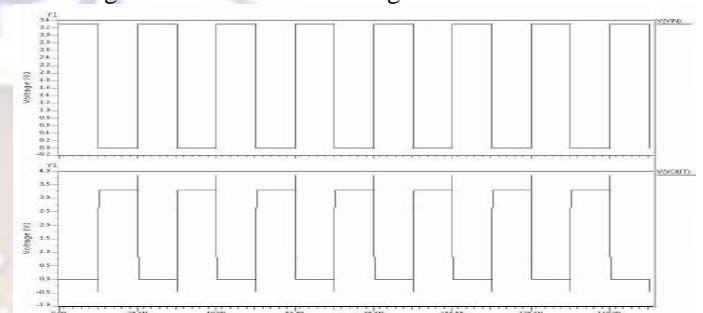Simulation of Static CMOS inverter results in following waveform as shown in fig. 11:

Figure 11: waveforms after simulation.

So far we have discussed about inverters using ADCL, 2PADCL, GFCAL, 2PASCL and Static CMOS. On discussing them, we found that ADCL can be used as multiplexer to save power dissipation but it suffers from the problem of significant propagation delay problem as it uses single power clock, GFCAL also suffers from the problem of propagation delay as it also uses single power clock and 2PASCL suffers from the problem of ripples in the output. So, we used 2PADCL to make a 2:1 multiplexer as it significantly cure the problem of propagation delay by using two power clocks and also, it does not suffers from the problem of ripples in the output as in the case of 2PASCL. Further, now we will discuss on the multiplexers based on Static CMOS and 2PADCL.

VI. DESIGN AND SIMULATION OF A 2:1 MULTIPLEXER

In this section, we have designed and simulated a 2:1 multiplexer using Static CMOS and 2PADCL. The 2:1 multiplexer is designed and simulated by HSPICE and we have used 180nm technology parameters provided by predictive technology. The supply voltage V_{DD} is 1.8v and the body terminals of NMOS and PMOS are connected to GROUND and V_{DD} respectively. The length and width of MOSFETs are L = 180nm and W = 720nm respectively and the operating temperature is chosen is 25°C. The power clock is kept at 100MHz, input selected are D_0=12.5Mhz, D_1=8.33Mhz and S=25Mhz. Diodes used are made from MOSFET by

shorting gate and drain terminal of NMOS and PMOS respectively.

A. Design and Simulation of a 2:1 Multiplxer using Static CMOS logic.
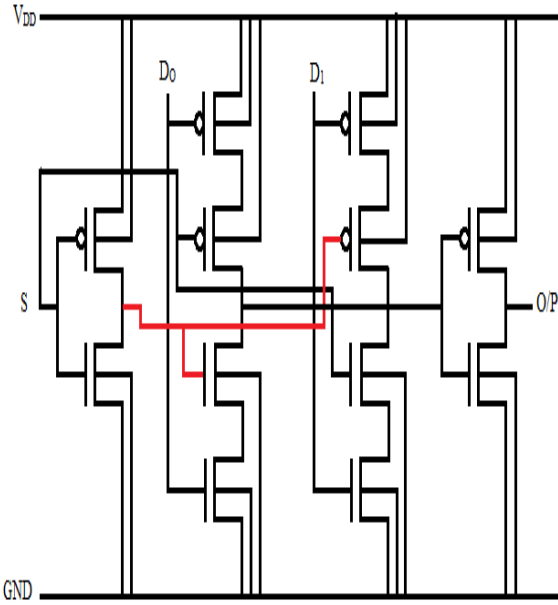

Figure 12: 2:1 multiplexer using Static CMOS.

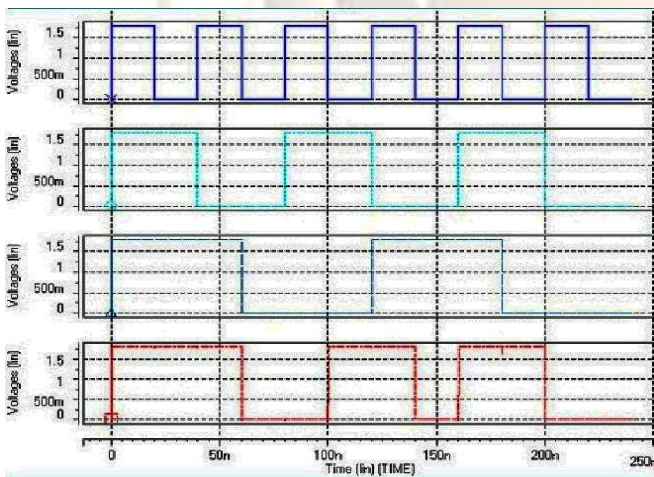Simulations results of waveforms for 2:1 multiplexer using static CMOS are as shown in fig. 13:

Figure 13: Waveforms after simulation.

The above waveforms after simulation indicates that Static CMOS multiplexer gives a ripple free output without any significant propagation delay problem.

B. Design and Simulation of 2:1 Multiplexer using Adiabatic 2PADCL:

It implements the function F = $(D_0)(S') + (D_1)(S)$. When the select(S) signal is low, it selects the signal D_0 and steers it to the output and when the select(S) signal is high it outputs the signal D_1, respectively. The multiplexer based on adiabatic 2PADCL uses complementary two phase supply signals as input. The power clock is 100MHz, input selected are D_0=12.5Mhz, D_1=8.33Mhz and S=25Mhz, and the operating temperature is 25°C. The design of 2:1 multiplexer circuit using adiabatic 2PADCL is given below in fig. 14:
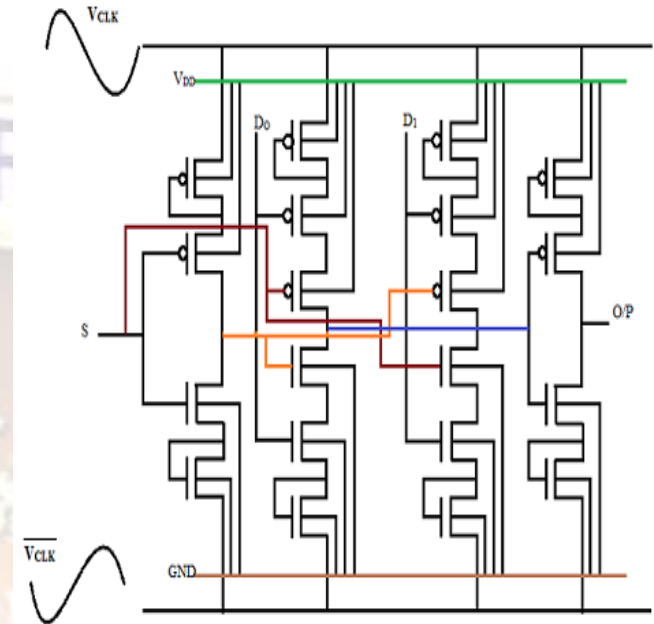

Figure 14: 2:1 multiplexer using 2PADCL.

As to avoid confusion and for better understanding, we made a coloured power supply, ground and select. The waveforms resulting after Simulation of multiplexer using 2PADCL are as shown in Fig. 15.
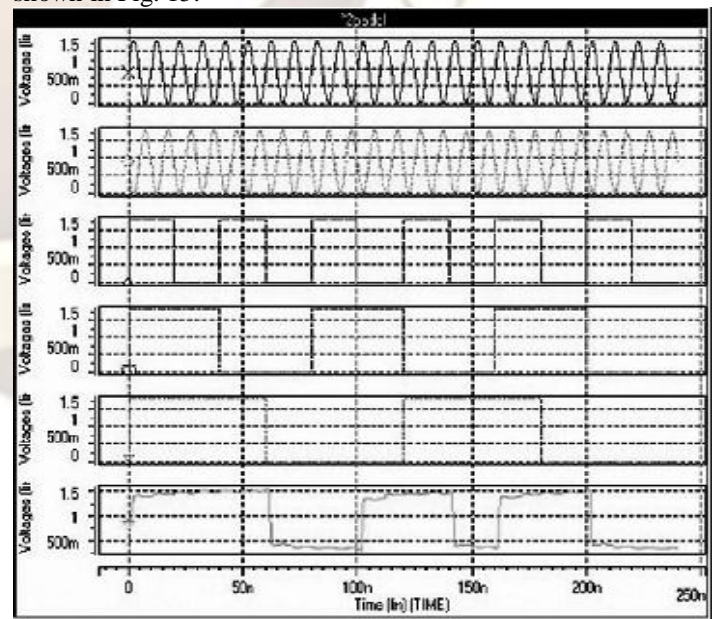

Figure 15: Waveforms after simulation.

As can be seen from the fig. 15, that because of the use of diodes in charging and discharging path, we are getting ripple free output and also, the use of complementary sin waves eliminates the problem of delay, as associated with ADCL and GFCAL with an advantage of low power dissipation across the circuit.

C. COMPARISON OF MULTIPLXER ON THE BASIS OF DIFFERENT PARAMETERS:

We have so far designed and simulated 2:1 Multiplexers based on static CMOS and adiabatic 2PADCL. But this simulation is based on constant load capacitance, constant frequency and constant room temperature. But in the real world, multiplexer need to be work on varying parameters and varying conditions. So, now we will observe the effect of varying condition or varying parameters on Static CMOS Multiplexer and Multiplexer based on adiabatic 2PADCL and observe, why multiplexer based on adiabatic 2PADCL is better in power savings then Multiplexer based on Static CMOS. The 2:1 static CMOS Multiplexer and 2:1 adiabatic 2PADCL Multiplexer were compared on different varying parameters on the basis of power dissipation across them.'

i) Average power consumed by 2:1 Multiplexer designed with static CMOS family and 2PADCL family for different values of load capacitence.

In this section, we have observed the effect of variation in load capacitance over the average power consumed by 2:1 multiplexer based on Static CMOS and Adiabatic 2PADCL. The load capacitance is varied from 10-190fF with a step size of 20fF and resulting power consumption is observed. The operating temperature is kept constant i.e 25^oC. Input selected are D_0=12.5Mhz, D_1=8.33Mhz and S=25Mhz. The effect of variation of load capacitance over power dissipation is shown in the table below:

Table I : Variation of Avg. Power Consumption with Load Capacitance.

Load capacitance C_L (fF)	Power Dissipation Of CMOS	Power dissipation of 2padcl mux	Power reduction μw	% of Power reduction
10	2.249	1.019	1.23	54.69
30	3.03	1.3761	1.654	54.58
50	3.829	1.692	2.137	55.81
70	4.632	1.977	2.655	57.31
90	5.439	2.233	3.206	58.94
110	6.246	2.467	3.779	60.50
130	7.054	2.679	4.375	62.02
150	7.863	2.875	4.988	63.43
170	8.672	3.054	5.618	64.78
190	9.481	3.216	6.265	65.07

On the basis of simulation results shown in Table I, a graph has been plotted showing the variation of power consumption by Static CMOS Multiplexer and 2PADCL Multiplexer:
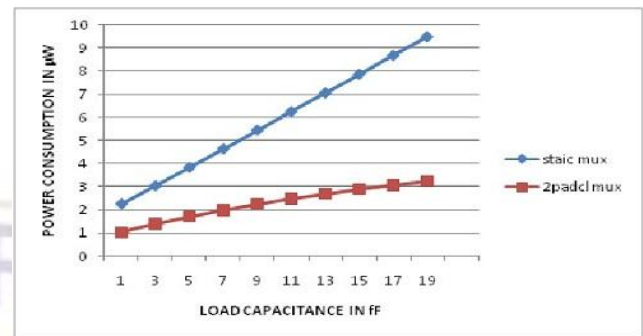

Figure 16: Variation of Avg. Power Consumption with Load Capacitance.

The average power dissipation increases with the increment in load capacitance. As can be seen from the graph I, with increase in load capacitance, the power dissipation across Static CMOS multiplexer increases significantly but in multiplexer using 2PADCL, this power dissipation is not increasing at the rate as with the case of multiplexer using Static CMOS. With constant temperature and power clock supply and varying load capacitance, the multiplexer using 2PADCL tends to offers upto 65% of power saving in comparison to multiplexer based of Static CMOS.

ii) Average power consumed by 2:1 Multiplexer designed with static CMOS family and 2PADCL for different Input frequecies.

In this section, we have observed the effect of variation in frequency over the average power consumed by 2:1 multiplexer based on Static CMOS and Adiabatic 2PADCL. We have kept power clock frequency to be 100MHz. While varying the frequency of inputs, we have kept temperature and load capacitance constant. The variation in T_{SON} kept between 20-200ns with a step size of 20ns. The temperature is kept 25^oC.

As, frequency is inversely proportional to the time period of the wave $T = 1/f$, so by varying the time period T_{ON} of a wave, we can observe power dissipation for different values of input frequencies, where $T = T_{ON} + T_{OFF}$ and the wave is square in nature with $T_{ON} = T_{OFF}$. So, more the time period, lower will be the frequency, and less will be the power dissipation. Also, as multiplexer has two inputs and a select line: D_0, D_1 and S, so we have selected their time periods as $T_{D0} = 2T_S$ and $T_{D1} = 3T_S$. As we have mentioned the relationship between time periods of both input and select line, the time period of all three will vary, as a fact frequency will also vary.

Table II : Variation of Avg. Power Consumption with Varying Time Period..

T_{SON} of select line	Power Dissipation Of CMOS In µw	Power dissipation Of 2PADCL In µw	Power reduction In µw	% power reduction
20	3.116	1.195	1.921	61.64
40	1.355	0.6200	0.735	54.24
60	0.8337	0.4211	0.4126	49.49
80	0.5696	0.3036	0.266	46.69
100	0.4681	0.2522	0.2159	46.12
120	0.3974	0.2136	0.1838	46.25
140	0.3569	0.1986	0.1583	44.35
160	0.3072	0.1684	0.1388	45.18
180	0.2581	0.1393	0.1188	46.02
200	0.2307	0.1221	0.1086	47.07

On the basis of simulation results shown in Table II, a graph has been plotted showing the variation of power consumption by Static CMOS Multiplexer and 2PADCL Multiplexer:
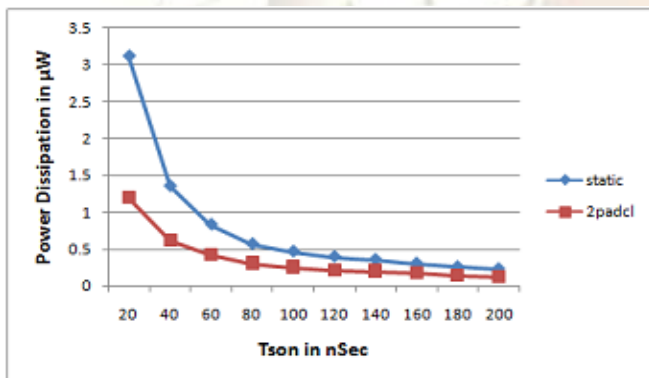

 Figure 17:Variation of Avg. Power Consumption with Varying Time Period

As can be observed from the Fig. 17, with increase in frequency, the power dissipation across multiplexer using Static CMOS and 2 PADCL is increasing. At low freqencies, the power dissipation is less. With constant load capacitance and consrant temperature and varying frequency, the multiplexer using 2PADCL gives a power saving upto 61% in comparison to multiplexer using Static CMOS.

iii) Average power consumed by 2:1 Multiplexer designed with static CMOS family and 2PADCL for different operating temperature.

In this section, we have observed the effect of variation in temperature over average power consumed by 2:1 multiplexer based on Static CMOS and Adiabatic 2PADCL. While varying the temperature, we have kept constant frequency and constant load capacitance. The variation in

temperature is kept between 10°-90°C with a step size of 10°C. The power clock used is of 100MHz and the load capacitance is kept at a value of 10fF. The effect of variation of temperature on power dissipation of multiplexer using Static CMOS and 2PADCL is shown in the table III below:

Table III : Variation of Avg. Power Consumption with Varying Temperature.

Temperature In °C	Power dissipation Of CMOS In µw	Power dissipation Of 2PADCL In µw	Power Reducti -on In µw	% power Red- uction
10	2.239	0.9921	1.2469	55.69
20	2.245	1.009	1.236	55.05
30	2.255	1.029	1.226	54.36
40	2.267	1.050	1.217	53.68
50	2.277	1.071	1.206	52.96
60	2.292	1.095	1.197	52.22
70	2.309	1.118	1.191	51.58
80	2.363	1.142	1.221	51.67
90	2.387	1.167	1.220	51.11

On the basis of simulation results shown in Table III, a graph has been plotted showing the variation of power consumption by Static CMOS Multiplexer and 2PADCL Multiplexer:
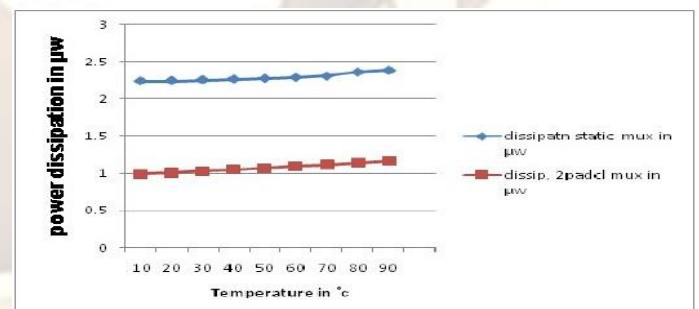

Figure 18: Variation of Avg. Power Consumption with Varying Load Capacitance.

As can be observed from the Fig.18, with increase in temperature, power dissipation across multiplexer using Static CMOS and 2PADCL is increased. The reason for increase in dissipation is static power dissipation associated with it, which occurs due to sub threshold current and leakage current. At normal temperature the power dissipation due to sub threshold and leakage current can be ignored. But with increase in temperature, the dissipation due to sub threshold and leakage starts

increasing and contributes effectively to the overall power dissipation of the circuit.

The power saving in multiplexer based on 2PADCL is 55% more as compared to multiplexer based on Static CMOS. This power saving decreases with increase in temperature as sub threshold and leakage current starts increasing across the circuit.

VII. CONCLUSION

With this research paper, we have successfully designed a 2:1 multiplexer based on 2PADCL adiabatic logic and Static CMOS. With adiabatic logic switching approach, the circuit energy is retained rather than dissipated as heat. We compared the results based on average power dissipation in both the circuit on various parameters like varying load capacitance, varying temperature and varying frequency. We found that under certain operating conditions, the 2:1 multiplexer based on 2PADCL adiabatic logic style can save power upto 65% as compared to 2:1 multiplexer based on Static CMOS. Although, multiplexer based on 2PADCL is having delay and circuit complexity than multiplexer based on Static CMOS but with the advantage of high power savings, 2PADCL multiplexer is advantageous in applications where power saving is of prime importance as in high performance portable digital systems running on batteries such as palmtops, note book computers, smart phones etc.

VIII. ACKNOWLEDGMENT

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