

## Electromagnetic Modeling of Electronic Package wirebond

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### ABSTRACT

This paper will describes the modern packaging issues and the simulated studies using CST MWS as electromagnetic full wave solver.

In fact, the aim of this study is to present the impact of the contribution of the geometrical parameters and to know how much it is the impact on. In the other hand, the position of a BW is not exact as it was expected, then an error evaluation of the difference in return loss between theoretical and practical bond wire positions is simulated to know how much it is the impact on. The simulation is performed using CST MICROWAVES software, whose calculations are based on The Finite Integration Technique (FIT).

**Keywords** - Bond Wire, Cross talk, Geometrical parameters, processes error.

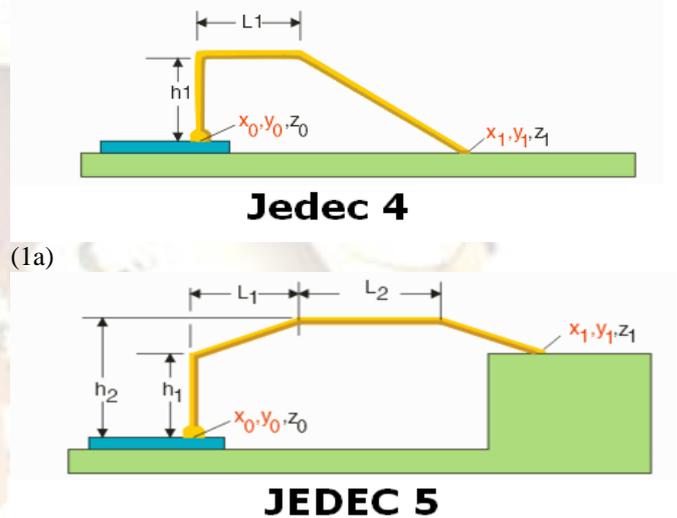
### 1. INTRODUCTION

Cross talk (XT) is an electromagnetic phenomena caused by undesired capacitive, inductive, or conductive coupling from one circuit, part of a circuit, or in our case: bond wires and electrical paths, resulting in undesirable effect on other bond wires or circuits behavior and leading to signal performances degradation such as distortion and attenuation. Actually the information lack about bond wire behavior oblige academic and professionals researches to use approximated models for the bond wires such transmission lines since the size of package elements becomes comparable or smaller to the travelling wavelength at microwave and millimeter-waves.

The bond wire is a thin cable of often  $25\mu\text{m}$  diameter (1 mil) and of a length between 200  $\mu\text{m}$  and several mm (i.e. 4mm) made up by gold, copper or aluminum. It is used to connect die pads, which are supposed to be input/output electrical connection of the chip, to the finger pads and then via a series of traces and vias. The electrical connections find its way to the outside of package. The bond wire can have different profiles, fig.1, standardized by organizations such as JEDEC and they are summarized in four mains categories:

- JEDEC4: having four coplanar points to be defined (see Fig.23).
- JEDEC5: Having five coplanar points to be defined (see Fig.23).
- Spline shape: Having a smooth arc and this geometry is very used for RF connections.

- Ribbon: Is like a strip having a section of  $13 \times 75 \mu\text{m}^2$ . This profile is well used for supplying high power such as for power transistors, amplifiers and antennas in package (AiP).

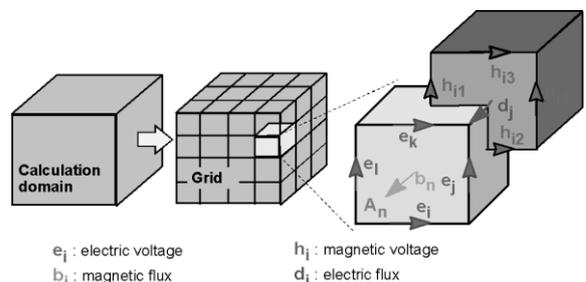


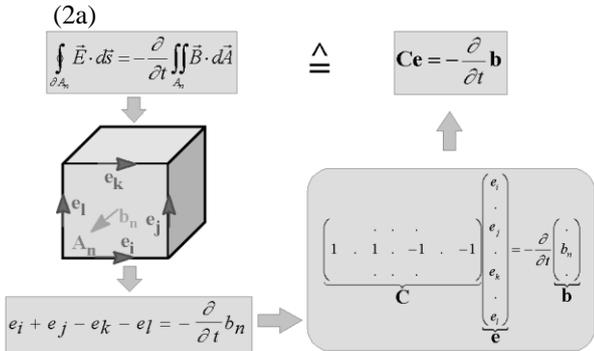
(1a) Figure 1 : WireBonde profiles ;(a) Jeduc 4 ; (b)Jeduc 5

### 2. DESIGN TOOLS & FIT

The Finite Integration Technique (FIT) is a time-domain numerical method based on the integral form of Maxwell's equations. The FIT is a consistent formulation for the discrete representation of Maxwell's equations on spatial grids. First proposed by Weiland in 1977, the finite integration technique can be viewed as a generalization of the FDTD method. It is also similar to the finite element method.

This numerical method provides a universal spatial discretization scheme (fig.2), applicable to various electromagnetic problems, ranging from static field calculations to high frequency applications in time or frequency domain.

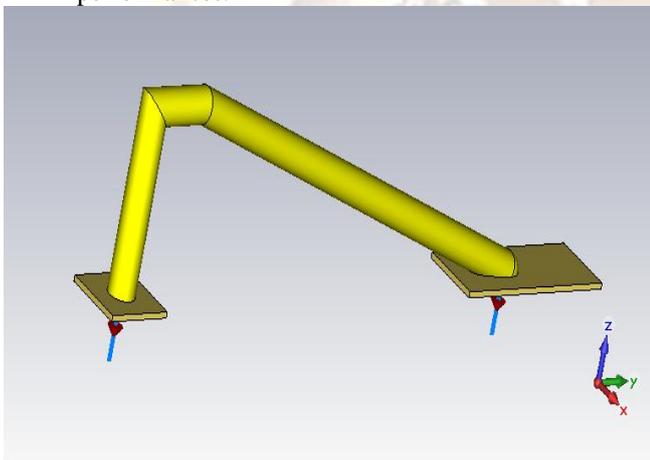




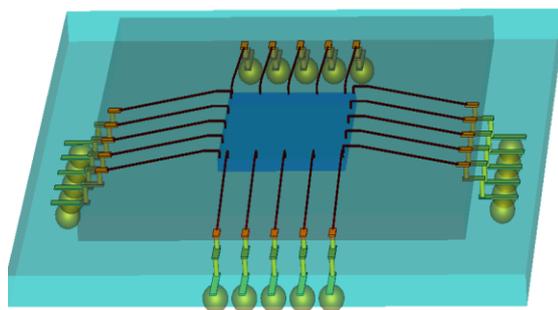
(2b)  
 Figure 2: Allocation field components: (a) macroscopic picture and (b) fields relationship in one cell

### 3. WIRE-BOND SIMULATION STUDY

Epoxy mold compound is one of the key words in electronic package industry; this is the medium encapsulating the die, the bond wires and the substrate. The choice of the mold is critical area for both thermal-mechanical and electrical performances.



(3a)



(3b)  
 Figure 3: example of simulated WireBonde; (a) off-chip & without mold; (b) WB with mold.

#### 3.1 Study of wire bond material impact:

In this part of study the material choice influences on the scattering parameters of a bond wire. Copper wire bond is less expensive compared to the gold one which is cost is increasing every time. The main problems of copper WB occurs at

the processing moment where the temperature is very high causes copper erosion due to the existence of several di-oxides and the higher stress on the chip required to attaching copper wire on the die pads. However, in term electrical performance and costs, the copper wire is an excellent choice because of his higher electrical conductivity and much better its reflection coefficient compared to the gold wire.

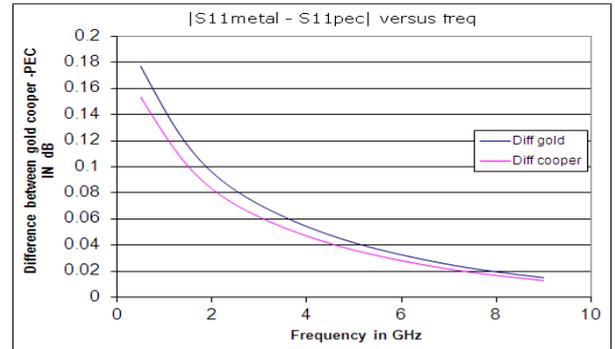
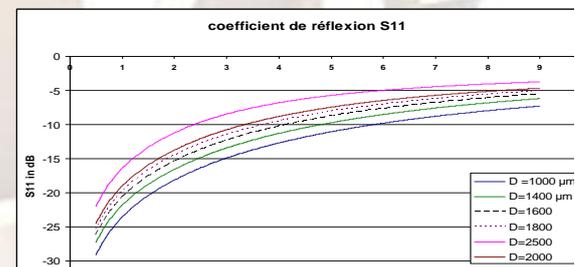


Figure 4: |S11metal – S11PEC|  
 It is clear from the diagram, that the copper optimizes the transmission, in fact, in recent year the companies is immigrates to the cooper wire technology, that's means best productivity.

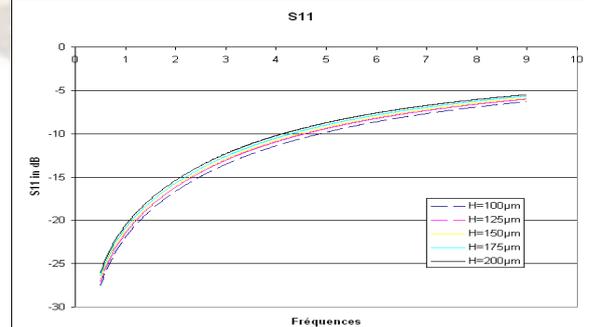
#### 3.2 Wire bond parametric study:

In this part of study, we are interested by the contribution of the geometrical parameters, that's why we have simulate the effect of horizontal bond wire distance & bond wire height effects.

In the first step we will modify the bond wire height by +/- delta (where delta = 25 μm) and the second step we will modify the horizontal length by ±Δ (where Δ=1mil= 25.4μm).



(5a)



(5b)

Figure 5 : S11 versus frequencies: (a) for different distances;(b) for different height.

Fig.5 illustrates the results of horizontal distance and height variations effect on the return loss parameter. It has been shown that return loss increases versus frequency when the total length increases (the sum of BW height, horizontal length and oblique length), or Manhattan length. As result and suggestion, It is preferable to use the shorter bond wire length in the interconnection, this why manufacturer has immigrated to the flip chip technology.

### 3.4 Processing error

Through this part, we are going to present the result of study of the side effect of processing error of bond wire. In fact, The fabrication process is not perfect, the position of a BW is not exact as it was expected, then an error evaluation of the difference in return loss between theoretical and practical bond wire positions is simulated to know how much it is the impact on.

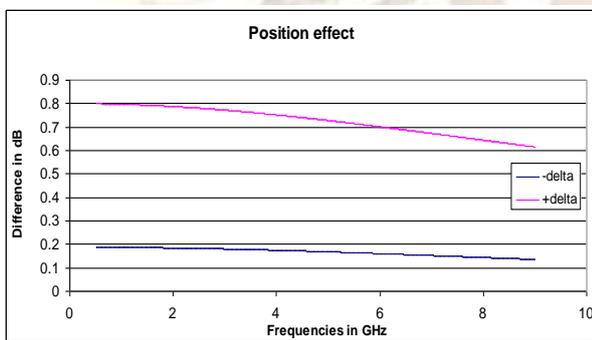


Figure 6: comparison of S11 difference between Theo. & longer height and between Theo. & shorter height.

As shown in fig.6, in the case of « + $\Delta$  » that means the length of the wire is longer there are more reflections of power.

From these results, we note that there is an effect, in the case of position effect, the error approximately equal to  $\pm 0.8$ dB, and  $\pm 0.3$ dB in the case of the height effect.

## 4. CONCLUSION

This work starts with geometry modeling for both on-chip and off-chip interconnects followed by extensive electrical performance investigation.

During our work we have focused on the return loss parameter because it is characterizes essentially any two ports structure- the bond wire is one of them- a lower return loss parameter values means better values for transmission coefficient if there are no conduction or dielectric losses. In addition, the effect of geometrical and processing error was analyzed

Design insight and suitable guidelines for minimizing interconnect inductance are in phase of investigation, electrical parameter extraction, such

as capacitance and inductance, for arbitrarily shaped objects are presented, which provide a direct link between design parameters and electrical performance. An approach using 3D modeling of the geometry for bonding wires for RF applications and packages is demonstrated.

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